CAMAC

4CH FADC

MODEL RPC-081

Instruction Manual

REPIC

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Introduction

Thank you for selecting our 4ch FADC module. This module is developed for measurement of fast analogue signal.
Analogue signal from any kind of detectors can be digitized with the fast ADCs and digitized data can be transferred via the standard CAMAC bus. The module consists of analogue amplifiers, fast ADCs, and fast memories. The 4 channels can be operated in parallel.
The gain of the amplifier and offset of the ADC input can be adjusted with two variable registers equipped for each channel.
This module is designed based on the CAMAC standard and is appropriate for various kind of experiments and measurements.

Note

- Please turn off the power when you insert the module into a crate.
- Amplifiers are equipped in the input stage of the module for adjusting the signal amplitude to the ADC and variable registers are also equipped for offset adjustment.
- Data is read by Q-stop mode.
- There is a jumper switch in the module for selecting LAM enable and disable functions. Please be careful when you start to use. The initial setting of the jumper switch is in the enable mode.

*It is impossible to select the mode via a CAMAC function.

- It is possible to select with a jumper switch which clock signal you use, internal or external. The jumper should be set at EXT for external clock use and at INT for internal clock use. The switch is set at INT when the module is delivered.

Specification

Number of channels:	4 channels
Dynamic range:	8 bits
Data sampling:	100MHz sampling (Internal Clock)
	Possible to use an external clock by setting a jumper switch
Data memory:	1k word/channel
Analogue input:	Amplification gain -2
	Offset -5V ~ 5V
	Set at -2V when delivered without input signal
	50 ohm impedance
Start signal:	Negative NIM
	50 ohm impedance
	Minimum pulse width is less than 10nsec
Stop signal:	Negative NIM
	50 ohm impedance
	Minimum pulse width is less than 10nsec
External clock input:	Negative NIM
	50 ohm impedance
	Maximum repetition rate is above 125MHz
ADC chip:	CXA1396D (SONY)
	Input to the ADC should be 0V ~ -2V
Connectors:	85QLA-01-0-2 (Suhner) 7 pieces

CAMAC functions:

N F(0) A(0~3):	Read the channel (Q-stop mode)
	R1(LSB) ~ R8(MSB)
N F(26) A(0~3):	Start all channel
N F(24) A(0~3):	Stop all channel
N F(8) A(0~3):	Test LAM
N F(9) A(0~3):	Clear LAM and start data acquisition
N F(10) A(0~3):	Clear LAM

CAMAC commands

LAM:	Look-At-Me can be enabled and disabled by using a jumper switch on the board.
Z or C:	Clear LAM on S2 and start data acquisition
I:	Not implemented

	X:	Generated when the module receives above functions.
	Q:	Q=1 when F(0) is sent, data is stored, F(8) is sent, and the LAM flip-flop is in the state of 1.
Case:		CAMAC single width
Power:		+6V 250mA
		-6V 3.5A
		total 22.5W

Circuit diagram and operation

See the figure 1.

The circuit consists of the front-end part including fast amplifiers, 8-bit fast ADCs, and fast memories, and the CAMAC interface part. The internal clock is 100MHz.
Data acquisition is invoked by Z, C or F(9). A stop signal should be provided prior to read out since data acquisition continues until the signal is provided.

	M							L	
	S							S	
Voltage at ADC input	B							B	Data Code
≧ 0V	1	1	1	1	1	1	1	1	
	1	0	0	0	0	0	0	0	Complementary Straight Binary
≦-2V	0	0	0	0	0	0	0	0	

Data in the memory is read from the earlier data by repeating the F(0) function. (FAST IN FAST OUT). After the read out cycle is repeated 1024 times, Q response will not be generated, then move to the next channel read out.
* There are variable registers for adjusting offset and amplification gain. Please adjust according the amplitude of the input signal so that the signal can be in the range of 0V~ -2V at the inputs of the ADCs.

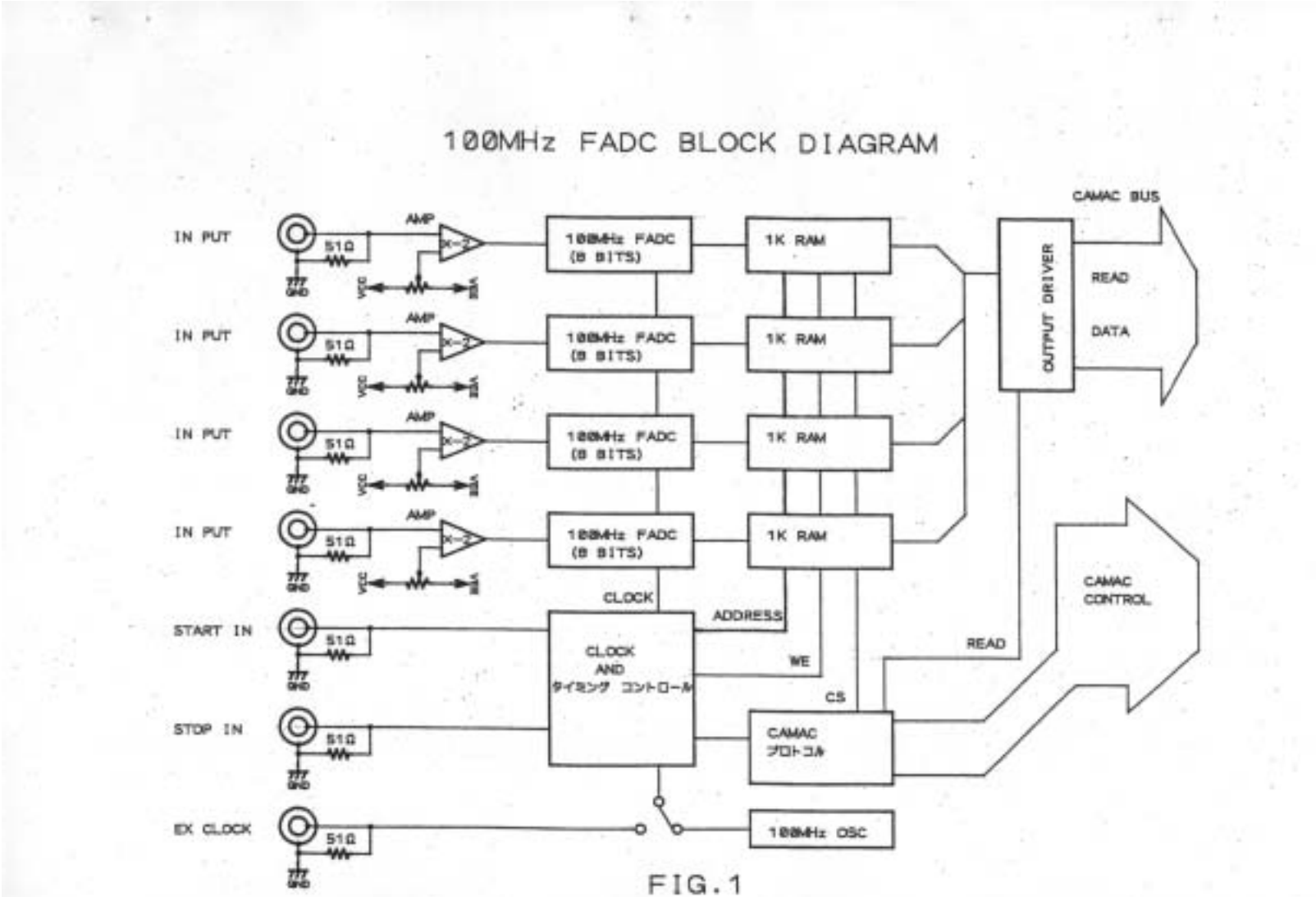
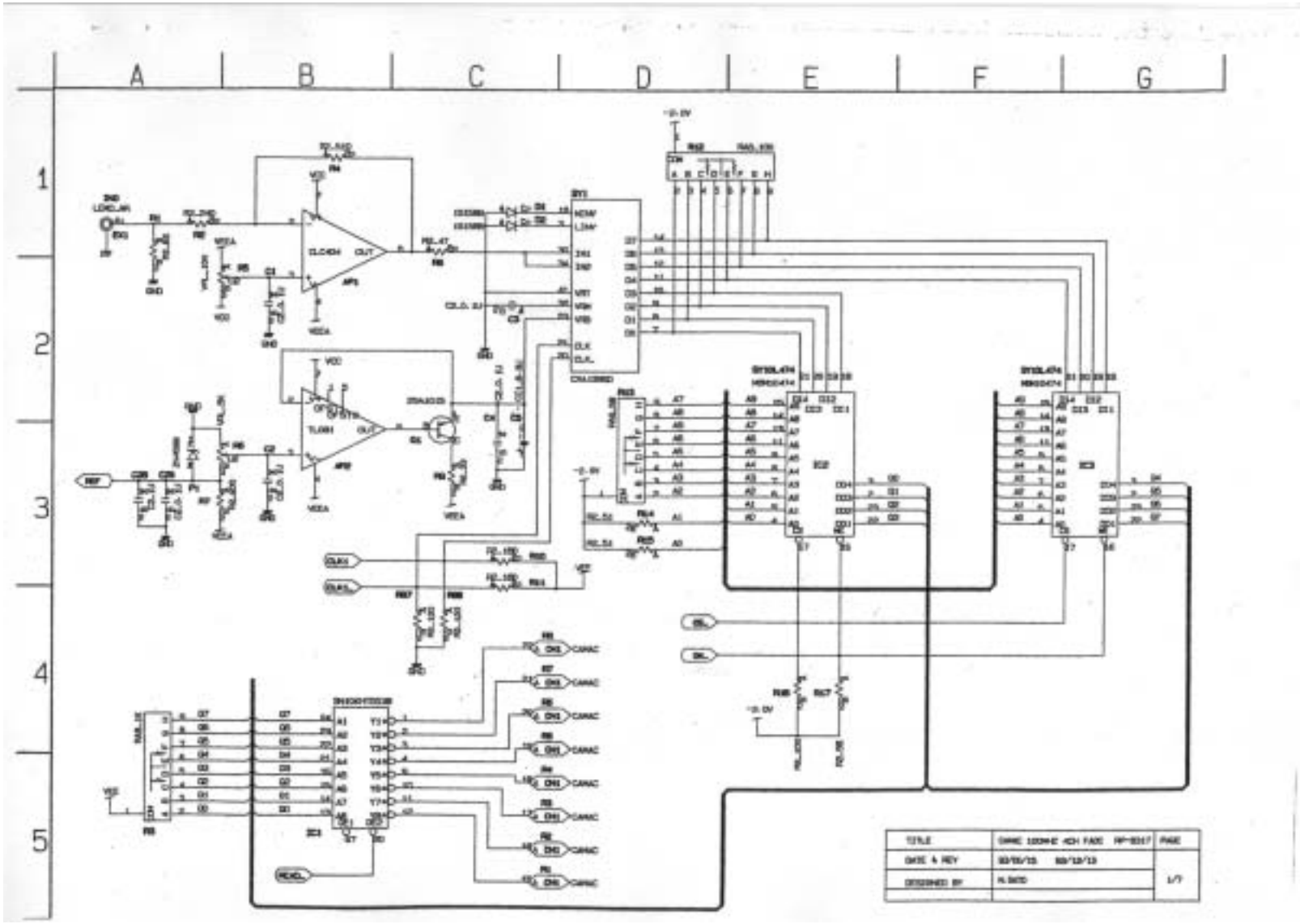

100MHz FADC BLOCK DIAGRAM
IN PUT
IN PUT
IN PUT
IN PUT
START IN
STOP IN
EX CLOCK
51Ω
AMP
VCC
VEE
100MHz FADC (8 BITS)
1K RAM
CLOCK
ADDRESS
WE
CS
CLOCK AND タイミング コントロール
CAMAC プロトコル
100MHz OSC
OUTPUT DRIVER
CAMAC BUS
READ
DATA
CAMAC CONTROL
READ

FIG.1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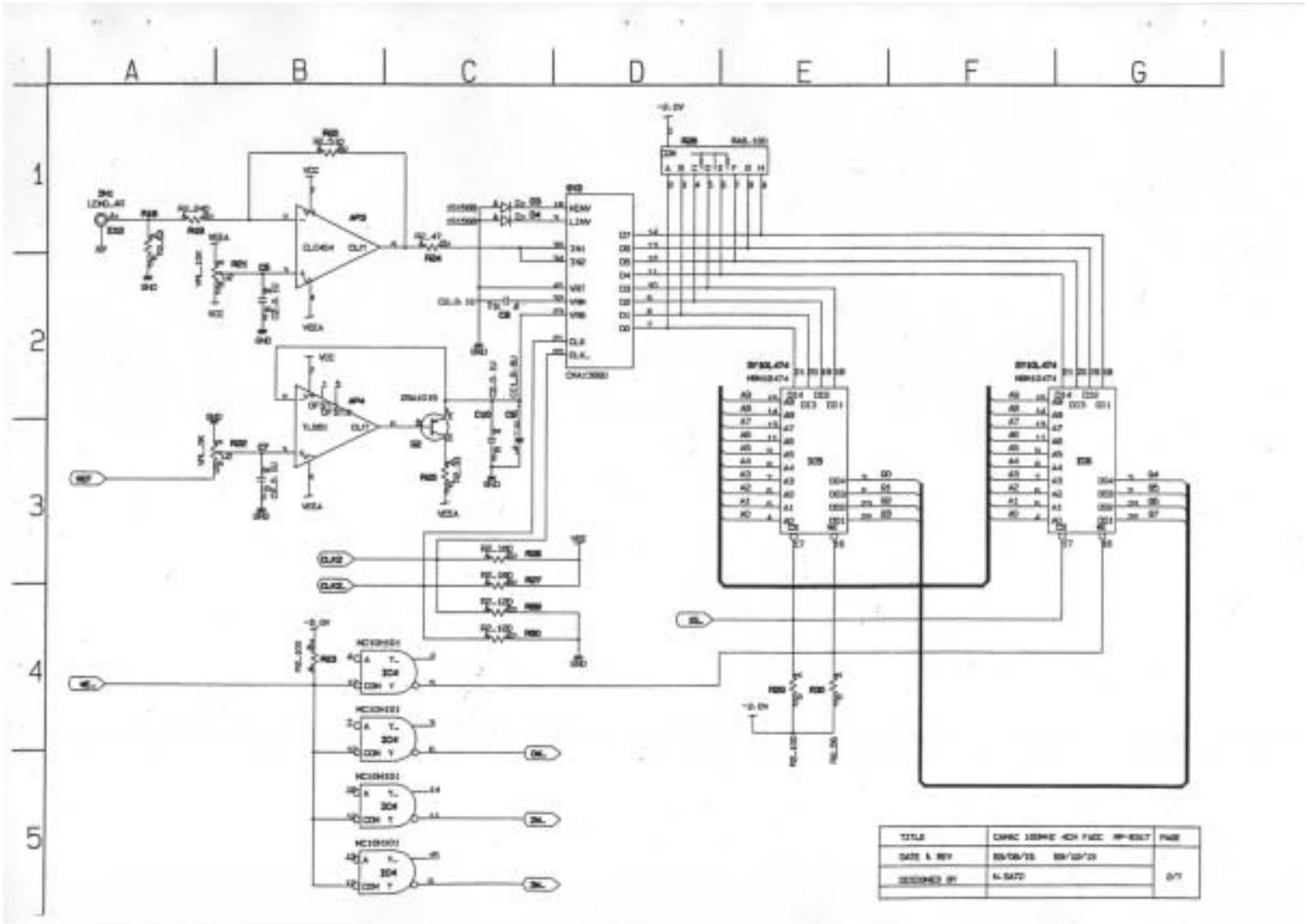
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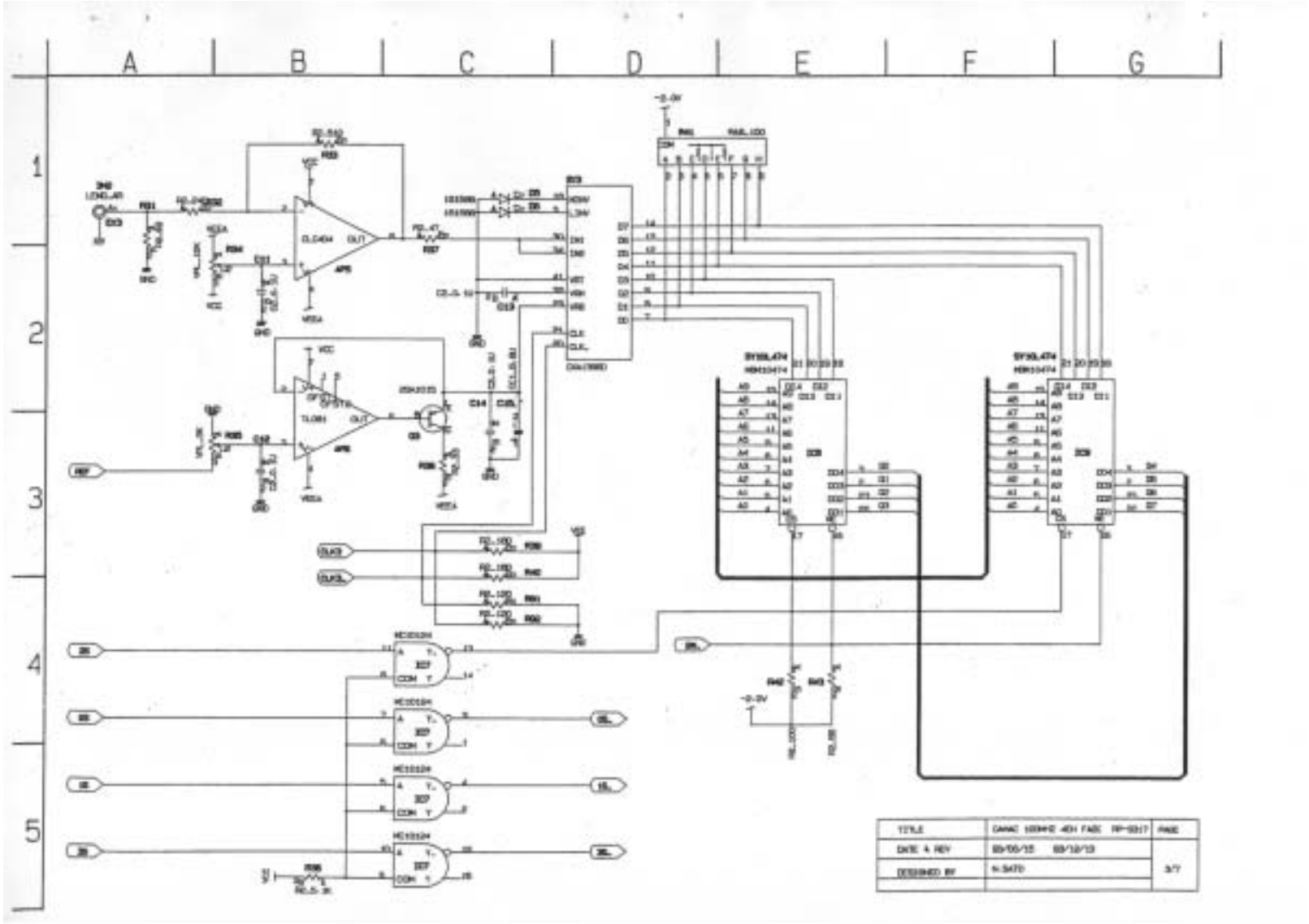
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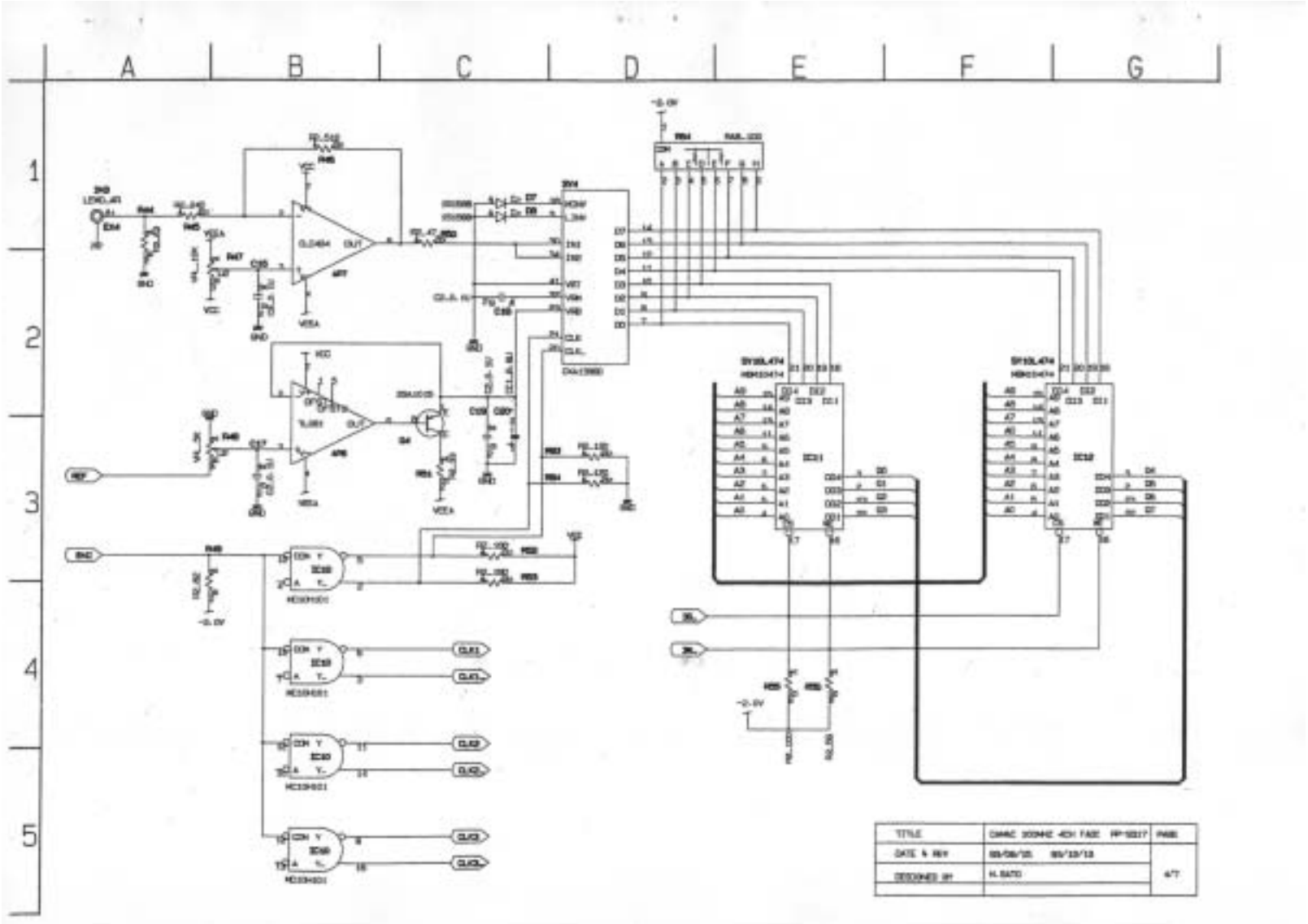
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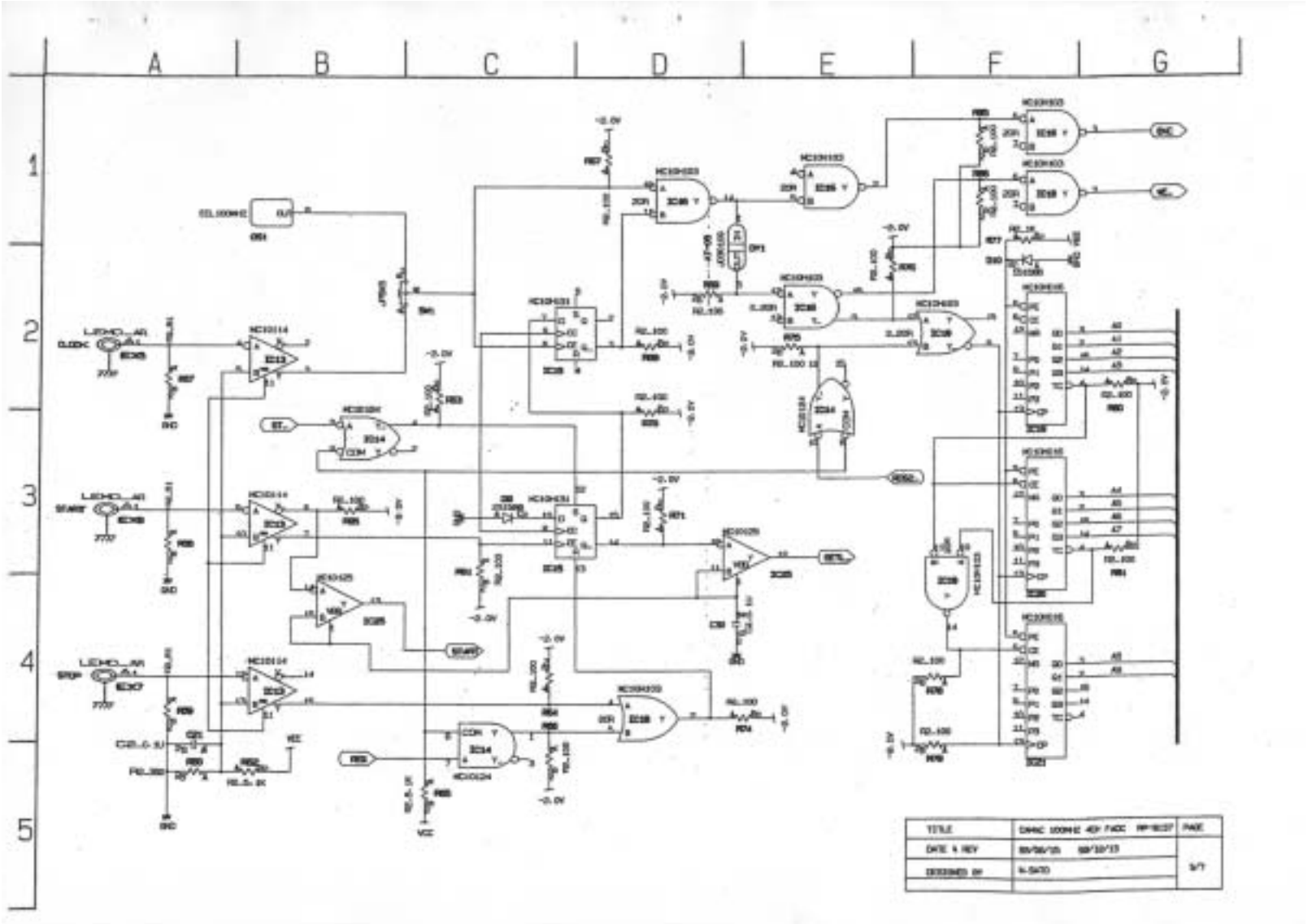
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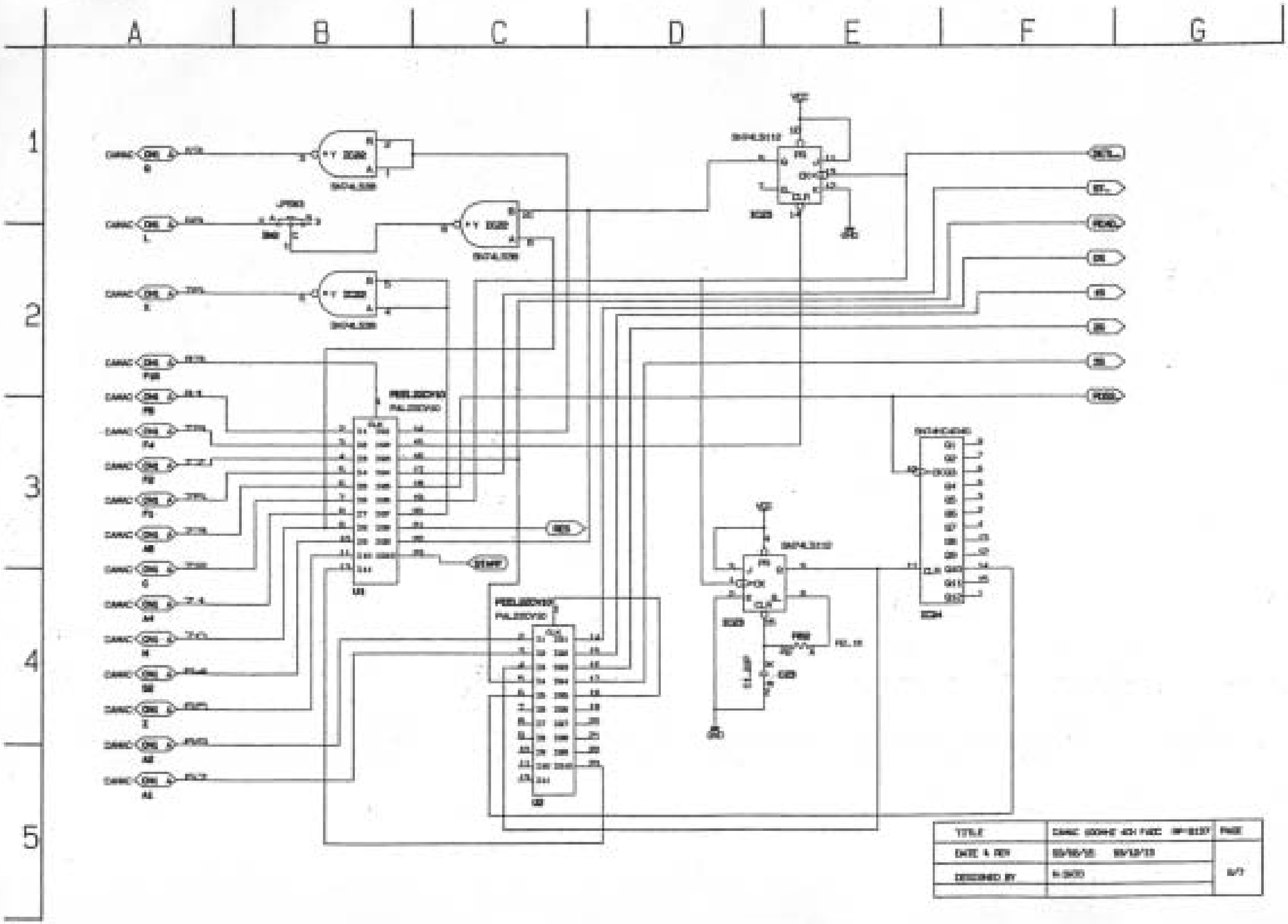

A
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SN74LS112
SN74LS08
START
VCC
GND
TITLE
DATE & REV
DESIGNED BY
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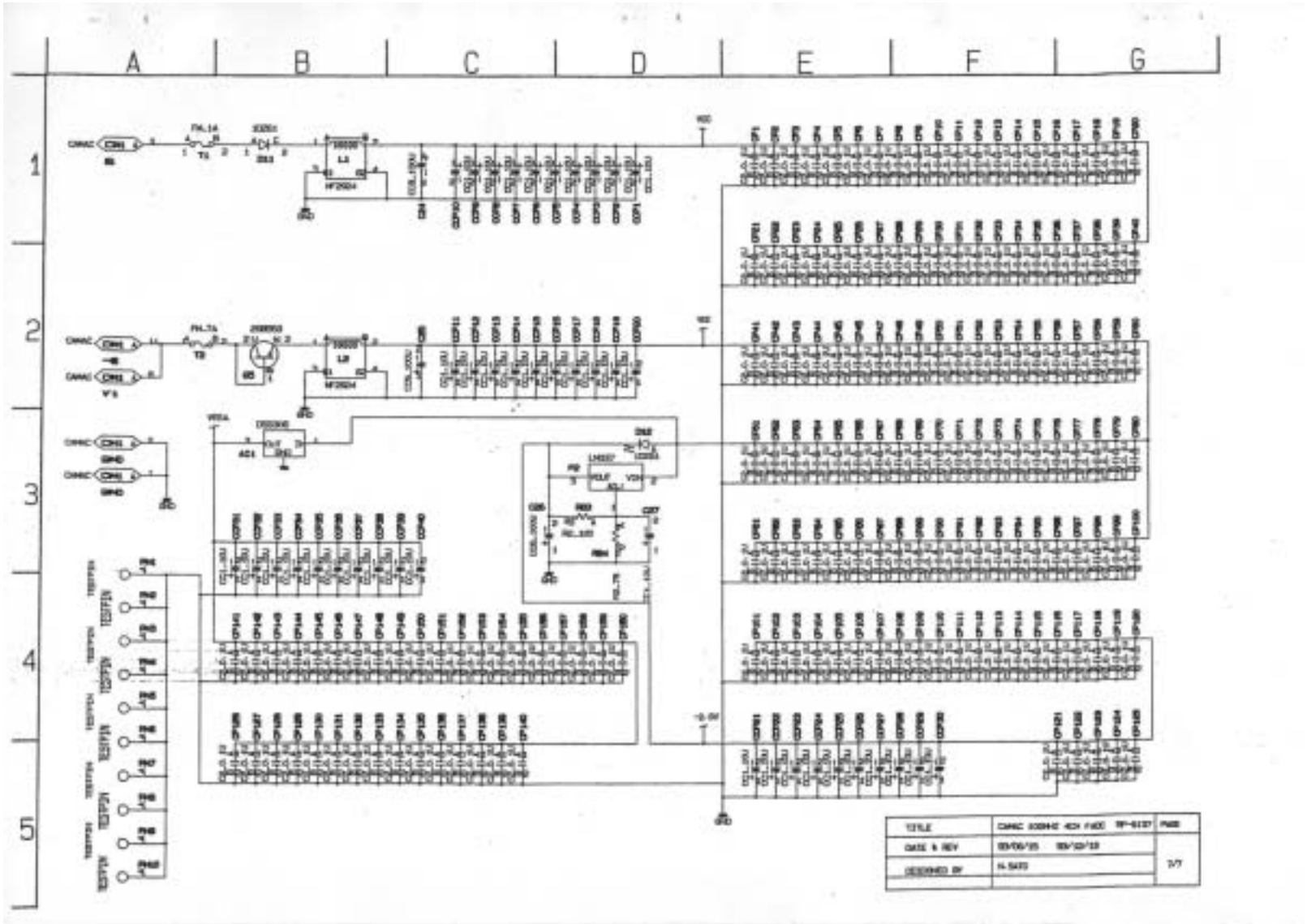
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