OPERATOR'S MANUAL

MODEL HV4032A

HIGH VOLTAGE SYSTEM

Revised
March, 1994

(FAN 2043)

A T T E N T I O N

THE PROM UPDATE SHEET IN THE REAR POCKET LISTS CHANGES WHICH HAVE BEEN MADE IN NEWER VERSION PROMS. THE INFORMATION IN THE TEXT OF THIS MANUAL HAS BEEN REVISED TO CORRESPOND TO "M" SERIES PROMS.

AC LINE POWER MUST BE OFF WHEN REMOVING OR INSTALLING HIGH VOLTAGE PODS (SEE SECTION 1.3).

CAUTION: IF THE GROUND AT THE LOAD HAS AN AC VOLTAGE DIFFERENCE WITH RESPECT TO THE CHASSIS GROUND, AN APPARENT OUTPUT VOLTAGE RIPPLE WILL RESULT IN THIS CASE, IT IS RECOMMENDED THAT THE GROUP CONTACT ON THE POWER CORD BE DISABLED.

CAUTION: FOR PROPER COMMUNICATION VIA THE DAISY CHAIN, ATTENTION MUST BE GIVEN TO VARIATION OF THE GROUND VOLTAGE CHASSIS-TO-CHASSIS. A $\leq$2 AC OR DC VOLTAGE DIFFERENCE BETWEEN ANY TWO CHASSIS IS LIKELY TO CAUSE COMMUNICATION ERRORS OR COMMUNICATION LOCK-UP. IF SUCH A VOLTAGE DIFFERENCE EXISTS, A POSSIBLE SOLUTION IS TO REMOVE THE GROUND CONTACT ON THE POWER CORD AND TO TIE THE CHASSIS TOGETHER. NOTE THAT THE 2132 INTERFACE MAY DIFFER IN GROUND POTENTIAL FROM THE HV4032 CHASSIS BY UP TO 100 V.

CAUTION: DO NOT RACK MOUNT UNIT VIA FRONT-PANEL SCREWS WITHOUT PROVIDING ADDITIONAL SUPPORT. (SEE SECTION 2.3).

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

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LeCroy offers a selection of customer support service. For example, Blue Ribbon service provides guaranteed three-day turn around on repairs, a direct access number for product application assistance, yearly calibration and the addition of engineering improvements. Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

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- Modify the software and/or merge it into another program for your use on a single machine.

- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

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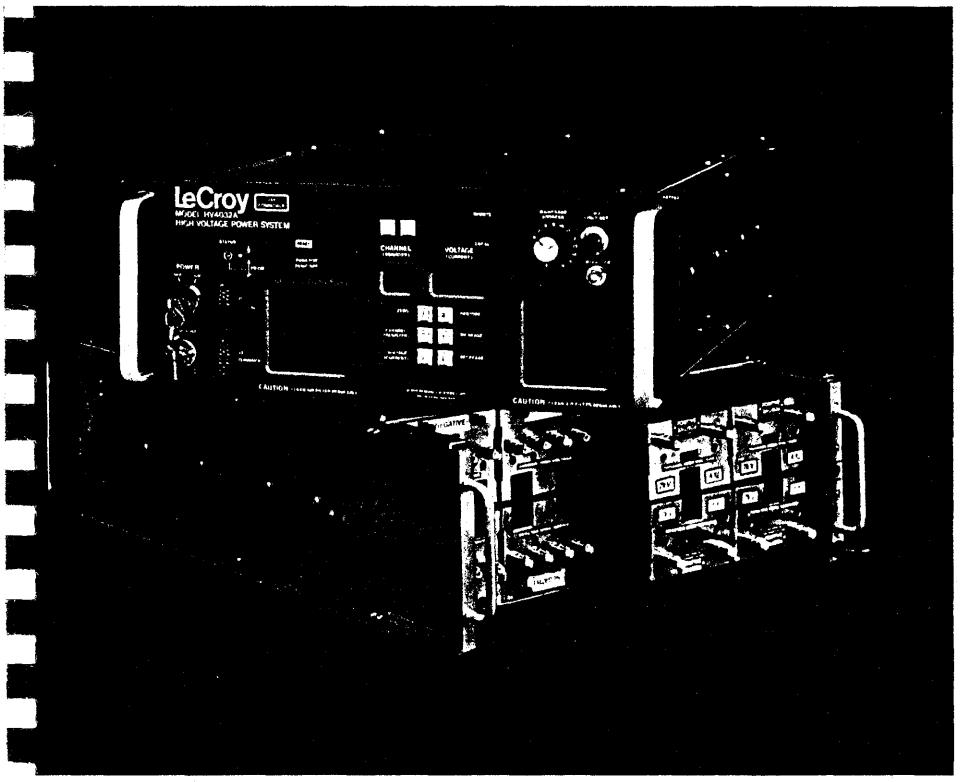
HIGH VOLTAGE SYSTEM
MULTIPLE CHANNEL, MEDIUM DENSITY

LeCroy

SYSTEM HV4032A
WITH LOCAL AND REMOTE CONTROL



- **Up to 32 Independent Channels per Mainframe**
- **Safety Interlocks, Trips, and Fault Reporting**
- **Local or Remote Control**
- **Multiple Mainframe Daisy-Chain Control**
- **Comprehensive Microprocessor Control and Monitor**

FOR PHOTOMULTIPLIER AND WIRE CHAMBER APPLICATIONS

The LeCroy HV4032A System is a modular, programmable, microprocessor controlled, High Voltage Power System for photomultiplier and wire chamber applications. Control and read-back for up to eight plug-in pods is provided by the HV4032A/M Mainframe. Plug-in pods are available for either polarity and for systems requiring up to either 3.3 kV or 7 kV (Series VII). Any combination of eight pods may be used in a single mainframe, and each kind of pod is automatically identified by the mainframe. Up to 32 individually controlled channels of High Voltage are housed in a single mainframe, depending upon the application. The mainframes themselves are programmed either locally with pushbutton controls and an LED display, or remotely. The latter is done with a daisy-chained link of up to 16 mainframes to either a computer terminal or a CAMAC interface for computer control and fault reporting.

FEATURES

Modular Construction – All four types of plug-in pods may be used simultaneously in a single mainframe. Pods are easily and quickly installed via rear-panel access, without dismounting the mainframe or removal of access panels. An internal dataway of the HV4032A/M allows pods to identify themselves.

Continuous Memory – High Voltage settings are stored in a battery backed-up memory, and can be recalled on demand. Battery backup, continuously recharged whenever AC power is available, protects the integrity of internal memory for 24 hours. This makes the memory immune to occasional power failures.

Digital Voltage Control – A 12-bit ADC reads the actual output voltage and compares the result to the demand (programmed) value. Deviations beyond the control range indicate channel failures. Failures result in system shutdown and are reported on the front panel and via any computer interface.

Thermal Protection – A temperature monitor on the internal power supply shuts off the high voltage in the event of overheating. This can be the result of excessive loading, a clogged fan filter, or high ambient temperatures.

CAMAC Programmability – All operations that can be performed from the front panel are available through the Model 2132 CAMAC (IEEE-583) Interface. Simple binary control words make programming the HV4032A/M easy. A unique RESPONSE feature may be enabled, indicating the completion of each command.

Current Limit/Trip – All 3.3 kV pod channels have fixed current limits. Series VII channels are limited separately in programmable 1 μA steps with $\pm(5\ \mu A + 5\%)$ accuracy. For Series VII pods only, a current trip crowbar action is initiated when surges are detected. This protects against detector damage from high voltage breakdown.

FUNCTIONAL DESCRIPTION

The HV4032A System consists of up to eight pods in each HV4032A/M Mainframe with provision for remote operation of all channels in up to 16 mainframes. A single LeCroy Model 2132 CAMAC (IEEE-583) Interface (Page 8) permits daisy chain control from gain control needed for practical operation of large systems. The system also provides total status outputs which allow for a remote HIGH VOLTAGE ON indicator, and a HIGH VOLTAGE FAULT alarm.

Each voltage channel employs a high-efficiency switching supply with low ripple and a safe, low stored-energy output stage. Channel output is controlled by a microprocessor in the mainframe which establishes demand settings, continuously measures the output voltage (using a 12-bit ADC), compares the output with the 12-bit programmed demand, and adjusts the output to maintain constant voltage. Any channel which cannot be brought into regulation, either due to overload or channel failure, is shut down and reported by the CPU.

Voltage run-up and run-down are performed at safe rates of 1 kV/sec for 3.3 kV channels and 2 kV/sec for Series VII channels. Series VII also allows for current-limited run-up at less than 2 kV/sec. Under current-limited conditions, the voltage run-up speed is set by the rate at which the load capacitance can be charged. Series VII has special algorithms to automatically allow for this mode.

The system is fail-safe against erroneous voltage or current-limit demands which occur in day-to-day programming. Series VII provides for setting individual hardwired voltage and current limits, using rear-panel terminals. This safeguard is in addition to the mainframe front-panel vernier which sets the system voltage limits. The vernier setting establishes the maximum demand voltage of the 3.3 kV pods and sets a Series VII limit at twice this value.

Numerous safeguards and error checking subroutines are included in the HV4032A/M microprogram. The memory stores all of the system parameters (demand voltages for each channel, current limits for Series VII channels, idle-down voltages for the system and the mainframe pod complement), and is safeguarded by battery back-up. The auto-rechargeable battery guards against memory loss due to power failures of up to 24 hours duration, and includes fail-safe self-checking of memory integrity at power up.

All pods voltages are programmable, and Series VII pods are also programmable for current limit, with separate settings for each channel in 1 μA steps. Each Series VII pod also has a fast current trip circuit, sensitive to current surges. All pods identify themselves to the CPU and may therefore be randomly placed in the

mainframe, without restriction. Placement of one or more Series VII pods in a mainframe activates special firmware to perform current limit and current monitor functions on those stations containing Series VII channels.

Series VII supplies include innovative load protection features. An extremely fast current surge detector allows each channel to initiate a trip sequence as soon as a fault is detected. Power supply output is stopped within 50 μsec of the sensing of the fault. This trip feature is the first step in the load protection sequence of Series VII. To fully protect the chamber, the energy stored in the HV cable and Series VII output filter capacitor must be dissipated. It is shunted to ground and discharged with a response time of typically less than 1 msec. Application of this crowbar protection is a first from LeCroy. Any and all Series VII channels (up to 16) can be ganged for common HV trip to prevent the potentially dangerous voltage imbalances which can result from the shutdown of only one channel. When configured as a daisy chain, the channel initiating the trip reports its action to the user.

For the unexpected, the HV4032A/M also includes a PANIC OFF, allowing all channels to be shut down in less than 20 msec (full load). Local PANIC OFF is accommodated via a large illuminated front-panel button, with remote activation via a front-panel INTERLOCK connector. The trip is reported in CAMAC or TTY mode operations.

Full digital control for all functions is provided locally via front-panel push-button and provided remotely via computer or TTY. Front-panel decimal displays identify the channel addressed for control, as well as the value of the parameter that is inserted. Channel numbers 0 through 31 identify a voltage channel. For 7 kV supplies, the odd numbered channels are omitted, and a "c" register is added to indicate current settings. Thus, with 7 kV pods in locations 1 and 2, and 3.3 kV pods in the remaining locations, the active channel numbers would be 0, 0c, 2, 2c, 4, 4c, 6, 6c, 8, 9 . . . Demand voltage for the selected channel is set via each of the Channel 0 through 31 registers (except those registers asssigned a current demand value, as just described). Preset registers have addresses which are larger than 31 and contain settings for groups of channels. Groups can be set to a common value defined by these registers for system initialization. This parallel load feature is active only when the HV is off.

TABLE 1

Preset Registers with Addresses and Functions

Address 33	3.3 kV Preset Register	Sets all 3.3 kV pods (negative and positive) to a common value. This is useful for system initialization. All channels can start out at a common value and then be trimmed individually as required. Resolution is ±1 V, with a channel-to-channel accuracy of ±(0.1% + 1.5 V). See example below.
Address 70	Series VII Preset Register	Sets all 7 kV pods (negative and positive) to a common value. Resolution is 2 V, with a channel-to-channel accuracy of ±(0.1% + 3 V).
Address 70c	Series VII Current Preset Register	Presets the current limit of all Series VII pods. Setting is made in 1 μA steps, with an accuracy of ±(5% + 5 μA).
Address 43	3.3 kV Idle-Down Register	Sets the idle down voltage for all 3.3 kV channels to this idle-down value.
Address 47	Series VII Idle-Down Register	Sets the idle-down voltage for all Series VII pods. It functions exactly as register 43, permitting all Series VII supplies to have their own common idle-down voltage.
Address 99	Diagnostic Register	Used for calibration and diagnosis, using procedures described in the manual.

Address 33
3.3 kV Preset Register

FRONT-PANEL FEATURES

1 STATUS OUTPUT

A front-panel Lemo output indicates HV present at rear connectors. This may be used for personnel safety interlocks or as an independent indicator.

2 PROGRAMMED RUN-UP/RUN-DOWN

A HV turn-on command initiates a ramp-up of all channels. The ramp rate is a safe 1 kV/sec for 3.3 kV supplies and 2 kV/sec for 7 kV supplies. A turn-off command ramps down similiarly. Series VII supplies (pods) also permit programmed current-limited run-up over the range of 10 to 500 μA, determined by the load capacitance, C, and the current limit i, ($dV/dt = i/C$).

3 ZERO (Z)/RESTORE (R)

Momentary pushbuttons. Depressing ZERO (Z) loads demand voltage of selected channel into a buffer, then loads a zero into the demand voltage register. A slow voltage run-down to <100 V (no load; <20 μA for personnel safety) is initiated for the selected channel. Depressing RESTORE (R) initiates slow run-up of selected channel previously ZERO'd, if HV is ON. Active only in LOCAL mode.

4 LOCAL/REMOTE

Front-panel slide switch selects LOCAL or REMOTE control of mainframe. In REMOTE control, the unit automatically distinguishes between ASCII characters from a TTY and binary words from the Model 2132 CAMAC Interface. TTY operation may run at either 110 or 300 baud (factory set at 300 baud) as set by a user-selected internal plug.

5 MAINFRAME ADDRESS

Each mainframe may be assigned an address between 1 and 16. This permits unambiguous addressing of mainframes that are daisy chained together for remote control. Special shorthand allows the addressing to be skipped after the first reference.

6 VOLTAGE LIMIT

Front-panel hardware voltage limit for all channels. The clamp point for 7 kV (Series VII) channels is twice that of the 3.3 kV channels. When a demand voltage exceeds the limit, the CPU detects a failure, zeroes the channel, and reports the shutdown. Series VII pods have a rear-panel current and voltage clamp for each channel.

7 INTELLIGENT ON/OFF

Upon loss of AC power, the ON/OFF switch position is stored in memory, as is a self-test pattern. When AC power is restored, the self-test pattern is checked for integrity. A successful self-test pattern check insures integrity of stored demand voltages and switch settings. If shutdown was by user switch-off, the Model HV4032A/M stands by. If shutdown resulted from a power failure at a time when the HV was on, a controlled voltage run-up is executed unless Series VII pods are present. If any stations have 7 kV pods, the system stands by.

8 INTELLIGENT DAISY CHAIN

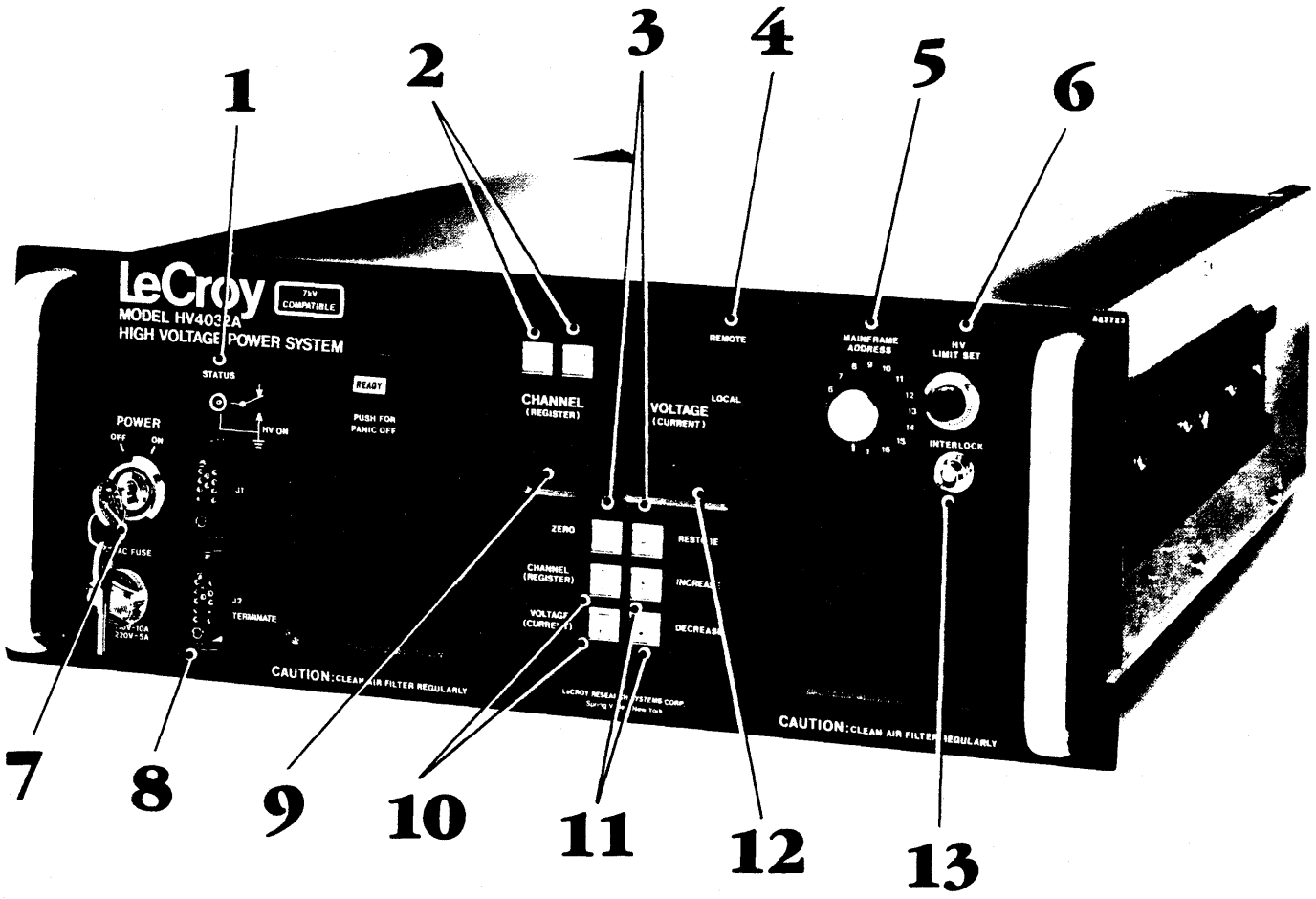
Up to 16 mainframes may be linked together with Serial Transmit, Receive, and Control bus lines. An identifier line allows the system to differentiate between CAMAC and TTY modes. This allows ASCII coding for TTY operation and binary coding for CAMAC control.

9 CHANNEL DISPLAY

LED display showing the channel selected corresponding to the Voltage (or current for Series VII pods) output or demand setting shown in the VOLTAGE display.

10 VOLTAGE (V)/CHANNEL (C)

Momentary pushbuttons enable a VOLTAGE or a CHANNEL to be changed by INCREASE or DECREASE switches. When V is depressed, the demand voltage of the selected channel is displayed. When V is released, the measured output is displayed. Active only in LOCAL mode. V is also used to set current limit for 7 kV pods.



11 INCREASE(↑)/DECREASE(↓)
Momentary pushbuttons increase (decrease) channel number if CHANNEL pushbutton is depressed simultaneously; or increase (decrease) voltage (or current for Series VII pods) of selected channel if VOLTAGE pushbutton is depressed. Internal software prohibits settings in excess of pod design.

12 VOLTAGE DISPLAY
LED display showing the measured output voltage or, when the V button is depressed, the demand voltage. The leftmost digit displays a "c" when an output current is displayed (Series VII pods only) instead of a voltage.

13 INTERLOCK
A front-panel BNC input accepts TTL levels, triggering a panic off. Internal jumper allows user assignment of logic levels, allowing the input to act as a fail-safe interlock or a remote panic off.

SPECIFICATIONS

GENERAL

Pods/Mainframe: Eight

I/O Connectors (J1 and J2): Two multipin connectors, with front-panel retainer, provide daisy chain capability. Five wire pairs interconnect the modules. Two pairs are 20 mA current loops (transmit and receive), two pairs are used for bus control and one pair mates with LeCroy Model HVCK-14. Differentiates between CAMAC and TTY remote operation.

Packaging: 19″ rack-mount chassis, 17″ × 28¼″ × 6⅝″. Side-panel slides facilitate internal access.

Voltage Required: 100-130 V, 60 Hz, or 205-260 V, 50 Hz (<750 W at full load). Selected by rear-panel switch.

Maximum Output: 208 W—all channels.

Operating Temperature: 5°C to 40°C.

Voltage Regulation: 0.05% line; ±0.5 V load.

Common Voltage Limit: Mainframe Front-Panel Control. 3.3 kV pods: V_{max} about ((.314 × S) + .2) kV. Series VII pods: V_{max} ((.628 × S) + .96) kV

HV Output Connector: SHV (Note 1).

Ambient Humidity: 0-90% relative humidity.

HIGH VOLTAGE PLUG-IN PODS

SERIES VII SAFETY

Current Surge Detector: One per channel. Responds to current surges of ⩾50 μA and a risetime <25 μsec. Initiates fast current trip and output crowbar.

Fast Current Trip: Shuts down supply with 50 μsec of surge detector output. Residual energy remains on output filter capacitance and cable until output crowbar is activated. Up to 32 channels may be ganged via rear-panel connector. Current trip by any one causes all to trip,

Output Crowbar: Discharges output filter capacitance and cable capacitance by a clamp to ground through 5 kΩ.

Crowbar Response Time: Typically <2 msec.

Manual Voltage Limit: One voltage-programmable rear-panel node per channel. Internally connected to + 15 V via 5.6 kΩ ±5% resistor. V_{max} = 0.8 V_{node} kV (Note 2).

Manual Current Limit: One voltage-programmable rear-panel node per channel. Internally connected to + 15 V via 4.3 kΩ ±5% resistor. I_{max} = 50 V_{node} μA (Note 2).

Pod Designation:	HV4032A1N & HV4032A1P	HV4032A7N & HV4032A7P
Channels/Mainframe:	32 maximum	16 maximum
Channels/Pod:	4	2
Voltage Output:		
for HV40☆☆A☆N	0 to − 3.3 kV (Note 3)	0 to − 7 kV (Note 4)
for HV40☆☆A☆P	0 to + 3.3 kV	0 to + 7 kV
Recommended range for rated performance	⩾±1 kV	⩾±1.5 kV
Current Output/Channel: (For rated performance)	2.5 mA maximum	500 μA maximum
Current Limit/Channel:	3 ±0.3 mA Fixed (Also limited by maximum power output. See below).	Programmable/channel 5 – 500 μA. ±(5% + 5 μA) at 25°C.
Current Limit Programming Step:	N/A	1 μA
Current Trip:	Limit only	Surges of ⩾100 μA in ⩽25 μsec (Response time typically 50 μsec)
Power Output:	6.5 W/channel maximum. Derate at 75 mW/°C above 30°C ambient.	3.5 W/channel maximum
Current Monitor:	No	1 per channel
Current Monitor Resolution:	—	1 μA
Voltage Monitor Resolution:	1 V	2 V
Programming Step:	1 V	2 V
Voltage Regulation:	0.05% line; ±0.5 V load	0.05% line; ±1 V load
Voltage Accuracy: (Channel-to-channel matching)	±(0.1% + 1.5 V) (In HV4032A/M mainframe at 25°C after 30 min. stabilization at a fixed demand voltage.)	±(0.1% + 3 V)
Ripple: (at rated load)	<25 mV RMS for <1 kHz Bandwidth <100 mV wideband (Note 5)	Typically 25 mV p-p <50 RMS wideband (Note 6)
Output Voltage Temperature Coefficient:	Typically 0.005%/°C at 2 kV <0.01%/°C (+ 45°C ambient).	Typically 0.005%/°C at 5 kV

Notes: 1. Kings type 1064-1 connectors available at extra cost on Series VII only. Specify HV4032A7N/200 or HV4032A7P/200.
2. V_{node} = voltage applied at voltage/current limit connector.
3. Minimum non-zero demand voltage is 80 V.
4. Minimum non-zero demand voltage is 160 V.
5. Digital regulation updates of ±250 mV DC ⩾250 msec apart.
6. Digital regulation updates of ±500 mV DC ⩾250 msec apart.

ORDERING INFORMATION

For any configuration, including fewer than eight pods, order the HV4032A/M Mainframe and up to eight pods, which may be mixed in any combination of the four models shown in the table on page 3. Although a mainframe may hold eight pods, any number from one to eight may be installed.

INTERFACE

To interface up to 16 mainframes to the CAMAC control system, order one Model 2132 CAMAC Interface and the appropriate cables as described below. Larger systems require one additional Model 2132 CAMAC Interface for each 16 additional mainframes.

HARDWIRED VOLTAGE AND CURRENT LIMIT FIXTURE

Model HV4032A7X is an optional plug-in board with four trimpots used to set the voltage and current limits for the two channels in a pod. Order one board per Series VII pod if this feature is desired.

EXTERNAL TRIP CIRCUIT CONNECTOR

Commoning of surge detector trip circuits requires that all channels which must crowbar together be linked through external wiring. Connection diagrams, supplied with the mainframe, require use of an AMP 87456-7 twelve-contact housing (with inserts) for each Series VII pod.

NOTE

On units received before May 1, 1981 an HVUK upgrade kit is required for Series VII features. User-installation time is less than 30 minutes.

MODEL 2132 CAMAC INTERFACE

Model 2132 is a single-width CAMAC Interface designed for use with up to 16 of the Model HV4032A's in a daisy chain. The unit is also compatible with the Models HV4032 and HV4032P. The unit offers 40 words of buffering on both input and output. The 2132 employs two interrupt registers, L_1 and L_2. One is designed to offer a CAMAC LAM upon non-routine phenomena such as channel failures, whereas the other is used for routine responses. Control words and responses employ a simple binary code. A control line is employed to identify the controller in use as either Model 2132 or a TTY.

ACCESSORIES

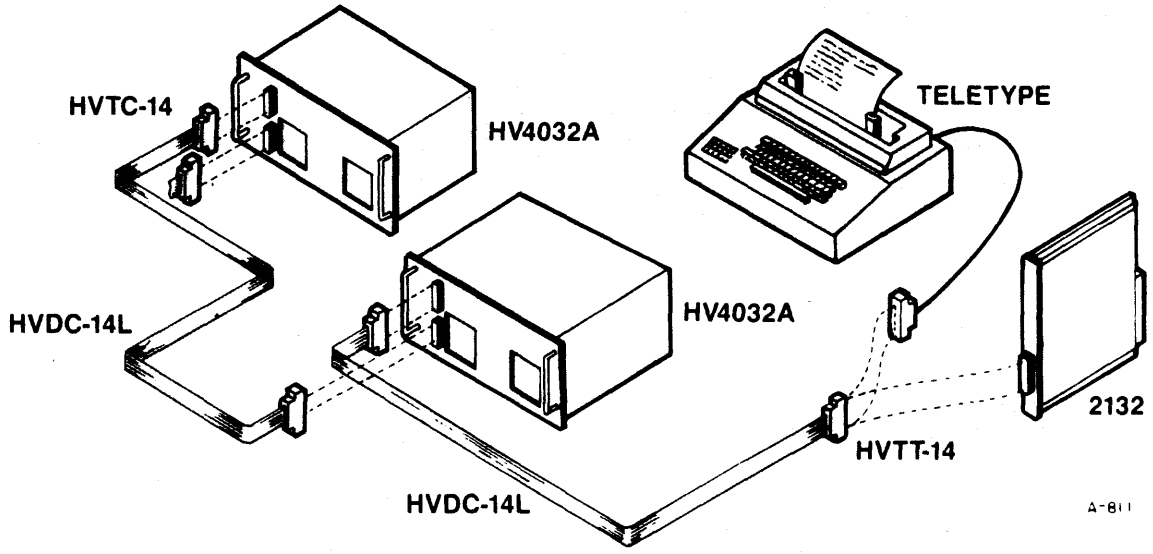
Model HVDC-14L— A data cable used to connect HV4032A chassis to one another or to the Model 2132. Includes one LeCroy HVCK-14 connector at each end. The length in feet, L, must be specified.

Model HVTC-14— A terminator for the HV4032A daisy chain. One employed at the end opposite the controller (CAMAC or TTY). One required per daisy chain.

Model HVTT-14— Consists of all the parts required to connect a HV4032A daisy chain to a teletype. The HVTT-14 consists of mating connector to the HVCK-14 with a pair of pigtails to be connected to the teletype.

Model HVCK-14A— Connector kit to mate with the HV4032A front-panel daisy chain connectors.

Model HVAK— Adapter kit to allow change of retention hardware to mate with HV4032A system connector.



Programmable High Voltage

Large Systems

Series 1440—The most economical, yet the most rugged programmable multichannel supply available.

- Up to 256 HV outputs/mainframe
- All outputs independently controllable
- ±2.5 kV, 2.5 mA/channel
- RS232 or CAMAC (IEEE 583) control
- Industrial grade—field proven reliability
- Utilizes 16-channel plug-in cards

Medium Systems

Series HV4032A—Offers four different supplies which may be used simultaneously and controlled in the same mainframe. Offers exclusive HV protection features and convenient controls.

- Up to 32 HV outputs/mainframe
- All outputs independently controllable
- ±3.3 kV, 2.5 mA/channel
- ±7 kV, 0.5 mA with programmable current limit/crowbar
- RS232 or CAMAC (IEEE 583) control
- Utilizes 2 and 4-channel plug-in pods

Small Systems

Model 2415—Designed for use in CAMAC-Standard (IEEE 583) modular systems. Allows convenient remote control of your entire setup.

- One HV output module
- CAMAC-programmable control or manual operation
- Up to ±7 kV at 1 mA
- Up to ±3.5 kV at 2.5 mA
- Voltage and current monitor
- Programmable current limit and voltage

...to simplify your setup, stabilize your system, and eliminate the margin for error

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SECTION 1

SPECIFICATIONS

1.2 Introduction

The Model HV4032A is a complete high voltage system providing up to 32 independently programmable channels. The mainframe, Model HV4032A/M, accepts eight plug-in multichannel pods, Models HV4032A1N, HV4032A1P, HV4016A1N, HV4016A1P, HV4032A7N, and HV4032A7P. The HV4032A7 pods are called "Series VII." The HV4032A/M contains a microprocessor which provides the facility for both manual or remote control via TTY or the LeCroy Model 2132 CAMAC Interface.

Up to eight pods of six different types may be simultaneously employed in the HV4032A/M. The HV4032A1N and HV4032A1P each provide four channels of up to 3.3 kV at up to 2.5 mA. The HV4016A1N AND HV4016A1P each provide two channels of up to 3.3 kV at up to 5 mA. The HV4032A7N and HV4032A7P each provide two channels of up to 7 kV. The N and P suffixes denote negative and positive polarity.

The set voltage for each channel is stored in the microprocessor's memory. These demand voltages may be retained for up to 24 hours without AC power by the battery backup provided for the memory. Data will not be lost if power is turned off. On restoration of AC power, the microprocessor checks the memory for specific bit patterns. If the patterns are incorrect, all stored data are erased and must be re-entered by the user. If the memory bit patterns are verified the microprocessor examines the mainframe pod complement for Series VII and 3.3 kV style pods. All channels that have the same pod type are left as originally stored. Channels with a changed pod type are set to zero.

Monitoring of the high voltage outputs is done by a 32 channel multiplexed ADC. The microprocessor uses the ADC data to regulate the HV outputs and displays these readings on the front panel Voltage Display. They are also available to a remote control device.

The Models HV4032 and HV4032A mainframes are compatible and can be mixed in a control daisy-chain. Certain precautions must be observed. In addition, newer versions ("7 kV Compatible") of the HV4032A containing version "K" firmware offer additional features and require some cautions in a mixed daisy-chain. For details, see Sections 3.7 and 7.3.

1.3 Front Panel Controls

POWER ON:

The POWER ON key switch controls the line power to the HV4032A/M.

ZERO/RESTORE:

These two buttons allow alternate states to be accessed. Specific meanings depend on the CHANNEL(register) being displayed. The voltage setting of an HV channel may be zeroed using the ZERO button. The RESTORE operation is the complement of ZERO and has the general meaning of return to normal. For HV channels the RESTORE operation returns the voltage to its original value. Note that a ZERO operation on a Series VII current channel actually ZEROs the associated voltage channel. ZERO/RESTORE operations have no effect on the values stored in Registers 33, 70 or 70. Registers 33 and 70 may be used to ZERO or RESTORE all 3.3 or 7 kV pods respectively.

CHANNEL(register)/
VOLTAGE(current) and
INCREASE/DECREASE:

These buttons are used in conjunction with the CHANNEL(register) and VOLTAGE(current) displays. INCREASE and DECREASE functions act upon whichever parameter button, CHANNEL or VOLTAGE, is depressed. Two buttons must be used together in order to achieve a change. For HV4032A7N and HV4032A7P (Series VII) pods, voltage display programming on the corresponding current subchannel is also used to set the current limit.

Release of the VOLTAGE button loads a digital buffer memory for the indicated channel with the displayed value. When the VOLTAGE button is depressed, the demand for the indicated channel is displayed. Otherwise, the actual channel output is shown. It should be remembered that the current demand values are limits and actual output current will be determined by voltage and load.

If the supplies are turned on, and the user modifies the setting of a channel, the output voltage will not change until the user releases the VOLTAGE button.

HV ON and HV OFF: Used to turn the high voltage ON and OFF. The high voltage outputs will change at the standard rate of 1 kV/sec for the HV4032A1 and HV4016A1 Series pods or 2 kV/sec for Series VII pods. Slower runup rates may be programmed via the Diagnostic Register (see section 3.1). Series VII pods may achieve a slower runup if connected to a capacitive load programmed for a low current limit. All channels change simultaneously. Unlike other front panel controls which may be ignored if the microprocessor is still responding to an earlier command, the front panel HV ON and HV OFF request is always responded to immediately or when the previous operation is completed.

PANIC OFF: Front-panel momentary pushbutton unconditionally disables all channels. Integral with HV ON and READY indicators. This trip condition is reported to Model 2132 or TTY in remote operation. An HV ON may be initiated after the READY indicator is turned on.

INTERLOCK: TTL compatible input with internal 4.7 K Ω pull-up resistor. Negative edge triggers a PANIC OFF. While the INTERLOCK is low, the READY indicator is extinguished and all commands will be ignored. Internal jumper option complements the disabling state of the INTERLOCK. Trip is reported in the REMOTE mode.

STATUS: Front-panel Lemo connector. Clamp-to-ground when HV is present at rear connectors. Sinks $\geq$35 mA; up to 32 mainframes may be daisy-chained.

MAINFRAME ADDRESS: The setting of this switch establishes the address of the mainframe. It is relevant only in the remote mode. Valid addresses are 1 to 16. If only one HV4032A mainframe is employed, its address must be 16. For more than one, the last one in the daisy chain must be address 16. This is necessary for priority control of the serial data bus. The HV4032 employed address 63 for this purpose.

Both models may be mixed if proper last module addressing is employed. Both 16 and 63 may not be present in the same daisy-chain. Note that the MAINFRAME ADDRESS may

be changed at any time; however, the older HV4032 recognized address changes only on AC power up.

J1/J2 CONNECTORS:
(Serial Port)

These connectors provide for daisy-chaining up to 16 HV4032 and HV4032A units in a system. See the interconnection wiring diagram, Figure 3.1. The HVDC-14 data cable provides the necessary connections.

HV LIMIT SET:

A 10-turn potentiometer providing a hardware limit to the output of all channels. (The limit is adjusted by first setting a channel to the desired maximum, adjusting until the display just begins to indicate a decrease, and backing off slightly). Limit for Series VII channels is approximately twice that of 3.3 KV channels.

REMOTE/LOCAL:

This switch selects operation either from the front panel in LOCAL mode or from the TTY or 2132 CAMAC Interface in REMOTE mode. The Model 2132A CAMAC Interface (available August, 1981) may also be used. It provides identical features to the Model 2132 but allows for control of future LeCroy products. An in-progress command sequence is always completed by the mainframe before recognizing a mode change request. If a remote command sequence has been started but not completed just before a change to local mode, the mainframe will wait about one minute before aborting the remote command and recognizing the local mode controls.

FUSE INDICATOR:

Illuminated to indicate blown fuse. (Replace with 3AG SLO BLO type. 5A for 220 V operation, 10A for 110 V.)

FANS:

Two high power fans provide airflow through the HV4032A and guarantee cool operation of the multi-channel pods. Serviceable air cleaners are provided to prevent an accumulation of dust inside the mainframe.

These filters should be cleaned whenever they become visibly dirty. The filter is easily pulled out of its holder. Clean the filter by tapping it against a hard surface. Twice yearly, or when convenient, washing with mild soap and water is recommended. The filter should be dry before reinstallation. If the air filters become

clogged with dirt, a thermal overload will occur. This will result in a shutdown which will automatically be reported.

1.4 Rear Panel Description

HV SUPPLY: The HV4032A may employ up to eight multichannel high voltage power supplies (pods). These may be removed (see figure 1.2) by pulling the two quick disconnect fasteners and sliding the pod out.

WARNING: AC line power must be off when removing or installing pods. To install a pod, verify that the plungers of the fasteners are withdrawn before guiding pod into place. Push the plungers in to secure the pod.

NUMBERING SEQUENCE: Channels are numbered from 0 to 31 in the clockwise direction (facing rear of unit) with channel 0 at the upper left hand corner. For two channel supplies, odd addresses are suppressed. See figure 1.2.

POWER SELECT: A 110/220 V selector is located behind a round inspection hole on the right side of the rear panel.

1.5 Options

The HV4032A is a 32 channel high voltage power supply designed to supply 2.5 mA (average) per channel (200 watts total). Each channel can be voltage programmed over the range -100 V to -3300 V in 1 V steps. It consists of one HV4032A/M with eight HV4032A1N pods.

The HV4032A/M is a mainframe exclusive of plug-in pods. By purchasing the mainframe and pods separately, the system can be configured to diverse user requirements.

Pods - The two- and four-channel supplies used with the HV4032A/M.

Model HV4032A1N	-100 V to -3.3 kV; 2.5 mA/channel
Model HV4032A1P	+100 V to +3.3 kV; 2.5 mA/channel
Model HV4016A1N	-100 V to -3.3 kV; 5.0 mA/channel (discontinued)
Model HV4016A1P	+100 V to +3.3 kV; 5.0 mA/channel (discontinued)
Model HV4032A7N	-160 V to -7 kV; 500 µA/channel, with programmable current limit and a trip/crowbar safety feature.
Model HV4032A7P	+160 V to +7 kV; 500 µA/channel, with programmable current limit and a trip/crowbar safety feature.

Accessories

Model HV4032A7X is a plug-in module to the External Controls Header of the Series VII pods. Multiturn potentiometers are installed to allow setting of the hardware voltage and current limit for each channel while still providing access to the trip circuit control lines.

Model HVDC-14L	A data cable used to connect HV4032A chassis to one another or to the Model 2132. Includes one LeCroy HVCK-14 connector at each end. The length in feet, L, must be specified.
Model HVTC-14	A terminator for the HV4032A daisy-chain employed at the end opposite the controller (CAMAC or TTY). One required per daisy-chain.
Model HVTT-14	Consists of all the parts required to connect an HV4032A daisy-chain to a teletype. The HVTT-14 consists of the mating connector to the HVCK-14 with a pair of pigtails to be connected to the teletype.
Model HVCK-14A	Connector kit to mate with the HV4032A front-panel daisy-chain connectors.
Model HVJS	Adapter kit to allow change of retention hardware to mate with HV4032 system connector.
Model HVAK	Adapter cable to allow HV4032 family data cable

components to mate with an HV4032A front-panel connector.

Model HVUK	HV upgrade kit. Upgrades a non 7 kV compatible HV4032A to 7 kV compatibility.
Model 1534	Pod Extender.
Model 1535	Pod Tester. Used with 1534 and HV4032A mainframe. Provides buffering at mainframe voltages and signals to pod under test and allows manual control of outputs.

1.6 Absolute Calibration

In applications which stress precision high voltage, good channel-to-channel accuracy is required. The specification on page 7 of the technical data sheets shows a channel-to-channel voltage matching accuracy of ($\pm$0.1% + 3 V) for 7 kV pods. This means that the user may depend upon a reproducable voltage when moving a load to a different pod or another mainframe.

Since the beginning of production on the HV4032, LeCroy has used a particular high voltage divider to test the absolute accuracy of all devices used for the production and servicing of HV4032 and HV4032A units. This has insured consistency in testing and calibration. A high precision test of the LeCroy voltage scale to that of the U.S. National Bureau of Standards was made in 1982. The result was

1 NBS Volt = 1.0014 LRS Reference Volts

A change in voltage standards by LeCroy would be a disservice to previous customers since it would introduce a channel-to-channel inaccuracy of .14% between new units and old ones. Therefore LeCroy continues to use the same voltage reference. Any user requiring high absolute accuracy may use the equation above to compute the voltage output. Thus a setting of 7000 counts for a 7 kV pod actually corresponds to an output of 7000 (1/1.0014) = 6990 V. From the channel-to-channel accuracy specification, the user may be assured that any pod at this setting will produce an actual output of 6990 ($\pm$.1% + 3 V) = 6990 $\pm$ 10 V.

SECTION 2

INSTALLATION

2.1 Inspection

Upon receipt of the HV4032A it is recommended that a careful inspection be performed to insure that no damage occurred during transit.

The shipping box has been custom designed for this unit and should be saved should shipping be necessary.

After removal from the box, the unit should be examined for physical damage to the chassis and front panel.

Actuate the switches without power to assure physical integrity. Inspect the rear panel and be sure all HV pods are locked in their proper positions.

2.2 Power Requirements

The HV4032A has been designed to operate on 100-130 V AC, 57-63 Hz, or 205-260 V AC, 47-53 Hz. A 110/220 V selector switch is located on the right rear panel of the unit and may be accessed through a round inspection hole. The UP position will select the 110 V range, DOWN selects 220 V.

Should replacement of the line cord be necessary, a standard IEC cord may be locally purchased.

2.3 Rack Mounting Instructions

Do not rack mount unit via front panel screws without providing additional support.

Rack Mounting requires the use of drawer slides which are provided on a shelf.

Holes in the HV4032A Front Panel are provided to prevent the unit from sliding out of the rack.

Physical damage caused by cantilever mounting the HV4032A will void the warranty.

2.4 Instrument Checkout and Tutorial

Switch power on. The ready lamp should be lit. Set the LOCAL/REMOTE switch to the Local position.

A display of 33 1500 or 70 3000

indicates that the memory backup battery is discharged. This is considered normal on a new unit.

Push the VOLTAGE button. This either causes the loading of a demand value of 1500 V for all 3.3 kV channels or loading 3000 V for all Series VII channels.

A display of 00 00XX

indicates that the batteries are still partially charged and that the memory contents from previous use are preserved.

The following steps access and test service registers as follows:

Register 99 - Diagnostic register. Used to enable the mainframe for diagnostics and to allow entry of otherwise illegal demand values. Voltage programming selects optional HV run up rates.

Register 70c - Current Limit Preset Register. Used to commonly load a current-limit demand value for all mainframe pod stations containing Series VII pods. Display is possible only if one or more Series VII pods is installed. Values displayed are in units of μA. Valid only if HV is OFF.

Register 70 - Series VII Voltage Demand Preset Register. Used to commonly load a voltage demand value for all mainframe pod stations containing Series VII pods. Display is possible only if one or more Series VII pods is installed. Values displayed are in units of volts. Preset valid only if HV is OFF. A RESTORE operation on register 70 restores all failed, tripped* or ZEROed Series VII channels. ZEROing register 70 will zero all 7 kV pods. They can subsequently be simultaneously RESTORED through this register if desired. If the user desires to keep the output of a channel at 0 when using register 70 RESTORE, the demand voltage should be set to 0.

***Note** that a HV turn off or a Reset signal applied to the Series VII External Controls Header is necessary to clear the "Trip" status before a RESTORE will be effective.

Register 47 - Series VII Idle-Down Register. Used to commonly change all Series VII demand voltages while retaining the original demands in memory for use upon exiting idle-down mode. Display is in units of volts.

Register 43 - 3.3 kV Idle-Down Register. Similar to Register 47.

Register 33 - 3.3 kV Voltage Demand Preset Register. Similar to Register 70. Display is possible if one or more HV4016A1- or HV4032A1-Series pods are installed or

if an HV pod slot is empty. All 3.3 kV pods may be preset, ZEROed or RESTORED using this register.

Using the CHANNEL (register) button in conjunction with the INCREASE and DECREASE buttons, select all of the registers indicated above for the pod complement installed. Note: empty pod stations are treated as 3.3 kV pod stations.

Select Register 99. Depress the ZERO button. A "u" will flash in the most significant digit of the VOLTAGE(current) display. This indicates that the Diagnostic Mode has been selected. Depress the RESTORE button, returning the set to the normal mode.

Select each of the active Preset Registers. Using the VOLTAGE(current) button in conjunction with the INCREASE or DECREASE buttons; set desired preset values. Note that, upon power up, voltage default values are displayed, however, they are not loaded into the corresponding demand registers. To load default values, depress the VOLTAGE(current) button.

Select the active Idle-Down Register(s). Load the desired Idle-Down value(s). Selecting an Idle-Down value of 0 V defeats the feature for the register loaded with 0 V. Depress the ZERO button. A "ɔ" will flash in the most significant digit of the VOLTAGE (current) display. This indicates that the Idle-Down mode has been entered. Depress the RESTORE button, returning the set to normal mode.

For the purpose of the tutorial, set the display to an active voltage channel.

Set the HV Limit potentiometer to full clockwise (10.0) and switch HV ON by pushing the HV ON button.

The voltage display should blank out for approximately 10 seconds and return to the programmed demand value for the channel selected.

The HV ON light should come on immediately. When display returns, all channels should be at their DEMAND values. If the mainframe contains empty pod stations, they will report as failed (voltage display shows "9999").

Employing the CHANNEL INCREASE and DECREASE buttons to select channels 0 through 31, all channels should indicate an output voltage equal to the programmed demand. Series VII current channels (displayed with lower case c in the most significant digit of the voltage display) will show the current drawn by any load connected to the output. If no load is connected, a reading of c00X will be shown. Here, X is the offset current, typically 0.

Select one 3.3 kV channel and increase to 3300 V using the CHANNEL, VOLTAGE, INCREASE and DECREASE buttons. Upon releasing the VOLTAGE button, the display should blank for several seconds and then indicate 3300 V.

Select one 7 kV channel and increment to 7000 V using the CHANNEL, VOLTAGE, INCREASE, and DECREASE buttons. Upon releasing the VOLTAGE buttons, the display should go blank for several seconds and then indicate 7000 V.

Select the Diagnostic Mode by displaying register 99 and depressing the ZERO button. Display a Voltage Channel. Slowly rotate the HV LIMIT SET potentiometer counter-clockwise to cause a decrease in the Voltage Display of more than 64 V (128 V if a Series VII pod is being limited).

Return the display to Register 99. Depress RESTORE in order to return to the Normal Mode. The system will now recognize voltage errors and report them as failed channels, setting their Demand Voltage to zero and indicating 9999 in the VOLTAGE(current) display.

Return the HV LIMIT SET potentiometer to the full clockwise setting of 10.0 and push RESTORE button. The indicated channel should return to its previously set voltage value.

Push the PANIC OFF switch. Note that the READY light is momentarily extinguished followed by the HV ON light. The READY light comes back on after HV is turned off, indicating the unit is again ready to respond to commands.

Turn the HV ON again. Short the HV INTERLOCK BNC. A 50 Ω terminator may be used for this purpose. The response should be identical to pushing the HV PANIC OFF button.

SECTION 3

OPERATING INSTRUCTIONS

3.1 Local Mode

With the LOCAL/REMOTE switch in LOCAL, the HV4032A will respond to the front panel switches and not to the Serial Port. Front panel operations to which the unit can respond are:

HV ON
HV OFF
Set Voltage Demand - each channel
Set Current Limit - Series VII (7 kV channels) only
Display Demand Voltage
Display Actual Voltage
Display Output Current - Series VII only
Display Current Limit Setting - Series VII only
Preset Voltage - 3.3 kV channels
Preset Voltage - Series VII
Preset Current Limit - Series VII only
Set Voltage Limit
Zero/Restore - voltage on each channel
Shut Down all channels rapidly (PANIC OFF)
Enter/Exit Diagnostics Mode
Set Idle-Down Values
Enter/Exit Idle-Down Mode
Select HV Run Up Rate
Commonly Restore all failed Series VII channels

Power On

When the HV4032A is switched on, the High Voltage Power Supply (HVPS) is in the stand-by mode. If demand voltages have been maintained by the battery back-up, the front panel display will indicate:

Ch 00 00XX Volts

If the high voltage is turned on, the outputs will be set to the values in memory, except for any channels that have a changed pod type. Note that when removing a Series VII pod, a power on will erase the programmed values for those channels since the empty slot is interpreted as a 3.3 kV pod.

If the memory has not been maintained, all demand voltages are set to 0 and the display indicates:

Ch 33 1500 V or Ch 70 3000 V

Channel Assignments and Mode Definitions

The HV4032A has thirty-two possible physical channels. These are numbered sequentially from 0 to 31. In the case of Series VII (7 kV units), there are two channels reserved in firmware for each physical channel, the voltage channel being an even number and the current channel the next higher number (displayed as the voltage channel with a "c" in the most significant digit of the voltage display.) Note that the odd channel numbers of HV4016A1P/N pods are non-functional and will fail if voltage programmed.

There are also several pseudo-channels or registers used to access some of the operating features. Some of these depend upon the actual complement of pods in the set. When a preset register is not applicable it cannot be accessed on the front panel display. Since empty pod slots are recognized as 3.3 kV channel slots, a mainframe without a full complement of pods will always display the 3.3 kV preset register. The features of these registers are discussed below:

Register 33 - Is used to preset the demand voltage for all 3.3 kV channels. When not user-accessed its default value is 1500 V, however, this value is not entered unless the VOLTAGE button is depressed. The voltage displayed will be loaded for all 3.3 kV pods when the VOLTAGE button is pressed, if the high voltage is off. This Register can be used to ZERO or RESTORE all 3.3 kV pods.

Register 43 - "Idle-Down" register for 3.3 kV channels. To enable the Idle-Down mode for 3.3 kV channels, a non-zero voltage demand must be entered into Channel 43. The Idle-Down demand may be any value within the normal, programmable range and may be enabled/disabled while HV is ON or OFF. Idle-Down is an alternate operating state, entered by ZEROing either Register 43 or 47. The mode is indicated by the most significant digit of the voltage display flashing a "ɔ". Both Idle-down registers are always accessible on the front panel display regardless of the complement of pods. If both Idle-down registers contain 0000 it is not possible to enter Idle-down.

Upon entering the Idle-Down mode all channel types that have been enabled to Idle-Down will simultaneously change to the respective Idle-Down value. Idle-down or Idle-up changes occur at a rate of 1.7 kV/sec for 3.3 kV channels or 3.5 kV/sec for Series VII channels if the HV run-up rate selected using Ch. 99 is at maximum (display of 99 0000). Otherwise the Idle Down/Up rate is the same as the turn on rate. HV changes upon entering Idle-down occur in the same way as if the Diagnostics mode were enabled. Digital regulation is temporarily by-passed and voltages are allowed to be ± .5% from demand. If the unit is in the normal Regulate mode the outputs will slowly regulate after Idling down. Digital regulation (± .1%) will then be restored. Exiting Idle regulates similarly to a normal HV Turn-on. The regulation of both the 3.3 kV and 7 kV channels in the mainframe will be slightly affected in this way even if only one type is enabled to idle-down.

ZEROed and FAILed status information is maintained during a change in mode. While operating in the Idle-Down mode, all functions remain accessible; voltages can be changed, ZEROed or RESTOREd; HV may be turned ON or OFF. Demand voltages that are changed while in Idle-Down are lost upon exiting the mode, and a later entry into Idle-Down will set all channels to the respective Idle-Down voltage displayed. Failed channel detection is purposefully slowed down in the Idle down mode. It may take up to 30 seconds for a single channel to be judged as a failed channel, although several problematic channels will be detected in less time (down to 1 sec if all channels are beyond the error limits).

The original operating voltages are Restored when Idle-Down mode is exited by RESTORing either the 3.3 kV or 7 kV Idle-Down register.

Register 47 - Same as 43 except that it is used for 7 kV voltage channels. Current limits are not changed during Idle-Down.

Register 70 - Same as 33 except that it is used for 7 kV voltage channels (default value of 3000 V.)

Register 70 c - Same as 33 except that it is used to set 7 kV current limits. All current channels are automatically initialized to 511 μA until they are otherwise programmed.

Register 99 - "Diagnostic Mode Register." The Diagnostic Mode bypasses digital regulation and failed-channel detection (both are based on ADC readings) and allows voltage and current limit programming below minimum settings. The minimum current limit which may be programmed is 1 mA in the Diagnostic Mode. Although most unloaded pods will operate at this level, the guaranteed minimum operating level is 5 mA which is the lowest current limit which may be programmed in the normal, Regulate Mode. The Diagnostic Mode is indicated by the most significant digit of the voltage display flashing a "u." Diagnostic mode is entered by ZEROing channel 99 and exited by RESTORing channel 99. There are no limitations as to when a mode change can be accomplished. The voltage displayed for channel 99 is not affected by the ZERO or RESTORE operation.

When digital regulation is defeated, the Diagnostic mode controls the HV outputs as follows. No change is made to the HV outputs unless requested. All requests to change the HV output will end by loading the demand value into the DAC buffer of the mainframe. This leaves the HV outputs to the accuracy of the analog circuits (within 0.5% of demand). This occurs after an HV runup or a change in the demand of any single channel. The front panel monitor still shows the actual output voltage accurately.

If a change in mode is made from Diagnostic to Regulate mode, the HV outputs will, through digital regulation, approach and stabilize at the demanded output voltage. Restoring any voltage channels will force an immediate adjustment of the HV output to the correct value. After the mode change any channels that were in error by a large

enough amount in the Diagnostics mode will be detected and failed in the regulate mode. The current limits and voltage demands which were programmed while in the Diagnostic Mode will remain even if those values are lower than could be programmed in the Regulate Mode.

When a change is made from the Regulate to the Diagnostics mode, the HV outputs will remain unaltered, subject to the stability of the analog circuits unless a channel demand voltage is changed or a restore operation is performed.

Channel 99 voltage programming is used to select the HV Run-up rate. The turn off rate is the same as for turning the HV on. The value displayed is interpreted as the power of 2 by which the standard rate is divided for HV ramp-up. The following table details the available run-up rates.

CHANNEL 99	3.3 kV CHANNELS	SERIES VII CHANNELS
0	1 kV/sec	2 kV/sec
1	500 V/sec	1 kV/sec
2	250 V/sec	500 V/sec
3	125 V/sec	250 V/sec
4	62.5 V/sec	125 V/sec
5	31 V/sec	62.5 V/sec
6	16 V/sec	31 V/sec
7	8 V/sec	16 V/sec
8	4 V/sec	8 V/sec

Programmed changes in demand voltage for a single channel, ZEROing of channels or a RESTORE operation while HV is on will also occur at the rates detailed above. Channel 99 is reset to 0 only if the battery backup fails. If the batteries remain charged, the HV run up rate is remembered upon AC power-up.

Front Panel Mode Displays

The most significant digit of the Voltage Display is used to indicate alternate operating modes.

Diagnostic Mode

Idle Down Mode

Both Diagnostic and Idle Down Modes

These indicators alternate with the normal character in the display.

HV Limit Set

This potentiometer adjusts the maximum voltage to which any channel can be set. It causes a control to be bussed to all channels, thus

serving as a hardware clamp voltage. The relationship between the knob setting ($0 \leq S \leq 10$) and the maximum output (V) is approximately V=((.314 x S)+.24) kV for 3.3 kV channels and V=((.628 x S)+ .96) for Series VII channels.

To set the voltage limit more accurately, the following procedure is recommended. Using the Preset Register(s),

1. Turn the HV LIMIT control clockwise to full-scale.

2. Preset all channels to the desired maximum voltage.

3. Turn on HV.

4. Slowly rotate the HV LIMIT control counterclockwise until one channel reports failure. This channel has the largest clamp voltage sensitivity. Note the channel number.

5. Rotate the HV LIMIT control clockwise and restore the failed channel.

6. Select the Diagnostic Mode and return the display to the noted channel.

7. Rotate the HV LIMIT control until the displayed channel first indicates a voltage sag.

8. Return to Normal Mode.

CAUTION: The Limit feature offers protection against dramatic over voltage. Individual limit points may vary channel-to-channel by as much as ±2%. This constitutes a range of 280 V for 7 kV settings.

NOTE: Series VII channels also have a unique per channel analog voltage limit. Refer to Series VII Technical Discussion, Section 3.7, for application information.

Setting Demand Voltage

Voltage demands are loaded into the HV4032A using CHANNEL, VOLTAGE, INCREASE, and DECREASE buttons. Settings are indicated in the Channel and Voltage displays. When the CHANNEL button is pressed, INCREASE and DECREASE operate on the Channel Display. If VOLTAGE is pressed, they operate on the Voltage display. The output of the HV4032A is not affected until the VOLTAGE button is released. (See Technical Description, section 4.3.)

Setting Current Limit

For those stations containing Series VII pods, odd channel numbers are omitted. Current subaddresses are substituted. These are the even channel numbers with a "c" prefix located in the most significant digit of the voltage display. For example:

20 c125

represents channel 20c with 125 μA for the output current.

When the VOLTAGE button is depressed, the user-selected current-limit is displayed. Otherwise, the actual output current is indicated.

Presetting All Channels of Each Series

Channel 33 is used to preset all channels of the 3.3 kV series to the same voltage. Channel 70 is used to preset all channels of the Series VII to the same voltage. The preset feature can be used only when the high voltage is off.

To use the HV4032A in the preset mode, turn off the high voltage, select Channel 33, and choose the desired voltage up to 3.3 kV. To preset the Series VII pods, turn off the high voltage, select channel 70 and choose the desired voltage up to 7 kV. When high voltage is turned on, all channels should come to the preset level.

The current limit may be set on the 7 kV supplies by turning off the high voltage, selecting channel 70c (Note: the "c" shows on the voltage display in the MSD position), and choosing the desired current limit in μA. Note that all Series VII current limits are initialized to 511 μA until altered.

HV ON/HV OFF

Pushing the HV ON button turns the high voltage on. Turn-on involves enabling a 40 V DC regulated supply common to all the High Voltage Power Supply (HVPS) and a slow ramping of the output voltage, (1 kV/sec for 3.3 kV series and 2 kV/sec for Series VII) with a final approach to the demand voltages under the microprocessor control. (See Technical Description, Section 4.5). This standard rate may be slowed down using register 99. The standard run-up procedure takes up to 10 seconds during which the display is blank. The HV ON light comes on immediately to indicate HV is present at the HV outputs. The STATUS output Lemo goes into its clamp to ground state.

When the HV is ON, pushing the HV OFF button causes the voltage to ramp down. The display goes blank with the HV ON light on until the rundown is complete. This process requires up to 10 seconds. With HV OFF the STATUS output is pulled up to +5 V. HV turn off always occurs at the same rate selected for HV run-up.

A precaution to prevent a false current trip during HV turn-on is to always allow about 30 seconds after an HV turn off before turning the HV back on. This allows the Series VII pods enough settling time to insure a smooth HV turn on.

ZERO/RESTORE

Pushing Z (ZERO) sets the channel indicated in the Channel Display to

some minimal value, usually 30 V or less. The Voltage is decreased as described above to avoid damage to the load. The Voltage display is blanked for the duration of the transition. Pushing R (RESTORE) performs the complementary operations. Voltage channels restore at the same rate that applies to HV Turn ON. Zeroing a Series VII current limit channel does not alter the current but does zero the corresponding voltage demand for that channel. ZERO/RESTORE does not affect the values stored in registers 33, 70 or 70c. A RESTORE on register 70 restores all ZEROed and failed Series VII channels and will fine-tune all Series VII channels as described below. ZERO and RESTORE operate similarly on all 3.3 kV channels using register 33. The ZERO and RESTORE buttons are also used to access the IDLE-DOWN and DIAGNOSTIC Modes.

A Restore operation on a channel that is producing voltage will cause digital regulation to fine tune the output to the exact voltage rapidly. This may be especially useful if the output is lower than demand and approaching the demand slowly as may occur in the idle down mode.

3.2 PANIC/INTERLOCK

Safety Shutdowns

Two means of rapid shutdown of all channels within a mainframe are provided: the PANIC button and the INTERLOCK input. Both have the identical effect of shutting down all supplies. This allows the outputs to rapidly go to zero as the output capacitors are discharged through the load and internal sense resistors. Both safety shutdowns are active in the local and remote modes. High voltage may be restored by conventional HV ON commands after the safety interlock is released.

Application of either of these conditions is indicated by the READY LIGHT (integral with HV ON indicator) being extinguished. This condition is reported in the remote mode.

PANIC OFF - Momentary pushbutton (integral with HV ON and READY indicators). In order to accommodate replacement of lamps, this button is designed to be easily removed from its fixture. thus "snapping" the button may cause it to come out of its socket. Replace bulbs with Type 382 (T1 3/4 base, 14 V 80 mA) bulb (LRS part number 320-240-003).

INTERLOCK - The INTERLOCK is a front panel BNC input accepting TTL levels. An internal 4.7 KΩ pullup resistor to +5 V acts as a 1 mA load in the low state. When daisy-chaining many INTERLOCK inputs, care must be taken not to overload the user-supplied driver.

The INTERLOCK is said to be active when it

disables the HV outputs. A jumper option (P1) located immediately behind the front panel allows the user to select Low or High active. These positions are designated N and I respectively on the circuit board. The unit is factory set with the jumper plug in the "N" or Active Low position. CAUTION: The Active High configuration, used for failsafe interlock, will cause a HV4032A with no INTERLOCK connection not to respond. For the purpose of test, a 50 Ω terminator on the interlock will operate the INTERLOCK circuit.

STATUS - Front panel Lemo output. Clamps to ground when HV is present at rear connectors. Output is open collector with an internal 4.7 KΩ pullup resistor to +5 V. Up to 32 mainframes may be daisy-chained, providing a clamp-to-ground if any HV4032A has the HV on. Each status output can sink ≥35 mA. Note that loss of power by an HV4032A will cause its status output to present a 4.7 KΩ path to ground. This can affect the operation of a STATUS daisy-chain.

Each channel of the Series VII pods also has a load-protecting hardware trip. This causes the channel detecting a fault to rapidly shut down. A rear panel connector on each channel allows the trip to be cascaded to other channels. For details, see the description of the Series VII pods in Section 3.7 and 4.2.

3.3 Fault Indicators

A channel is flagged as a failed channel if the high voltage is on and the measured output voltage is different from the demand voltage by ±64 V for 3.3 kV pods or ±128 V for Series VII pods. This is indicated by 9999 in the VOLTAGE (current) display corresponding to the failed channel number in the channel display.

A Series VII current trip (see Section 4.2) is indicated by 8888 in the VOLTAGE (current) display corresponding to the tripped channel number in the channel display. If several channels have their trips ganged, they will shut down together but only the channel sensing the trip condition will report as 8888. The remaining channels report 9999.

Normal causes of a failed channel:

1. The HV LIMIT SET control is set too low for the demand voltage.

2. The Output is overloaded or shorted and unable to reach demand due to current limiting. Series VII channels will fail during a current limited run up if the output dV/dt is less than 100 V/sec.

3. The Load is developing high voltage corona or arcing. The output must be in error for 2 consecutive readings so that single arc may not cause a channel to fail. (Special sense circuitry of the Series VII pods will detect arcs at the load and crowbar the output.) For any 3.3 kV channel or any Series VII channel with its trip circuit defeated the output must be in error for a duration of at least 200 msec to be failed. It may take longer than this for the microprocessor to locate the failing channel. The channel will return to normal with a restore command.

A local shutdown condition is indicated by the channel and voltage displays flashing 66 6666 while the mainframe is in the normal regulating mode. This condition is generated by a fault in the low voltage power supply (HV4032A-3). A temperature sensor monitors the case temperature of the output transistors of the 40 V DC supply. An over voltage monitor on the 40 V DC supply can also generate the local shutdown.

Local shutdown can occur only when HV is on. Once detected, the HV is turned off by an immediate shutdown of the 40 V supply. The mainframe remains locked in this mode and will not communicate via the front panel or the serial communications port.

The AC power must be cycled when local shutdown is encountered to allow communication with the front panel or the serial port.

1. Leave AC power on for at least 10 minutes to allow fans to cool unit.

2. Check air filters and clean if dirty.

3. Cycle AC power and turn HV on. If local shutdown occurs again, the internal 10 A fuse on the LVPS should be checked.

For more information, refer to Section 4.4.

3.4 Remote Mode - TTY

3.4.1 System Interconnection

Equipment Required:

1 HVDC-14 or equivalent cable for each HV4032A employed (See Figure 3.4). The maximum cable lengths between remote controller and mainframe is 1000 feet. See Figure 3.2 for recommended wiring with cables longer than 250 feet.

1 HVTC-14 (See Figure 3.5).

1 HVTT-14 or equivalent (See Figure 3.3).

1 TTY, line printer, or CRT terminal - must generate and respond to the American Standard Code for Information Interchange (ASCII), particularly the portions covering control functions,

numbers, and upper case letters. Must be able to function as the passive element of a 20 mA current loop interface at either 110 or 300 BAUD.

Connect pigtail ends of HVTT-14 to TTY terminals using Figure 3.3. SI and SO are sometimes designated receive and transmit, respectively. Make connection between HVTT-14 and the first HV4032A's J1 connector with the HVDC-14 cable assembly. The J2 connector can be connected to the next mainframe's J1 via HVDC-14 cable. Up to 16 mainframes may be "daisy-chained" in this manner.

The last J2 connector must be terminated with an HVTC-14.

3.4.2 BAUD Rate Selection

Operation at 300 BAUD is recommended. Verify that the BAUD rate of the HV4032A/M (TTY mode) and the terminal to be used are the same. An HV4032A/M is set for 300 BAUD when delivered. To change or verify BAUD rate, the front half of the top cover must be removed.

Identify the digital board (HV4032A-2) which is mounted horizontally on the right side of the mainframe. At the front right corner of the board, a jumper plug is labeled BAUD.

For 300 BAUD operation:
Factory set, BAUD jumper across the end pin labeled 300 and the center pin of the 3-pin header.

For 110 BAUD operation:
Move BAUD jumper to be across end pin labeled 110 and the center pin of the 3-pin header.

NOTE: For older HV4032 and HV4032A without 7 kV compatible firmware, the BAUD rate jumper plug is read only once upon power up and should be changed with the AC power off. BAUD rate programming for 7 kV compatible HV4032As may be changed at any time.

3.4.3 Control Switches

MAINFRAME ADDRESS: Each mainframe must have a unique address and the last HV4032A must be assigned address 16. This unit echoes the TTY as described in Section 4.10. It is not required that the mainframes be sequentially assigned. The MAINFRAME ADDRESS switch may be changed while the unit is switched on. If the address switch is changed and the mainframe was selected, the mainframe remains selected but responds with its new address. See section 3.5. Note that the older HV4032 examined its mainframe address only once on AC power up and that changes in this switch setting will not be recognized while power is on.

LOCAL/REMOTE Switch: All units should be placed in the remote mode. If, for purposes of local inspection, the unit is placed in the local mode while in a daisy-chain configuration, communication with other mainframes is possible. However, if mainframe 16 is in the local

mode, echo-back to the TTY will not be generated to all commands. When the switch is returned to the remote position, the mainframe will still believe itself to be selected if it was selected before being placed in the local mode. See Section 3.5.

NOTE: If the AC power of any mainframe is turned off, the entire daisy-chain is disabled.

3.4.4 Interconnection accessories available from LeCroy are:

HVDC-14	Standard connection between HV4032A mainframe and 2132 interface, HV4032A mainframe and HVTT-14, and between HV4032A mainframes. Specify length in feet.
HVTC-14	Terminating connector. Connects to J2 of mainframe address 16.
HVTT-14	HV4032A to TTY adapter to be used with HVDC-14.
HVEX-14	Extension cable in lengths of 100 feet. To be used with HVDC-14.
HVCK-14	A connector block, pins, and strain relief. Available for users who wish to make their own cables.
HVAC-14	An adapter cable (see Figure 3.7) to connect between an HV4032A mainframe and a data cable of the original HV4032 family. See Appendix.
HVAK	All parts required to change connector retention hardware of HV4032A family cables (see Figure 3.8) to mate with original HV4032 family cables or front panels. See Appendix.
NOTE:	Refer to appendix for directions that apply to constructing a system with HV4032As and HV4032 family mainframes.

3.4.5 Data Cable Components

CROSS REFERENCE

LRS #	DESCRIPTION	AMP PART #
405-152-001	Connector Block, Pin	201297-1
405-161-001	Connector Block, Socket	201298-1
405-232-004	Male Guide Pin	200389-4
405-240-005	Male Jackscrew	200868-2
405-332-003	Female Guide Pin	200390-4
405-360-005	Female Jackscrew	200870-2
405-453-020	Connector Pin	66308-4
405-555-001	Connector Socket	66309-4
405-712-001	Female Locking Spring	201992-1

405-721-002	Male Locking Spring	201921-1
405-786-008	Strain Relief Clamp	201843-1

3.5 USING THE HV4032A WITH TTY

When operating the HV4032A with a TTY, individual units must have a way of distinguishing the destination of commands. This is accomplished with mainframe addressing, using the letter M followed by a number from Ø to 16. For numbers greater than zero, the desired unit becomes selected and is the destination for all commands until the next use of mainframe addressing. An MØ command causes all units to respond to the next command (if possible) and then deselect themselves. It is then necessary to issue another addressing command. In the event of an error in entering a mainframe address (non-numeric character, or non-existent unit) an error message will be printed and all units will deselect themselves. When all mainframes become deselected, no echo back to any characters occurs until an M is entered on the keyboard. If it is desired to enter a mainframe address without specifying a command on a command line, the mainframe address should be terminated with two carriage returns.

CAUTION: Whenever a selected mainframe is taken "Off-Line" by changing the LOCAL/REMOTE switch to the local mode, the mainframe cannot be unselected. If another mainframe was selected during this time a situation can occur such that two or more mainframes will respond to commands once the other units come back "On-Line." "Off-Line" mainframes can be identified since they will not respond to an MØ Command. If in doubt, precede commands by the M## command until it is certain that all mainframes are "On-Line."

Following the mainframe address, the unit is ready to accept commands. All commands have the general format of one letter, optional numbers, and a carriage return. Error checking is performed on all commands. The first character in a command is always echoed back to the TTY. Subsequently, errors will not be echoed but will cause a "?" followed by a carriage return and prompt ("!"). Commands are checked for validity (e.g. "b" is meaningless) and proper termination. Numbers are limited to 4 digits (if more than 4 are entered the rightmost 4 are used). All errors cause no action to be taken and, where possible, print an error message. (note that this allows easy termination of unwanted commands.) All valid command lines must be terminated with a carriage return.

The TTY operations to which the HV4032A can respond are similar to those available in the local mode. These operations are:

HV OFF
- Read Demand Voltage or Current and Modify Each Channel
- Preset Voltage - 3.3 kV Channels
- Preset Voltage or Current Limit - Series VII

HV ON

· Read Actual Voltage or Current and Modify Each Channel
Zero/Restore - Voltage on Each Channel
Enter/Exit Diagnostics Mode
Set Idle-down Values
Enter/Exit Idle-down Mode
Select HV Run-up Rate
Commonly Restore all Failed Series VII Channels
Report Pod Complement of Mainframe
Report Status of Mainframe
Report all Demand Voltages/Current Limits
Report all Output Voltages/Currents

Front panel operations still active in Remote Mode are:

- Interlock
- Panic Off
- Voltage Limit Setting
- Mainframe Address

COMMANDS

N - Turn high voltage on.

F - Turn high voltage off.

I - Identify. Returns the pod configuration of the unit. Eight numbers (either 7 or 3) will be printed according to the actual pod type. Pod number zero will be on the left. The response 7 indicates a 7 kV pod and 3 indicates a 3.3 kV pod or empty pod station.

S - Status request. Returns status of high voltage (on/off), any failed channels, and indicates if in the Diagnostic or Idle-Down mode.

V - Voltmeter readings. Returns the actual measured output voltages/currents for all channels.

D - Demand Settings. Returns the demand voltages/currents for all channels. During this printout, the word ZERO will be used to indicate the ZEROed state versus a setting or reading of value zero, the word FAIL will be printed if necessary. Idle-Down Register and HV run-up rate register programming is also returned.

Pxxxx - Preset all 3.3 kV channels to xxxx. This command will work only if high voltage is off. Note this is identical to using register 33.

Cxx - Address a specific channel or register for further operations. The letter C may be entered after xx to indicate the current mode of the 7 kV channel, or the next higher odd number may be used. For example, CØØC is the same as C01 or C1. At this point, two courses are possible depending on the

channel number entered.

Real Channels - (number less than 32.) For these channels, a carriage return can terminate the command. If it is used, the unit will respond with a voltage or current. This will be the measured output voltage if high voltage is on, or the demand setting if it is off. In the event that a channel is either ZEROed or FAILed, the word ZERO or FAIL will precede the voltage. A new voltage may now be entered and the unit will update the output if it is on. The commands "Z" and "R" may be used whether the carriage return option is used or not. These commands have the same definitions as the front panel buttons. A carriage return terminates the command line.

Registers - (number greater than 31.) For these channels (registers), a slash (/) is mandatory. Following it may be either the "Z", "R", or a new voltage, and must be terminated with a carriage return. If a "/" is not used after the register number, a "?" will be printed and the command ignored.

(Note that channel numbers less than 32 may not be used with the MØ command.)

Channels that experience a current surge trip or that are daisy-chained to trip in common are reported as FAILed channels. The initiating channel of the trip sequence is labeled the "initiator" as part of the failed channel report. See following examples.

CAUTION: In TTY Mode, a 7 kV compatible mainframe must terminate the remote mode daisy-chain and be assigned as mainframe address 16 if used in conjunction with mainframes that are not 7 kV compatible.

3.5.1 Fault Reporting

A failed channel is reported in the following way:

```
!MXX*CHYY
```

Refer to Section 3.3 for further details of failed channel diagnosis.

A local shutdown condition is reported as:

```
Local Shutdown-Check Fan Filters
```

The mainframe will not function normally in either local or remote mode until the AC power is cycled. However, communication with other mainframes will not be interrupted as long as AC power remains on.

The application of either the interlock or the panic off will be reported as follows:

```
M##
TRIP (PANIC OFF)
```

Series VII channels that experience a current surge trip or that are daisy-chained to trip in common are reported as FAILed channels. The initiating channel of the trip sequence is labeled the "Initiator" as part of the failed channel report. See following examples.

Spontaneous reporting of failed channels may be suspended for both the CAMAC and TTY modes by a jumper option on the HV4032A-2 board. The jumper can be accessed by removing the top front cover. The jumper, labeled OPT, is adjacent to the BAUD rate jumper. Failed channels are still reported by the Status Request. In the OPT position, reporting is suspended. In the NOR position, reporting is active.

3.5.2 Examples of TTY Use

In the following examples, a lower case x is used to denote the use of the carriage return key. Characters generated by the HV4032A are underlined. Note that all spaces are generated by the HV4032A.

>M16_C20x 2000_3200x	Entering channel voltage with mainframe addressing.
>C20x 2000_3200x	Entering a channel voltage without mainframe addressing.
>M16_C70_C/500x	Entering current preset with mainframe addressing.
>C10_Rx	Restoring channel of previously addressed mainframe.
>C99_/Zx	Entering diagnostic mode.
>M16CH00 Initiator >M16CH02	Trip sequence of the channels 0 and 2 daisy-chained. Channel Ø detected current surge.
Invalid	
>M0_C2x	Channels less than 32 not allowed with MØ.
>C99_Rx	Missing slash. (see above)
>m16	Command in lower case.
? >	

3.6 Using the 3.3 kV Plug-in Pods

The HV4032A1N and HV4032A1P are quad high voltage power supplies and the HV4016A1N and HV4016A1P are dual high voltage power supplies. The N and P suffixes denote negative or positive polarity, respectively. Each power supply within a pod is referred to as a channel. Both the HV4032A1N/P and the HV4016A1N/P have a maximum output voltage per channel of 3.3 kV. The difference between the HV4032A1N/P and the HV4016A1N/P is that the quad supplies provide a maximum output current of 2.5 mA per channel, while the dual supplies provide a maximum output current of 5 mA per channel. For both the quad and the dual power supplies, the output voltage of each channel may be programmed from 100 to 3300 V in 1 V steps with a fixed current limit of 3 ±0.3 mA for the HV4032A1N/P quad power supplies and a fixed current limit of 6 ±0.6 mA for the HV4016A1N/P dual power supplies.

Using the Diagnostic mode of the HV4032A/M mainframe, the 100 V lower limit constraint is defeated, thus allowing lower values to be selected. When the diagnostic mode is exited, these values remain in effect. However, subsequent programming causes the channel output voltage to revert to the limit defined for the programming range.

The output voltage of both the HV4032A1N/P and the HV4016A1N/P has a very good regulation (±.05% line; ±0.5 V load), high accuracy (±0.1% + 1.5 V) and very low ripple (typically less than 50 mV rms) for output voltages greater than 1,000 V.

The HV4032A/M will accommodate a mixture of 3.3 and 7 kV pods of both negative and positive polarity. The firmware in the HV4032A/M recognizes the 3.3 or 7 kV pods and makes the appropriate programming decisions; however, the polarity of the pods is not recognized by the firmware.

Each channel of the 3.3 kV pods has a current limit circuit which limits the DC current to 3 ±0.3 mA for the HV4032A3N/P units and 6 ±0.6 mA for the HV4016A3N/P units. If the load demands a current in excess of the current limit value, the supply will operate in a current-limited mode, lowering the output voltage, setting the current equal to the current limit value. For time varying loads consistent with the response time of the current limit circuit (several msec), the circuit will react dynamically. A power limiter circuit becomes active for programmed output voltages in excess of 2200 V to linearly reduce the current limit to prevent overloading of the channel.

A failed channel is defined as an output voltage ($V_{measured} - V_{demand}$) greater than or equal to 64 V. The HV4032A/M mainframe responds to this condition by running down the output voltage to zero. The failure condition is detected and processed within 200 msec. (It may take longer for the mainframe to detect a failed channel if it is involved in other tasks such as HV Turn On.)

If long cables or highly capacitive loads are attached to the HV

pods, the HV output's decay time may become a function of the RC loading at the output and the channel may not be able to respond as quickly as the mainframe is controlling the decrease in HV output. This condition only poses a problem for the mainframe if an HV output is decreased to some very low value (below 300 V) from a much higher operating point. The mainframe may not detect the HV output is too high if its decay time is excessive and fail the channel. A Restore operation will then correct the output since increases in HV output are well controlled by the mainframe and are not affected as severely by external capacitance.

3.7 Using the 7 kV Plug-in Pods

3.7.1 General Description

The HV4032A7N and HV4032A7P are dual high voltage power supplies with 7 kV output capability. The N and P suffixes denote negative or positive output polarities, respectively. Each power supply within a pod is referred to as a channel. There are 2 channels per pod. Each channel is programmable from 160 to 7,000 V in 2 V steps with a programmable current limit ranging from 5 to 511 µA in 1 µA steps. Zero demands may also be selected. Using the Diagnostic mode of the HV4032A/M mainframe, the 160 V and 5 µA lower limit constraints are defeated, thus allowing lower values. When the Diagnostic mode is exited, these values remain in effect, however subsequent programming causes the channel output voltage and/or current limit to revert to the limits defined for the programming ranges.

The output voltage of the HV4032A7P/N has very good regulation ±(0.05% line; +1 V load), high accuracy (±0.1% +3 V) and very low ripple (typically less than 100 mV peak-to-peak) for output voltages greater than 1,500 V.

The HV4032A/M will accommodate a mixture of 3.3 and 7 kV pods of both negative and positive polarity. The firmware in the HV4032A/M recognizes the 3.3 or 7 kV pods and makes the appropriate programming decisions, however the polarity of the pods is not recognized by the firmware.

The 7 kV pods are normally supplied with SHV connectors. Under most operating conditions, these connectors will not compromise the operation of the pod. As an operating precaution, any channel which does not have a cable connected to the output connector should be programmed for less than 5000 V output. This precaution insures the integrity of the SHV connector. If the HV4032A/M is to be operated in high humidity or at high altitude, an alternate connector, the UHV (Kings 1064-1) is recommended. This is available from the factory by special request as a Mod 200.

If long cables or highly capacitive loads are attached to the HV pods the HV output's decay time may become a function of the RC loading at the output and the channel may not be able to respond as quickly as the mainframe is controlling the decrease in HV output. This condition only poses a problem for the mainframe if an HV output is

decreased to some very low value (below 500 V) from a much higher operating point. The mainframe may detect the HV output is too high if its decay time is excessive and fail the channel. A Restore operation will then correct the HV output since increases in HV output are well controlled by the mainframe and are not affected as severely by external capacitance.

Capacitive loads may also cause a false current trip if the HV is quickly cycled from On to Off to On. To avoid this possibility, allow about 30 seconds from an HV Off before turning HV back On again.

Capacitive loads (generally greater than 7 nF) may cause false trips during an exit from Idle-down unless a low current limit is programmed or the trip circuit is momentarily vetoed during the Idle-up.

3.7.2 Special Features

Voltage Monitor - The output voltage of each channel is measured with 2 V resolution via a local 12-bit ADC. The actual measured output is available to the user in Local, TTY and CAMAC modes.

Current Monitor - The output current of each channel is measured with 1 μA resolution via the local ADC. These measured values are available to the user as described in the above paragraph.

Current Limit - Current limiting is accomplished by a hard-wired circuit in each high voltage channel which is monitored in firmware. If the DC load demands a current in excess of the programmed current limit, the channel current-limits, lowering the output voltage to set the output current equal to the programmed current limit. For time varying loads consistent with the response time of the current limit circuit (several msec), the circuit will react dynamically, maintaining the output current at less than, or equal to, the programmed current limit. For very rapid changes in current, the trip circuit (see below) will respond.

If the voltage sag ($V_{demand} - V_{measured}$) is greater than or equal to 128 V, the system microprocessor identifies this as a failed channel. In less than 200 msec the fault is located and the output voltage for that channel is set to zero. The programmed demand voltage is saved in memory.

If the voltage sag is less than 128 V and $I_{measured}$ is greater than or equal to 98% I_{limit}, a firmware current limited mode is achieved. This may occur at any time that HV is ON as well as during HV run-up.

The firmware current limit mode (increasing digital regulation being suspended) is generally entered slightly before the hardware current limit takes effect to insure that there is no uncertainty between voltage and current limit regulation. At this transition region attempts to regulate output voltage may be unsuccessful due to current limiting. Without this precaution the internal voltage would

be increased at a rate of approximately 2 V/sec for the duration of the current limited state, and could cause a voltage jump when the load current is decreased. Since analog circuit tolerances may exceed the 2% window (e.g. 0.5 µA offset at a 5 µA limit) it is recommended that the limit be set 5% higher than the expected maximum load.

A limit set of 511 µA defeats this firmware current limit mode to guarantee voltage regulation at maximum rated output.

Current Trip - If a channel output current experiences a surge of 100 µA/50 µsec for a duration of greater than 150 µsec, the channel is automatically shut down (independent of the microprocessor cycle time) by a hardwired detector/crowbar circuit. See LeCroy Application Note 17.

Current Trip Veto - A current trip lockout via the External Controls Header (see Figure 3.9) is available for each pod. This provides a mechanism for the user to supply a veto to the current trip circuit. This control also serves as an external crowbar reset.

Current Trip Control - Pins on the External Controls Header (see Figure 3.9) allow the current trip of any channel to be daisy-chained to a maximum of 31 other channels. Any one of these 32 channels can then be the initiator of a current trip shutdown of all of the daisy-chained channels.

Voltage and Current Clamps - External DC voltages or resistance programming may be used to override the programmed voltage and current limit values of the individual channels. This feature can be used to prevent errors in user excessive voltage/current programming to prevent damage to sensitive loads.

3.7.3 Use of External Functions

The External Controls Header (see Figure 3.9) is the point at which all user-supplied external controls interface with the HV4032A7P/N pods. In this section, the implementation of the external functions is discussed in detail.

Trip - The External Controls Header of each HV4032A7P/N pod has two Trip 0 contacts (pins 11 and 5) and two Trip 2 contacts (pins 7 and 11). Connecting the trip pins of up to 32 channels in a daisy-chain allows any one of the HV4032A7P/N channels in the daisy-chain to initiate a multichannel crowbar shutdown due to a current trip initiation of any channel in the daisy chain.

The Trip-pin out has been designed for convenient daisy-chain connections. The Trip pins of each channel are internally connected to open-drain p-channel FET drivers that are driven to +5 V when a channel has been tripped. The trip input/output is capable of driving a total of 31 Trip loads plus one TTL input. A TTL gate could therefore be used in a user-supplied trip sense circuit.

When a channel initiates a hardware crowbar trip, the initiator channel is identified by a front panel voltage display of 8888 and the subsequent channels in the daisy chain which were also tripped are identified by a front panel voltage display of 9999. In TTY mode, a channel initiating a trip is labeled initiator. For CAMAC operation see the CAMAC response data, Figure 6.10. The identification of the initiator channel is LOST except for hard copy output of user-supplied remote TTY control when the high voltage is turned off. The front panel voltage display of 8888 denotes crowbar trip, while the error code 9999 indicates a failed channel.

A failed channel is defined as an output voltage $V_{measured} - V_{demand}$ greater than or equal to 128 V. The HV4032A/M mainframe responds to this condition by running down the output voltage to zero and setting the voltage display to 9999. In CAMAC and TTY modes, the failure is also reported.

After a hardware crowbar trip condition is generated, the hardware must be reset and the firmware must clear the failed channel status before the tripped channels can be returned to their original operating voltages. The hardware is reset when the HV is turned OFF. Another method would be to use the RESET on the External Controls Header (see below). All tripped channels are now indicated as normal "9999" failed channels and may be RESTORED using normal RESTORE commands on each tripped channel. When several Series VII channels in a mainframe have tripped in common, it is possible to use the RESTORE function on Register 70 which will RESTORE all failed Series VII channels to their programmed voltages. An HV ON command should restore the system to operating conditions assuming the cause of the current trip has been remedied.

CAUTION: If a daisy-chain connector is removed while there is a crowbar shut-down in the chain, and the HV4032A/M mainframe is in the diagnostic mode, the mainframe will attempt to re-establish the programmed demand voltage in the disconnected channel or channels.

Reset - The External Controls Header (see Figure 3.9) has two Reset connections; pins 9 and 3. The reset function is common to both channels of a HV4032A7P/N pod. There are two modes in which Reset may be used.

1. Trip Veto - In many installations, the user may require a current trip veto for some short duration of the data acquisition time. For example, very sharp current spikes at the leading edge of a beam spill might cause a current trip. Unwanted shut-down of the two channels in an HV4032A7P/N pod may be either defeated by connecting Reset, pin 9 or pin 3, to ground (ground is supplied at pins 12 and 2 of the External Controls Header) or overridden using a pulsed clamp-to-ground. This pulsed override must be actively at ground for the duration of the desired override. Due to the bouncing nature of contacts, a relay is not recommended. The LeCroy Model 2323A Dual Channel CAMAC-Programmable Gate and Delay Generator provides the appropriate clamped output.

2. Pod Reset - There are two methods for resetting tripped channels. Either of these two methods resets a tripped channel to the status of a failed channel. The first method is to cycle the high voltage of the HV4032A/M mainframe OFF. The second method is to apply a TTL active low pulse with a 0.5 µsec minimum width to a Reset pin (either pin 9 or pin 3) of the HV4032A7P/N which contains the tripped channel. Once the channel has been reset to the failed channel status the Restore command returns the original demand value and will initiate a controlled run-up if HV is ON.

   I Clamp - An externally controlled current clamp may be hard-wired to either channel of a HV4032A7P/N pod using pin 8 or pin 6 of the External Control Header. This external current clamp may be either resistance or voltage-programmed. Pins 8 and 6 are connected to +15 V via 4.3 KΩ ±5%. A voltage divider using the internal resistor or an externally applied voltage will set the current clamp with the algorithm $I_{max} = 50\ V_{node}$ µA, where V_{node} is the voltage on pin 8 or pin 6. The lowest value at either the external current clamp or the programmed current limit will be selected as the actual current clamp value.

   V Clamp - An externally controlled voltage clamp may be hard-wired to either channel of a HV4032A7P/N pod using pin 10 or pin 4 of the External Control Header. As with the I Clamp, the V Clamp may be either resistance or voltage-programmed. Pins 10 and 4 are internally connected to +15 V via 5.6 KΩ ±5%. A voltage divider, using the internal resistor or an externally applied voltage will set the voltage clamp with the algorithm $V_{max} = 0.8\ V_{node}$ kV where V_{node} is the voltage on pin 10 or pin 4. The actual voltage clamp value will be the lowest value of the front panel voltage clamp which is common to all channels in the HV4032A/M mainframe, the programmed demand voltage, or the hardwired programmed value of V Clamp.

   Both the I clamps and the V Clamps may be most easily set using the Diagnostic mode. If it is necessary to minimize the output ripple in the clamped mode, the clamp pins should be bypassed to ground with 6.8 µF capacitors. The clamp pins may also be dynamically pulsed to implement a hardwired Idle-down although all use of the clamps below programmed voltages should be in the Diagnostic mode to prevent failing the channels.

3.8 Calibration of Pods using Diagnostic Mode

This non standard operating mode is useful for system diagnosis as well as in simplifying the calibration of the HV outputs. When the Diagnostic Mode is enabled the digital regulation described in Section 4.4 is bypassed. The readings of the front panel VOLTAGE Display are a function of the voltage calibration adjustments on the HV4032A rear panel. By defeating the digital regulation a stable output voltage is produced that will not change as the calibration adjustments are made.

Since error detection is defeated in the Diagnostic Mode it is not possible for the microprocessor to generate failed channel reports in either local or remote operation. If a channel is reported as being failed in the normal regulate mode it is sometimes difficult to identify the cause of the failure because the channel is automatically zeroed under microprocessor control. The Diagnostic Mode maintains the demand to the channel so that problems such as arcing may be diagnosed by monitoring the front panel voltage display.

The DAC buffer values are not updated while in the Diagnostic Mode unless a channel's demand value is modified. DAC buffer values are ideal values that will produce a high voltage output based on the accuracy of the local divider network located within the pod (the 400:1 divider in 3.3 KV pods). This feature is used at the factory to calibrate the DAC circuit.

3.8.1 Changing Modes

Upon AC power up the mainframe always sets itself into the normal Regulate mode.

Operational sequence to ENABLE CALIBRATE MODE:

A. Select local mode with LOCAL/REMOTE switch.

B. Select register 99 and depress ZERO.

C. The Diagnostic Mode is now enabled. To return to the Regulate mode, RESTORE register 99.

3.8.2 Rules Governing Diagnostic Mode Operation

A. An indication is given to alert the user that the Diagnostic mode is enabled. This indication is that the front panel voltage display reading flashes a "u" in the most significant digit.

B. The transition between Diagnostic and Regulate modes may occur at any time independent of whether HV is on or off.

C. If the Diagnostic mode is enabled while HV is on the DAC buffer values (and consequently the HV output voltages) will not be modified unless modified by the user.

3.8.3 User Calibration Procedure

HV4032A mainframes are factory calibrated to meet published specifications based on channel to channel matching. The absolute calibration is against a LeCroy in-house voltage standard. Factory calibration of 3.3 kV channels is done at a demand voltage of 3000 V.

In the event that the user wishes to recalibrate the mainframe to some other voltage standard or desires closer matching at some other voltage than 3000 V the calibration procedure is outlined below.

Note that recalibration for matching channel outputs at lower voltages may cause wider variations in output voltage from ideal at higher demand voltages.

Procedure

A. Determine desired calibration voltage and preset channels to be calibrated to this voltage. Turn HV ON.

B. Allow at least 15 minutes for the unit to stabilize.

C. Enable the Diagnostic mode.

D. The user must have the means to measure the actual HV output. Connect the measuring device to the HV output.

E. Set the Channel Display to indicate the channel being monitored above.

F. Insert a small straight edge screwdriver into the adjustment hole associated with the channel being calibrated and find the slot in the adjustment potentiometer. The adjustment is a single turn potentiometer providing about ±0.75% of reading adjustment.

G. Note the reading of the actual HV output. Adjust the potentiometer so that the front panel VOLTAGE Display reads the same as the reading of the actual HV output. Clockwise rotation of the adjustment will increase the front panel reading.

H. Calibrate each channel in similar fashion.

I. Return to the Regulate mode.

3.8.4 Fine Tuning

±1 volt adjustments to the calibration can be made in the Regulate mode. Note that the direction of the potentiometer adjustment is the same with respect to the front panel VOLTAGE Display as experienced in the Diagnostic mode. Make adjustment to set VOLTAGE Display to same reading as independently measured, but make small adjustments and wait for the microprocessor to regulate the outputs. Normal Digital regulation will change the outputs about 1 V/sec.

3.9 Test Modes

The test modes are available with series K or later firmware. If the VOLTAGE button is depressed, during AC power-up the test mode is activated. This is indicated by a flashing "HV ON" front panel light. If the VOLTAGE button is not depressed, the system operates in its normal mode.

When this turn-on procedure is followed, five tests are available for use. One is automatically entered upon power-up, the other four may be selected. The first test will toggle the HV ON light repeatedly,

providing a visual indication that the test mode has been successfully entered. Also, at this time the address bus of the microprocessor is being cycled. To exit this or any other test, press the ZERO button. Once this test is exited, the other four may be selected by using the INCREASE button. The selected test is indicated by the least significant digit in the channel display. To execute the selected test, depress the RESTORE button.

Tests:

0 Calibration test. Intended to aid in the calibration of the digital board analog circuitry. During this test, the most significant digit in the channel display indicates the channel whose voltage is being displayed. Only channels 0, 1, 2 or 3 may be monitored by the front panel LEDs.

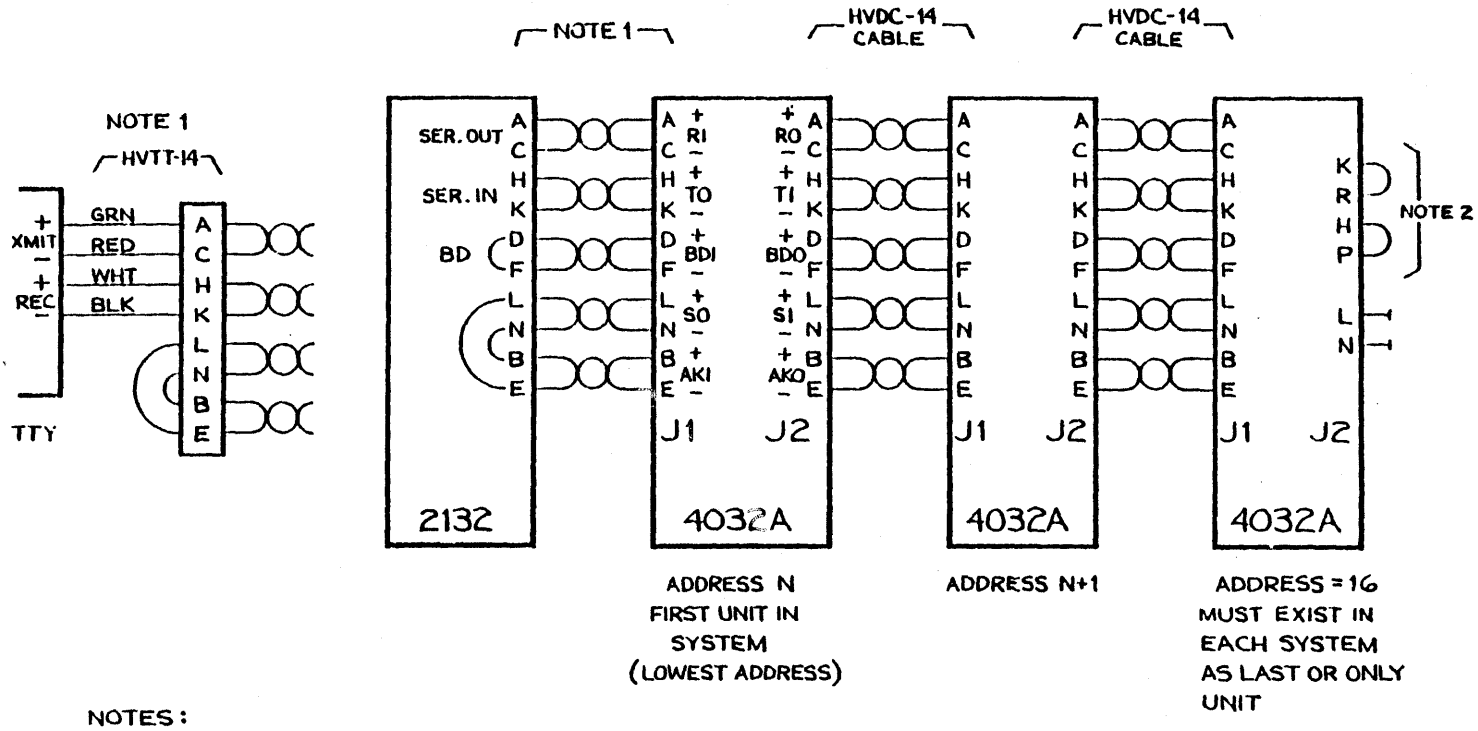
The channel may be changed by pressing the CHANNEL button. In this test, a demand voltage is sent to all channels. This is a repeating pattern of 2800, 2100, 1400, or 700 V. Note that pod type (7/3 kV) is not taken into account, so the actual output of Series VII channels is twice the display value. The channels on which these voltages fall may be altered in two ways. One is to hit both VOLTAGE and INCREMENT, which will "shift left once" the voltage pattern; the other is to hit the INCREMENT button only, which will "shift left twice" the voltage pattern (i.e. switch calibration points).

1 DAC least significant bits test. A digital ramp of the four least significant bits is generated. The direction of the ramp may be changed using the INCREMENT button. By removing the DG 508 on the digital board and terminating the DAC output with a 100 kΩ resistor to ground, the switching and step size of the LSBs may be seen on an oscilloscope.

2 FIFO test. A digital pattern of voltages is generated, such that a scope triggered on U9 pin 3 (upper/lower enable) will display a "walking" pattern when the FIFO lines are scoped in sequence.

3 Serial out test. Simply generates a square wave at the serial out pin of the processor. May be used to facilitate verifying the operation of the front panel board Transmit Circuits, and transmission to other HV4032As in a remote daisy chain.

The mainframe must be powered down to exit the Test Prom.



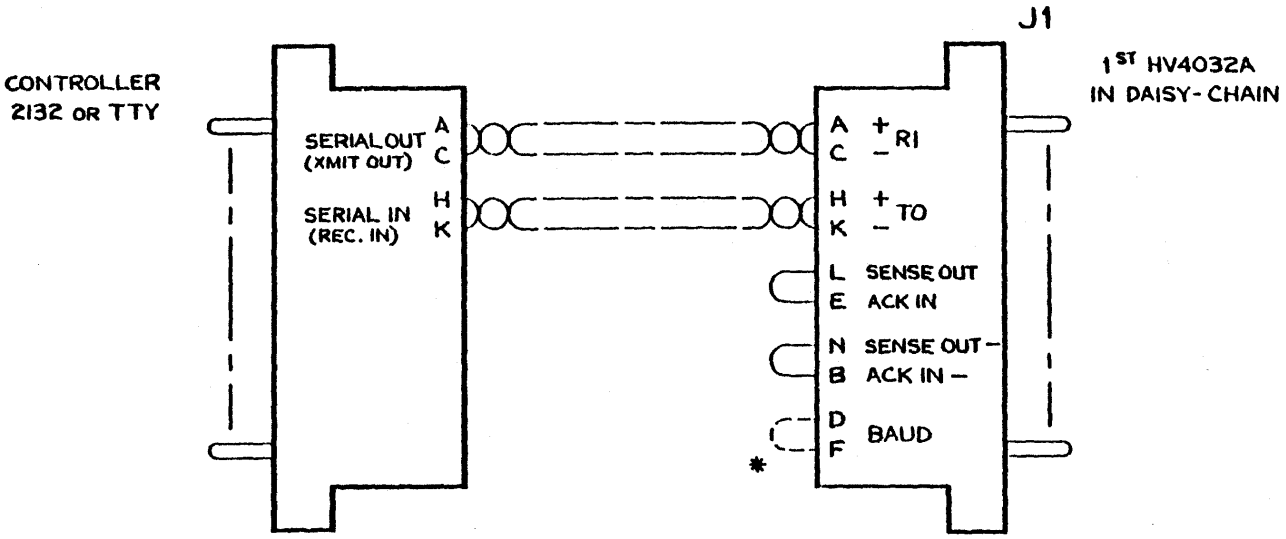
NOTES:

1) CONNECTION TO CONTROLLER:
   USING 2132 - HVDC-14 CABLE CONNECTS AS SHOWN
   USING TTY - HVTT-14 ADAPTOR IS NEEDED BETWEEN THE TTY AND THE MAINFRAME TO BE CONNECTED

2) THE LAST UNIT IN A SYSTEM (MAINFRAME 16) MUST USE TERMINATING CONNECTOR HVTC-14 IN J2.

SYSTEM INTERCONNECTION

Figure 3.1



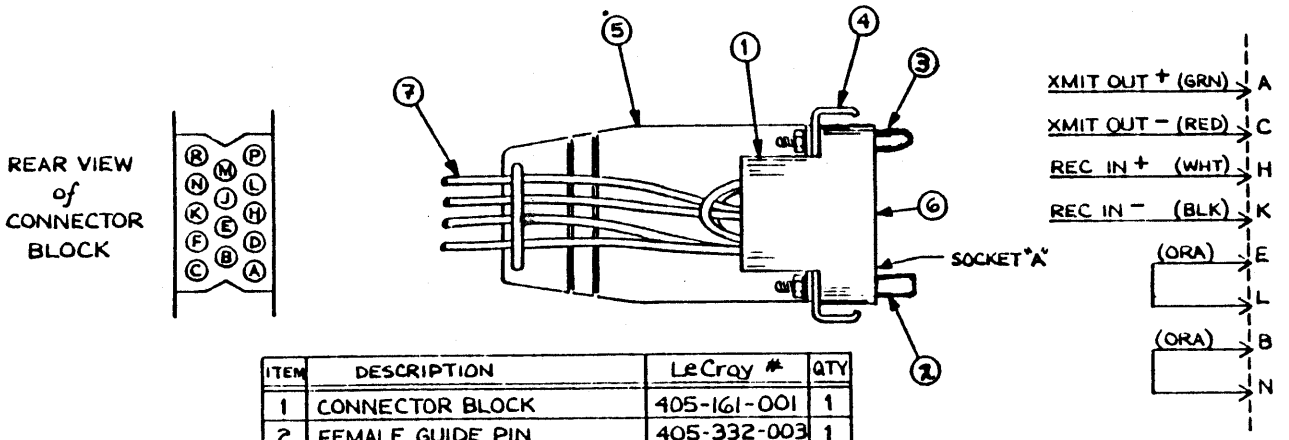
RECOMMENDED CONNECTION OF CONTROLLER TO 1ST HV4032A OF DAISY-CHAIN FOR CABLE LENGTH BETWEEN 250 AND 1000 FEET.

* JUMPER FROM D TO F FOR OPERATION WITH 2132. FOR OPERATION WITH TTY, LEAVE D AND F OPEN.

CONNECTORS ARE LeCroy #405-152-001

LONG DISTANCE SYSTEM CONNECTION

Figure 3.2



ITEM	DESCRIPTION	LeCroy #	QTY
1	CONNECTOR BLOCK	405-161-001	1
2	FEMALE GUIDE PIN	405-332-003	1
3	MALE GUIDE PIN	405-232-004	1
4	FEMALE LKG. SPRING	405-712-001	2
5	STRAIN RELIEF CLAMP	405-786-006	1
6	FEMALE CONN. PIN	405-555-001	8
7	WIRE, AWG #22	———	A/R

WIRE CHART

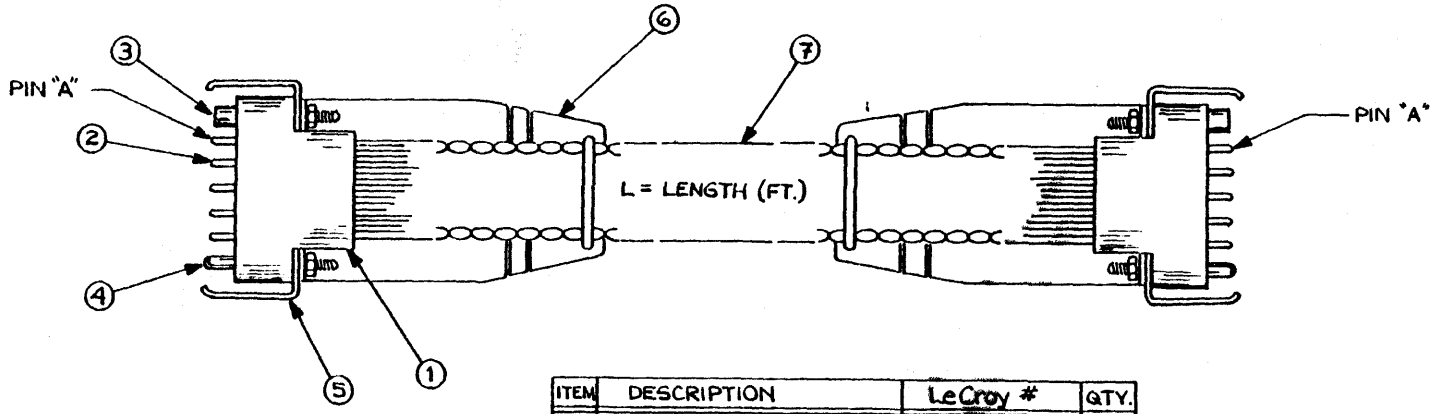
SIGNAL	PIN	COLOR	AWG #	LENGTH
XMIT OUT+	A	GRN.	22	4 FT.
XMIT OUT−	C	RED	22	4 FT.
REC IN +	H	WHT.	22	4 FT.
REC IN −	K	BLK.	22	4 FT.
E TO L		ORA.	22	A/R
B TO N		ORA.	22	A/R

NOTES:

1) HVTT-14 REQUIRES USE OF FEMALE-TO-FEMALE DATA CABLE (HVDC-14)

HV4032A-TTY ADAPTER
HVTT-14

Figure 3.3



ITEM	DESCRIPTION	LeCroy #	QTY.
1	CONNECTOR BLOCK	405-152-001	2
2	MALE CONN. PIN	405-453-020	28
3	FEMALE GUIDE PIN	405-332-003	2
4	MALE GUIDE PIN	405-232-004	2
5	MALE LKG. SPRING	405-721-002	4
6	STRAIN RELIEF CLAMP	405-786-008	2
7	CABLE, (7 PAIR)	592-120-014	A/R

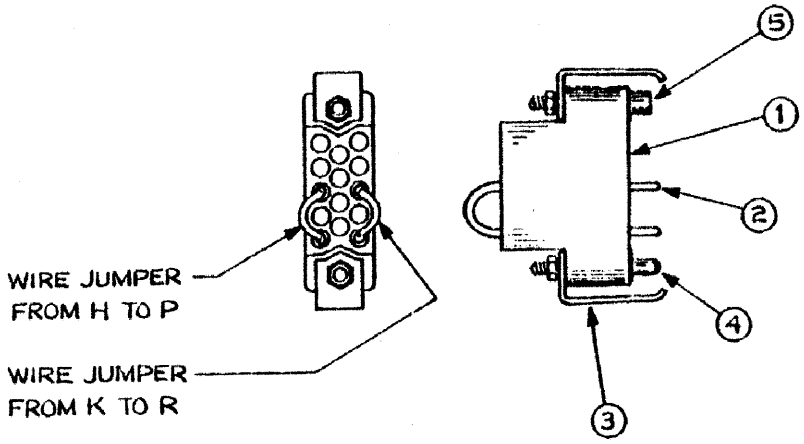
NOTES:

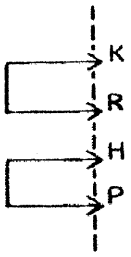
1) WIRE CABLE TO CORRESPONDING PINS (A TO A, B TO B, ETC.), USING CHART BELOW

PAIR NO.	PIN	COLOR
1	A	BRN
	C	TAN
2	B	RED
	E	TAN
3	D	ORA
	F	TAN
4	H	YEL
	K	TAN
5	J	GRN
	M	TAN
6	L	BLU
	N	TAN
7	P	VIO
	R	TAN

CABLE ASSEMBLY
HVDC-14-L

Figure 3.4

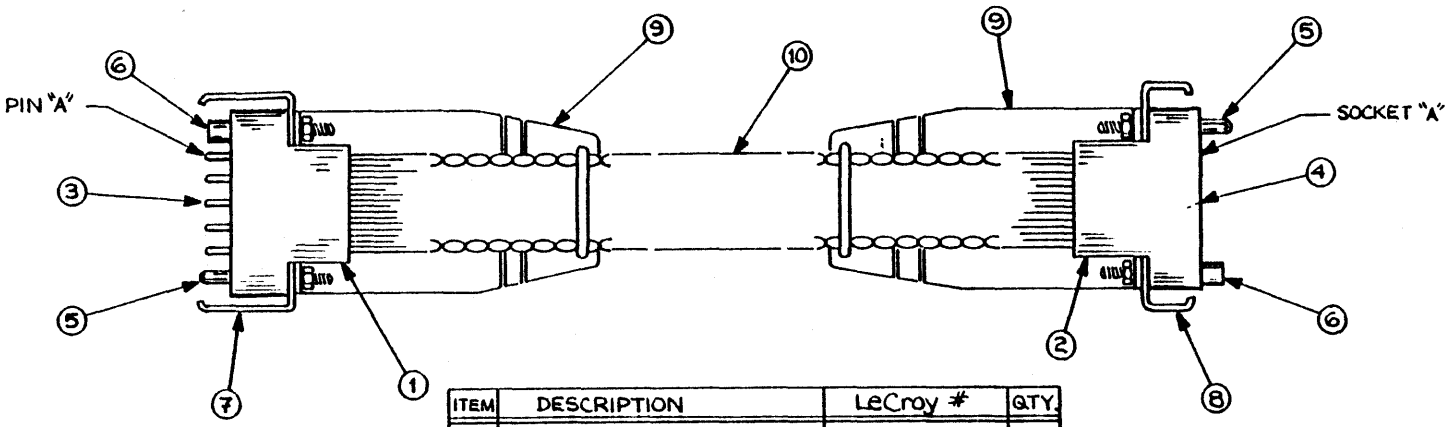




ITEM	DESCRIPTION	LeCroy #	QTY
1	CONNECTOR BLOCK	405-152-001	1
2	MALE CONNECTOR PIN	405-453-020	4
3	MALE LOCKING SPRING	405-721-002	2
4	MALE GUIDE PIN	405-232-004	1
5	FEMALE GUIDE PIN	405-332-003	1
6	WIRE, AWG # 22	———	A/R

TERMINATING CONNECTOR
HVTC-14

Figure 3.5



ITEM	DESCRIPTION	LeCroy #	QTY.
1	CONNECTOR BLOCK	405-152-001	1
2	CONNECTOR BLOCK	405-161-001	1
3	MALE CONN. PIN	405-453-020	14
4	FEMALE CONN. PIN	405-555-001	14
5	MALE GUIDE PIN	405-232-004	2
6	FEMALE GUIDE PIN	405-332-003	2
7	MALE LKG. SPRING	405-721-002	2
8	FEMALE LKG. SPRING	405-712-001	2
9	STRAIN RELIEF CLAMP	405-786-008	2
10	CABLE (7 PAIR)	592-120-014	100'

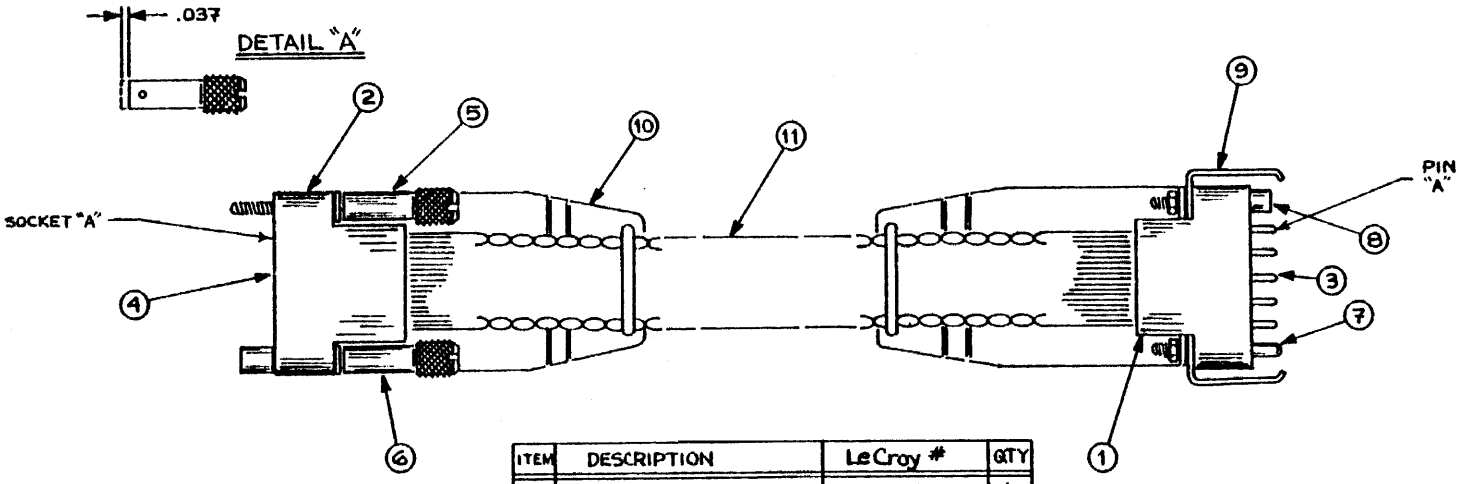
NOTES:

1) WIRE CABLE TO CORRESPONDING PINS (A TO A, B TO B, ETC.), USING WIRING CHART

PAIR	PIN	COLOR
1	A	BRN
	C	TAN
2	B	RED
	E	TAN
3	D	ORA
	F	TAN
4	H	YEL
	K	TAN
5	J	GRN
	M	TAN
6	L	BLU
	N	TAN
7	P	VIO
	R	TAN

CABLE ASSEMBLY
HVEX-14

Figure 3.6



ITEM	DESCRIPTION	LeCroy #	QTY
1	CONNECTOR BLOCK	405-152-001	1
2	CONNECTOR BLOCK	405-161-001	1
3	MALE CONN. PIN	405-453-020	14
4	FEMALE CONN. PIN	405-555-001	14
5	MALE JACKSCREW	405-240-005	1
6	FEMALE JACKSCREW	405-360-005	1
7	MALE GUIDE PIN	405-232-004	1
8	FEMALE GUIDE PIN	405-332-003	1
9	MALE LKG. SPRING	405-721-002	2
10	STRAIN RELIEF	405-786-008	2
11	CABLE, (7 PAIR)	592-120-014	1 FT.

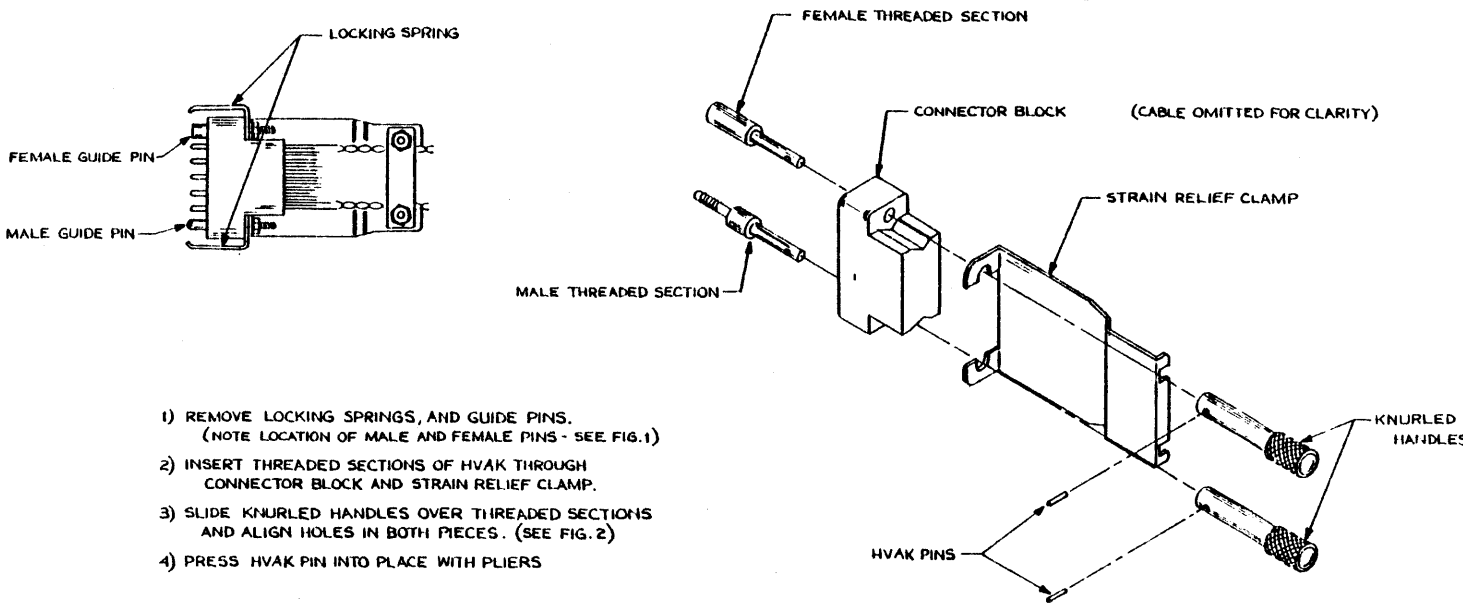
NOTES:

1) MILL JACKSCREWS AS SHOWN IN DETAIL "A".
2) WIRE CABLE TO CORRESPONDING PINS (A TO A, B TO B, ETC.), USING CHART BELOW

PAIR	PIN	COLOR
1	A	BRN
	C	TAN
2	B	RED
	E	TAN
3	D	ORA
	F	TAN
4	H	YEL
	K	TAN
5	J	GRN
	M	TAN
6	L	BLU
	N	TAN
7	P	VIO
	R	TAN

CABLE ASSEMBLY
HVAC-14

Figure 3.7



JACKSCREW ASSEMBLY
HVAK

Figure 3.8

External Controls Header
(Rear Panel View)

External Controls Header Connector Construction

Pin Configuration	Housing AMP Part Number
4-pin	4-87456-9
6-pin	4-87456-1
12-pin	4-87456-7
Wire Gauge	**Contacts AMP Part Number**
#20-24	4-86016-1
#22-26	4-87667-1
#26-30	4-86015-1
Shunt Jumper	**AMP Number 530153-2**

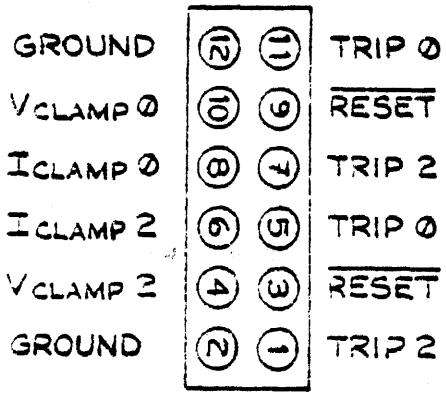


Figure 3.9

SECTION 4

TECHNICAL DISCUSSION

4.1 Introduction

The LeCroy Model HV4032A consists of up to 32 high voltage power supplies (HVPS) whose output voltages are set by digital values stored in a memory and applied to a 14-bit digital-to-analog converter (DAC). (See Figure 4.1). This system is one of the peripherals of the microprocessor in the HV4032A mainframe. The microprocessor allows numerous error and fault checks, programmed run-up and run-down of voltage, as well as digital feedback of the HVPS. A serial I/O port, as well as the front panel switches and front panel display, are additional peripherals to allow interaction with the user.

4.2 HVPS Plug-In Pods

Each channel of any pod type is a DC-to-DC converter, utilizing a constant frequency Pulse Width Modulated (PWM) switching regulator. The switch transistor "kicks" the primary circuit of the step-up transformer. The width of the drive pulse affects the sinusoidal voltage swing of the primary circuit which is symmetrical about the 40 V baseline. The secondary circuit of the transformer is capacitively tuned to be resonant at 62.5 KHz. The transformer provides voltage gain with a step-up turns ratio of 1:43. Additional gain is provided by either a voltage doubler or a voltage quadrupler, depending upon the pod type. The output of the voltage multiplier is smoothed by a multistage filter network.

Each HV output is monitored by two sense resistor networks. In 3.3 kV pods, a 400:1 divider is used by the local feedback loop to maintain the output at the value determined by the microprocessor. An additional sense resistor (30 MΩ in series with the rear panel calibration adjustment) is multiplexed to the HV4032A-2 Digital Board where the remainder of a buffered 400:1 voltage divider is located. This 30 MΩ resistor is used by the microprocessor to measure the HV output. For Series VII pods, an 800:1 divider and 60 MΩ sense resistors are used.

Under the microprocessor control, an analog control current is multiplexed to each of the eight pod slots within the mainframe. This current is converted to a control voltage reference in the pod and is then further multiplexed to each of the control circuits of the pod. 3.3 kV pods use the reference voltage for HV output voltage control only, while 7 kV pod channels use one reference voltage for HV output control and one for output stage current limiting. The multiplexed reference voltages are stored in an analog memory composed of a "hold" capacitor and a high impedance buffer amplifier. The applied control voltage for HV output is either 1/400th or 1/800th of the desired output voltage depending upon the pod type. The applied voltage for current control is 20 mV/μA. The output of

the buffer amplifier is diode connected to a limit voltage which is determined by the front panel HV LIMIT SET control.

The Series VII pods also offer rear panel nodes to allow the hardware limits (clamps) for both output voltage and current limit to be individually set. The per-channel output voltage clamp is mixed with the mainframe voltage clamp value using diode isolation at each channel. In this way, the more stringent of the two constraints is applicable to each channel.

The DC current out is monitored at its point of return to the high voltage multiplier and filter stages. In 3.3 kV pods, the current returns via a resistor from a reference voltage. When the voltage drop across a resistor exceeds a fixed threshold, a sensing transistor pulls on the tap of the 400:1 divider so as to simulate excessive output voltage as perceived by the error amplifier.

In Series VII pods, the return is via a precision current-to-voltage amplifier whose output is compared to the current limit reference voltage from the hold capacitor/external clamp combination by a separate error amp operating in parallel to the voltage error amp. The current drawn by the divider and 60 MΩ resistors is nulled out by introducing an equal current at the return point.

The error amplifier senses both control reference voltage input and the feedback sample of the high voltage output through the divider network. The amplifier integrates the difference between requested and produced output voltage. Its output finds the correct DC level to produce the desired high voltage output.

The HV4032A-2 Digital Board provides the necessary timing to generate a 62.5 KHz "Sync Pulse" to the pods. The pod uses the Sync Pulse to generate a ramp waveform with a duration of about 6 µsec for 3.3 kV pods and 4 µsec for Series VII. This ramp, in conjunction with a voltage comparator, allows the output of the error amplifier to control the PWM drive pulse to the switch transistor.

On Series VII pods, the DC current measurement is supplemented by a transient detector. The detector floats at the output potential, and is linked back to the low voltage control circuitry via an optocoupler. The standing current to the output and divider charges up a capacitor, clamped by a zener diode. This current also passes through a sensing resistor. An RC filter discriminates against DC and slowly rising currents. A rapid current increase of adequate duration turns on a transistor which uses the energy stored in the capacitor to flash the optocoupler's LED.

The optocoupler output is fed to the clock input of a flip-flop. If the clear input is not low (the Reset is not active), and the bi-directional TRIP bus has not been externally driven active, the flip-flop will set. This will drive the TRIP bus, disabling the PWM and activating a relay to discharge the HV filter capacitors and external cable capacitance. The flip-flop output will also inhibit driving the QUAD POD bus when the tripped channel is selected by the

digital board, indicating to the microprocessor that the channel has initiated the trip.

If the TRIP bus is activated via external connection from another channel, the PWM is disabled and the relay activated, but QUAD POD is unaffected and the flip-flop is inhibited from being set. The flip-flop can be cleared or inhibited by either sensing the turn-off of the 40 V DC supply (by turning HV off), or by pulling the external RESET input to ground.

To avoid surges at turn-on, the error amps and PWM on Series VII pods are biased, even with zero voltage demand and 40 V off. This is accomplished by adding a pedestal level to the control current input and maintaining the driver transistor collector supply (Vp) at about 2 V. The HV output will generate about 30 V.

4.3 HV4032A-2 Digital Board Introduction

The digital board houses an "F8" microprocessor set, micro-program storage PROMS (firmware), static random access memory (RAM), a recirculating data memory, timing generation, a 14-bit digital to analog converter (DAC), a 12-bit analog to digital converter (ADC) and the battery charge circuit. The input/output (I/O) ports of the microprocessor monitor and control all operation of the HV4032A.

The microprocessor controls the pod as follows. With HV OFF the 40 V DC supply is turned off as a guarantee that high voltage cannot be produced. The Sync Pulse is hardware generated and is normally free-running. When the HV ON switch is depressed the microprocessor turns on the 40 V DC supply and begins incrementing the control current causing the high voltage to ramp-up. When a certain "calculated control current" is reached, the microprocessor relies on the readings of the 30 or 60 MΩ resistor to do a fine adjustment of the high voltage output for each channel. HV turn-off causes a decrementing of the control current to 0 followed by a turn-off of the 40 V DC supply. When a Panic Off or Active Interlock condition occurs, immediate turn-off of the switching supply is guaranteed by the inhibiting of the Sync pulse input to the PWM. The microprocessor reacts as if a normal HV turn-off was requested.

4.3.1 Processing Voltage Demand

Twelve-bit voltage requests are received via the device selected (serial port or front panel). See figure 4.2. These values are written into a section of the random access memory (RAM) called the DEMAND BUFFER. The RAM is protected against power down by a battery backup. This 12-bit by 32-word array constitutes a set of user voltage demands which are saved whether or not the high voltage is ON. When the high voltage is OFF, writing a word into memory affects the output voltage of that channel only after the high voltage is turned ON.

4.3.2 High Voltage Control

When the high voltage is ON, 14-bit data derived from the DEMAND BUFFER section of the Data Memory are loaded into a data circulator buffer as shown in Figure 4.2. These values are applied to the DAC and the resultant output voltage programming level is multiplexed to the 32 HVPS, as a control current refreshing their analog memories every 512 μsec. The data circulator operates under hardware control in order to leave the microprocessor free to perform other functions.

Simultaneous with the refresh operation, the calibrated HV output sense resistor is multiplexed to the ADC front end circuit. The sense resistor of negative output pods acts as a current sink, causing the feedback resistor of the inverting amplifier to develop a positive voltage that is either 1/400th or 1/800th of the high voltage output monitored, depending upon the pod type. 7 kV pods produce a current sink proportional to output stage current when the odd channel (current subaddress) is addressed to allow the microprocessor to read output current. The sense resistor in positive output pods can be read by the ADC circuits in the same way as negative pods.

The output of the inverting buffer amplifier is monitored by a sample-and-hold amplifier which, in conjunction with the ADC, is controlled by the microprocessor. The ADC is a twelve-bit successive approximation type. Sixteen samples of each channel are averaged to minimize uncertainty caused by least-significant-bit of the ADC and noise from transients. All 32 channel locations are sampled and averaged approximately every 300 msec. For voltage control channels the microprocessor compares the sensed reading to the DEMAND BUFFER value. If a difference is detected an adjustment is made to the 32 word fourteen-bit section of memory designated the DAC BUFFER and these adjusted values subsequently replace the 32 words in the recirculating data buffer. For 3.3 kV pods an adjustment of plus or minus 250 mV of actual high voltage output will be made. 7 kV pod voltage programming is adjustable in plus or minus 500 mV increments while current programming may be adjusted in 1 μA steps. This system assures a long-term stability of plus or minus 0.5 V for 3.3 kV pods and 1.0 V for 7 kV pods. If an over voltage situation of greater than 4 or 8 V for 3.3 or 7 kV channels respectively is detected, the entire error will be reduced in a single correction cycle - avoiding a long term over voltage condition.

4.4 Error Detection

Normal scanning in the digital regulation mode will reveal any failed 3.3 kV channels by detecting a $\geq$64 V difference between average ADC value and DEMAND BUFFER value for that channel. This can be caused by a failure of the HVPS, an over current ($\geq$2.5 mA) due to faulty load, or action of the manual HV LIMIT SET potentiometer which protects against user error. When such a fault is detected, the DAC buffer voltage is run-down at 1 kV/sec. The demand buffer value is transferred to the TEMPORARY DEMAND BUFFER (see Figure 4.2), the

DEMAND BUFFER is zeroed, and a failed channel flag is set in memory with an indication given at the active user peripheral. For 7 kV pods a voltage difference of $\geq$128 V will cause a failed channel response and run-down at 2 kV/sec.

If the unit is in the LOCAL MODE, the failed channel number and the measured voltage at the time of the failure are flashed on the front panel display. The voltage display will then show "9999" indicating that the channel has been automatically zeroed as described above. If more than one channel has failed, the display will then flash the next detected failure and repeat the zeroing process for the indicated channel.

If the unit is in the Remote Mode in use with a TTY, an indication

```
  MXX
*CHYY
```

is given to indicate channel YY of mainframe XX has failed. A bell response is given, but no user response is required.

In Remote Mode with the CAMAC 2132 module, the CPU sends a Set High Priority LAM command to the 2132 and the failed channel number and its mainframe number are written into a buffer memory in the CAMAC module.

A channel failure may be the result of a failure of an HVPS to regulate itself. In that unlikely case, zeroing of the DAC buffer may not zero the output voltage. In most failure modes, however, the HV LIMIT SET control will perform its limiting function.

The microprocessor goes into an Low Voltage Power Supply (LVPS) error routine if the 40 V power source for the HVPS goes out of regulation (exceeding 44 V), the 10 A picofuse within the LVPS blows or it the temperature sensor detects a 40 V output transistor case temperature exceeding 90°C. In this case, the DAC buffer values are ramped to 0 as in HV TURN-OFF and a failure indication is given. In Local Mode, a display of 6666 is loaded and flashed. In Remote Mode, no error message is sent. In either case, the high voltage is shut off. The mainframe is nonresponsive to the front panel controls or to the serial port until AC power is cycled.

4.5 Turn-On/Programmed Run-Up

Pushing the HV ON switch performs two functions:

1. A 40 V DC regulated supply is enabled at the inputs of all HVPS (common bus to all pod HV supplies).

2. A programmed run-up if the high voltage is initialized.

Programmed run-up and run-down are employed to minimize the effects of transients on the load.

In the Local Mode, the HV ON/OFF bit as programmed by the HV ON/OFF switch is continuously interrogated. When it is set to ON (Local Mode only) or when an HV ON command is received at the Serial Port, (Remote Mode only), a run-up is begun.

The up to 32 DAC BUFFER voltage programming values are incremented in steps of 32 V or 64 V for 7 kV channels. This brings all channels to voltage at a safe rate of 1 kV/sec or 2 kV/sec for 7 kV channels. Incrementing of each channel is terminated when the DAC BUFFER value is within 16 V of the DEMAND BUFFER value or 32 V for 7 kV channels. When the last channel has reached a DAC value within 16 or 32 V of the DEMAND voltage, a fine tuning is performed. Here the voltage as measured by the ADC is compared with the DEMAND voltage and the up to 32 DAC BUFFER values are adjusted in 1 or 2 volt steps. The current limit programming for 7 kV channels is not ramped up; the desired value is immediately loaded.

When the ADC value equals the demand voltage for each channel, the Digital Regulation Mode goes into effect as described in Section 4.3.2. Complete run-up requires approximately 20 seconds, assuring slow run-up to the DEMAND values without overshoot. If a run-up is being performed in the Local Mode, the HV4032A will respond to no commands except Panic Off or Interlock until run-up is complete. The daisy chain communication to the other modules is not blocked.

In response to HV OFF, the up to 32 words of DAC BUFFER voltage programming are decremented in 32 V or 64 V steps, depending upon pod type, to 0 V. This operation is complementary to run-up, causing a 1 kV/sec response for 3.3 kV pods and a 2 kV/sec response for 7 kV pods.

In the event of a power failure (AC failure or power turn-off) the high voltage at the output of each 3.3 kV HVPS will approach zero V with a time constant of .05 seconds per MΩ of external load. The INTERLOCK (front panel BNC), or PANIC OFF will turn-off the HV power supplies causing the high voltage outputs to approach 0 V at the same rate of .05 seconds per MΩ of external load.

4.6 Zero/Restore

To zero a channel, one word of data is transferred from the DEMAND BUFFER to the TEMPORARY DEMAND BUFFER. The DEMAND BUFFER data word is set to zero and the channel is run-down at the same rate that applies for HV turn-off.

To restore a channel, the complementing sequence is followed. The value in the TEMPORARY DEMAND BUFFER is transferred to the DEMAND BUFFER and the channel is run-up at the rate that applies for HV turn-on. The restore command clears, at the same time, any failed channel or error condition pertaining to the addressed channel voltage. The TEMPORARY DEMAND BUFFER value will always be updated to the same value as in the DEMAND BUFFER except the time that a channel is zeroed.

Note: Zero/Restore operation is not valid for 7 kV current limit programming. A zeroed or failed 7 kV channel will maintain its current limit programming.

4.7 Power On/Off Control

Upon power down, the microprocessor can perform a shut down routine before fully losing power. The following operations are performed:

1. The status of the line switch is written into RAM in order to distinguish between power failure and shut down.

2. The status of the high voltage (on/off) is recorded.

3. The battery back-up takes over to preserve the data in RAM.

Two nickel cadmium 1.2 volt cells (Eveready CH-35 'C' cell) are used to maintain the contents of memory. When the batteries are fully charged, they provide a 24-hour back-up. In normal powered up operation, the batteries are charged at a rate to attain full charge in 48 hours. Upon power up, a set of check bits are read by the CPU and compared to a corresponding set in PROM. If they are identical, it is assumed that the battery back-up has maintained valid data in memory. The check bits are overwritten in preparation for the next power down.

If the status bits test is failed, the microprocessor sets all data to zero, sets the HV status to OFF and loads the display to read:

33 1500 or 70 3500

depending upon the pod types installed in the mainframe.

If the status bits test is passed and power down was due to a power failure, the HV4032A will revert to its former status. If the unit was in an HV ON mode, a controlled run-up is performed as described in Section 4.5.

If the status bit test is passed and power down was caused by the line switch, the HV4032A will maintain the values loaded into the DEMAND BUFFER, set its HV status to OFF, and load CH 00: 00xx V into the display. Depressing the High Voltage On switch will cause the unit to return to its previously set voltage levels.

4.8 User Controlled Microprocessor I/O Ports

The following ports are connected directly to the front panel:

Output Ports:

Channel and Voltage Displays:
4 BCD data bits, 3 address bits and a strobe are decoded on the front panel board controlling:

Channel Number Display:
Indicates the channel number to be monitored or changed.

Voltage Display:
Normally indicates averaged ADC readings of HV outputs. If VOLTAGE switch is pressed, displays demand value for the indicated channel. Also displays 7 kV channel current and current limit programming.

Input Ports:

The following bits of the I/O port are polled only in the Local mode and, therefore, are ignored in the Remote mode.

Voltage/Channel:
2 bits to select mode of INCREASE/DECREASE switches.

Decrease/Increase:
2 bits; changes variable selected by VOLTAGE/CHANNEL switches.

Zero/Restore:
2 bits; sets displayed channel voltage to zero or demand voltage. Since this action zeroes the DEMAND BUFFER and loads the TEMPORARY DEMAND BUFFER, this feature is active even with HV OFF.

HV ON/OFF:
These switches control a set-reset flip-flop. The flip-flop latches the request for a change in HV status and presents it to the I/O port.

The following are each one bit on the I/O port and are polled in either Local or Remote modes:

Remote/Local:
Selects user peripheral; front panel or serial port.

HV Trip:
Actuated by either PANIC OFF or INTERLOCK. Latched output from front panel instructs microprocessor to turn HV OFF. Latch reset by microprocessor upon turn-off.

Address Switches:
4 bits on the I/O port constantly monitored.

Power On Switch:
A three-pole single-throw switch to switch both sides of the AC line and also provide a third pole to act as a single bit on the I/O port polled only at power-down.

The following ports determine Remote mode operation:

CAMAC Mode:

Front panel board receiver monitors the High Voltage Serial Bus (HVSB) to operate in CAMAC or TTY mode. Constantly monitored during Remote operation.

TTY Baud Rate:
Jumper plug on digital board determines 110 or 300 baud communication with TTY. Read once on power up.

Interrupts:
Power Down-
Interrupts the microprocessor to initiate power-down sequence. See Section 4.7.

Serial Port-
(J1 and J2) for daisy chain connection to controller. Disabled in Local Mode operation.

Internal Timer-
60 seconds; abort command not completed within interval. Remote mode only. (Timer is by-passed when system address commands are used; i.e. M(0).)

4.9 System Interconnection

Mainframes of the Model HV4032A are connected via a 5 pair daisy-chained bus (HVSB). The interconnection is shown schematically in Figure 4.4. All signals are buffered at each mainframe. The HVSB utilizes current loop interfaces. The functions of the 5 pairs are described below. As a convention, the sense of signals propagating away from the controller is referred to as 'upstream.'

Serial Out: Used to transmit data from the controller to the HV4032A mainframes. Data on this pair are seen by all mainframes and are actually re-transmitted by each mainframe. 20 mA unipolar current loop.

R.I., R.O. lines of HV4032A.

Serial In: Used to transmit data from the HV4032A mainframes to the controller. Data transmitted by a Model HV4032A are actively retransmitted by the downstream mainframe. 20 mA unipolar current loop.

T.I., T.O. lines of HV4032A.

Contr. ID: Allows the HV4032A to distinguish between TTY and CAMAC controllers. This pair is shorted for operation with the CAMAC Model 2132 (2400 BAUD) and open for TTY operation (110 or 300 BAUD). 20 mA unipolar current loop.

BDI, BDO lines of HV4032A.

Sense: A request by one of the mainframes for use of the

bus. 27 mA differential current loop.

Acknowledge: A request granted. This signal is a response to SENSE described above. 27 mA differential current loop.

4.10 Hand-Shaking Sequence to Achieve Control of HVSB

Quiescent conditions - no mainframe requesting bus control.

Sense (J17-23): This line is an I/O port to the microprocessor. If mainframe is assigned address 16, the microprocessor sets sense to ØV. For any other mainframe assignment, this line will be in the HI impedance state at +5 V. A +5 V level indicates than an upstream mainframe is requesting bus control and would prevent the mainframe from requesting bus control until the sense returned to ØV. This is done by the open collector OR function at the output of the SI line receiver such that ØV sense line on M16 will propagate through each mainframe, indicating that no mainframe is requesting bus control.

Bus Request (J17-11): Normally 0 V; microprocessor output.

Disable (J17-14): Normally +5 V; microprocessor output.

Ack (J17-25): Normally 0 V; microprocessor input.

The following sequence must occur within 1 minute, otherwise the attempt to gain bus control is aborted:

1. Microprocessor checks for sense = 0 V.

2. Microprocessor sets bus request to +5 V. This propagates to downstream mainframes as a sense = +5 V preventing any other downstream mainframe from requesting bus control.

3. The return of the sense to the acknowledge lines at either the HVTT-14 or the 2132 causes an acknowledge to propagate upstream.

4. When an acknowledge high level is received by a mainframe which has issued a request, it sets its Disable (DIS) to 0 V to 0 V, blocking upstream acknowledge transitions to other units. The mainframe now has control over the bus and can, therefore, transmit to the controller via Serial In.

   The priority structure associated with the HVSB is positional. Higher priority is assigned to those units which are closer to the controller.

Data are transmitted from the TTY on SERIAL OUT lines. The data format is:

MXX COMMAND

The letter M and address XX are echoed by the last unit in the daisy-chain. M16 requests and is granted bus control before transmitting the echo back. M16 then releases its bus control so that the addressed mainframe can achieve bus control to echo back the command statement. The M16 mainframe, after releasing the bus, makes a single attempt at gaining bus control again. If it receives an acknowledge then it is assumed that no mainframe recognized the address and M16 echoes back a carriage return, line feed, and the "DOT." If a downstream mainframe has been validly addressed, it would prevent M16 from gaining bus control and normal echo back from the specified mainframe would result.

Operation in the CAMAC Mode is identical but without the echo provision.

4.11 HV4032A-3 - Low Voltage Power

The LVPS develops +15 V, -15 V, +12 V and -5. Two +5 supplies are used. +5 (DIG) is for general use within the mainframe while +5 (HV) is used only by the HV pods. A 40 V DC supply capable of 8 Amps is controlled by the microprocessor. All supplies except the 40 V are current limited. The 40 V supply is protected by a 10A pico fuse located on the PC board. In addition, the AC input to the 40 V supply is protected by two in-line fuses before entering the PC board.

The 40 V supply incorporates both an over-temperature sensor and over-voltage sensing. The temperature sensor is affixed to the heat sink and will trip if the 40 V regulator's pass transistors case temperature reaches about 90°C. If the regulator's output voltage exceeds about 44 V the over-voltage sensor will trip. Either of these error indications will disable the 40 V DC regulator and send a LOCAL SHUTDOWN signal to the microprocessor.

The supply buffers the front panel HV LIMIT SET potentiometer and provides a low impedance output limit voltage which is bussed to all pod locations. A threshold detector monitoring the unregulated feed to the plus 5 V regulators senses the removal of AC power and signals the microprocessor to go into it's power down routine before all supply voltages are lost. The LVPS passes the POWER FAIL line from the front panel AC power switch to the digital

The over-voltage sensor on the 40 V supply senses the voltage before the 10 Amp pico fuse such that if the fuse blows a LOCAL SHUTDOWN situation occurs. The ±15 V regulators are tied together such that if either goes out of regulation (due to a short circuit or current limiting) the other supply is also shut down. This is a safety feature to prevent uncontrolled HV should one supply fail.

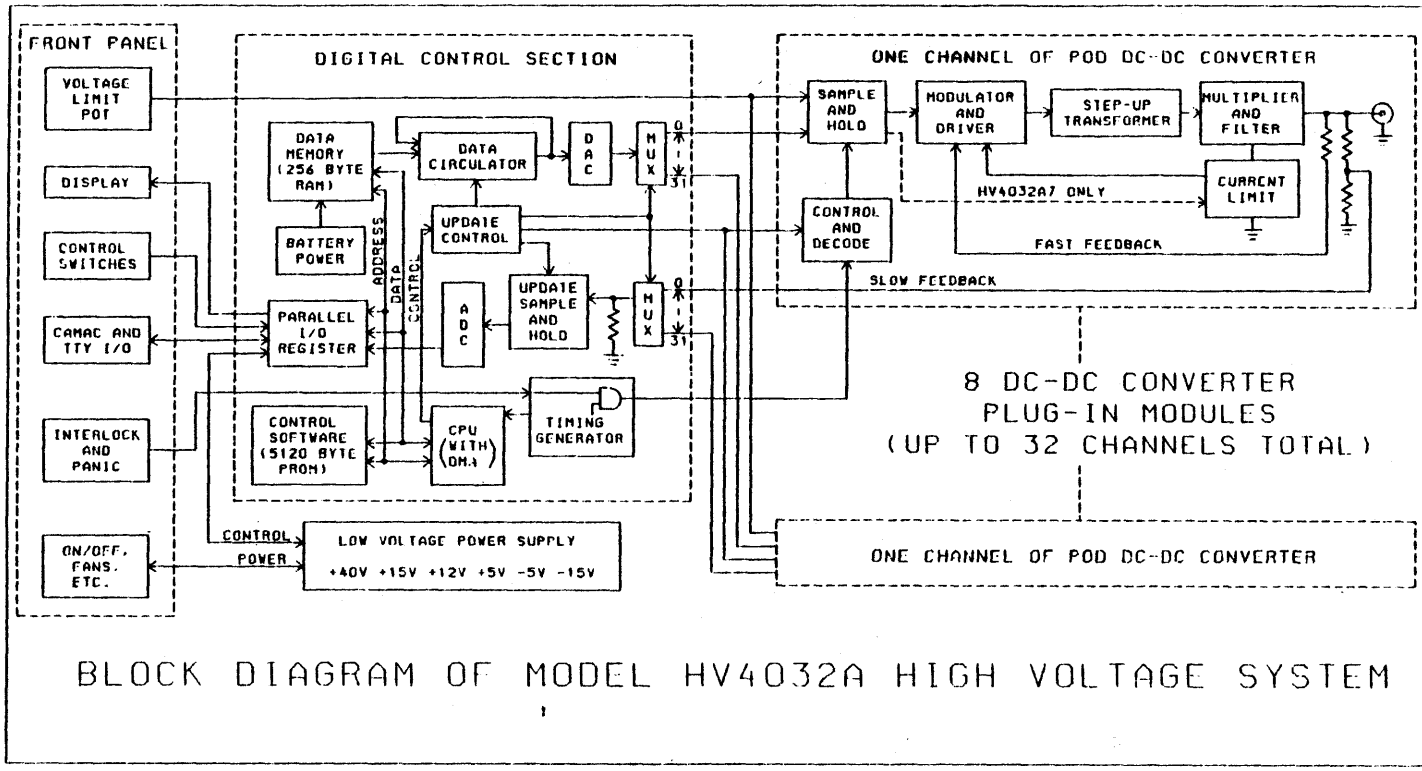
4.12 HV4032A-4 - Front Panel Board

The front panel board provides mounting and signal connections between the front panel and the microprocessor on the digital board. Buffering for the lamp indicators and other outputs is provided. The 7 segment LED display drivers and latches receive multiplexed data that is strobed into the appropriate digit latch by a decoder. The MSD of the Voltage Display is not latched but is directly displaying the data from an I/O port of the microprocessor.

The Front Panel HV Status latch (FPHVS) follows the HV ON and OFF switches in the local mode. In the Remote mode this latch is forced to the correct state upon receipt of a HV ON or OFF command. Upon initial power up the microprocessor initializes the latch by momentarily setting the Local/Remote I/O bit to the Remote state.

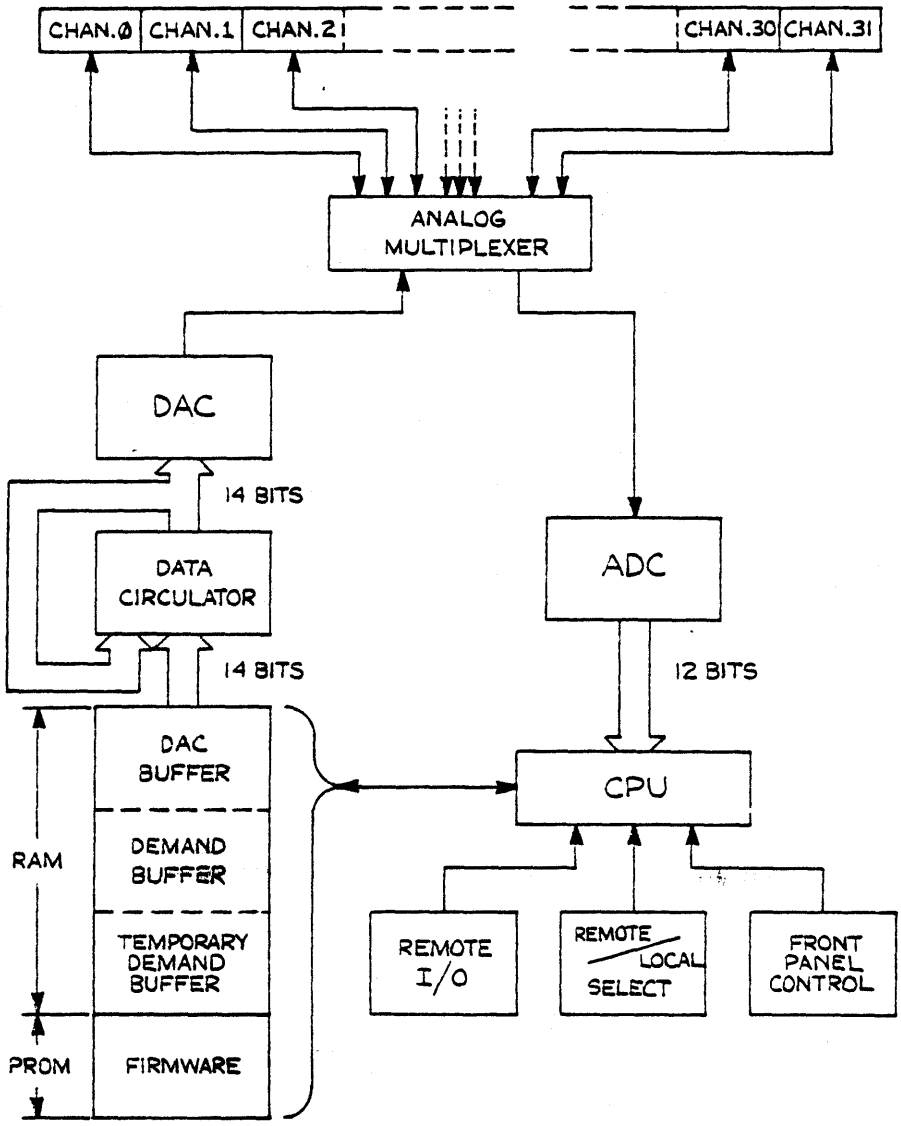
The Interlock and Panic Off controls are also latched on the front panel board producing the "Trip" signal to the microprocessor. Once the "Trip" is acted upon by the microprocessor it resets the Trip latch until the Trip condition is cleared.

The 20 mA unipolar current loop interfaces supply loop current at their J1 connections and are passive current sensors or floating switch closures at the J2 connections. The hardware is such that received serial data is re-transmitted even though the mainframe is in Local mode.



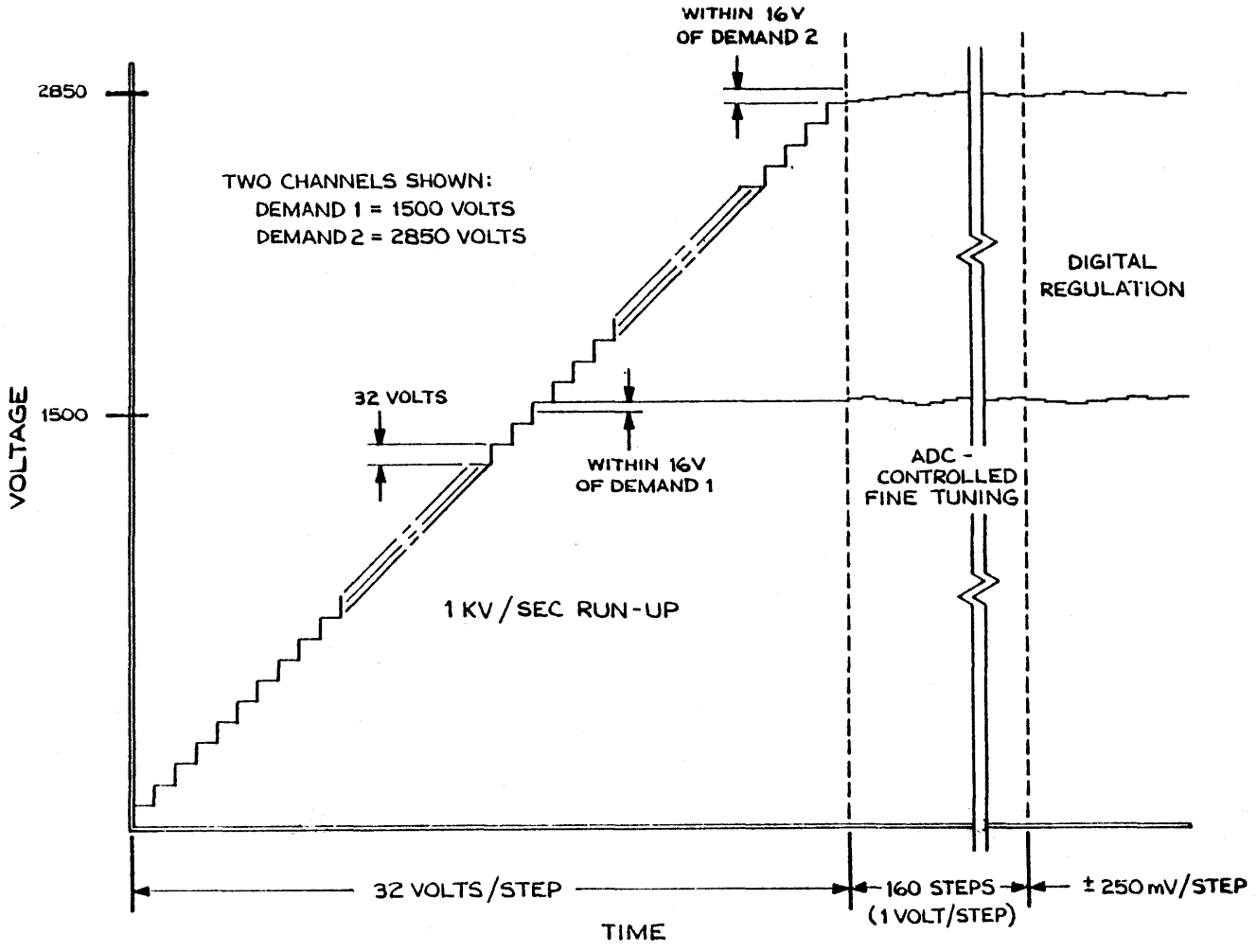
BLOCK DIAGRAM OF MODEL HV4032A HIGH VOLTAGE SYSTEM

Figure 4.1



HIGH VOLTAGE CONTROL

Figure 4.2



HV4032A: REPRESENTATION OF HIGH VOLTAGE RUN-UP FOR TWO 3.3KV CHANNELS

Figure 4.3

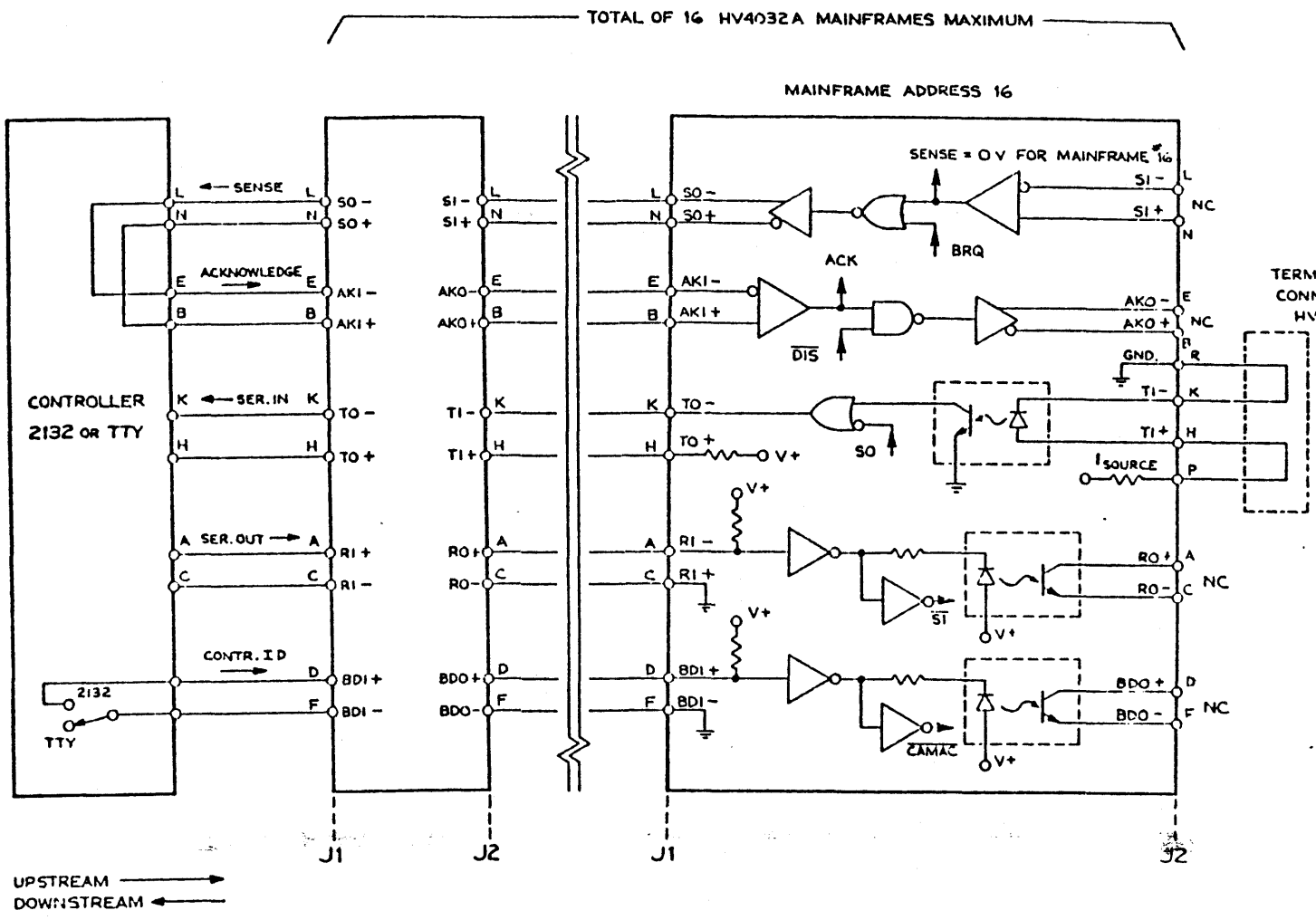

TOTAL OF 16 HV4032A MAINFRAMES MAXIMUM
MAINFRAME ADDRESS 16
SENSE = 0 V FOR MAINFRAME #16
CONTROLLER
2132 OR TTY
SENSE
ACKNOWLEDGE
SER. IN
SER. OUT
CONTR. ID
2132
TTY
SO -
SO +
AKI -
AKI +
TO -
TO +
RI +
RI -
BDI +
BDI -
SI -
SI +
AKO -
AKO +
TI -
TI +
RO +
RO -
BDO +
BDO -
BRQ
ACK
DIS
SO
V+
CAMAC
GND.
NC
J1
J2
UPSTREAM
DOWNSTREAM

Figure 4.4

SECTION 5

SERVICE/PARTS REPLACEMENT

5.1 The HV4032A is modularized to allow service by substitution. Replacement components are as follows:

HV4032A1N and HV4032A1P

Quad plug in negative and positive pods respectively. These supplies may be removed from the rear of the HV4032A without removing the mainframe from the rack. The AC POWER MUST BE OFF to avoid damage to the mainframe or the HV4032A1 module. To remove, pull the two nylon quick disconnect latches and extract the module. Unless channel Demand Voltages are zeroed, empty channels will respond as failed.

HV4032A7N and HV4032A7P

Dual plug in negative and positive 7 kV pods respectively.

HV4032A-2

Digital Board containing the microprocessor, I/O ports, memory, ADC and DAC. This board can be accessed after removing the top cover. It is mounted horizontally in the front half of the chassis. To remove the Digital Board, disconnect the flat cable from J17. This cable connects the HV4032A-2 to the front panel board, HV4032A-4. Release the two nylon quick disconnect latches located at the front corners of the board, lift the board and disconnect the remaining flat cable from connector J3. The HV4032A-2 can be removed by unscrewing the hinged standoffs from the distribution board bracket.

CAUTION - When reinstalling, exercise care in aligning the pins of J17 and J3 with the connectors. It is easy to inadvertently install them with improper registration.

NOTE: The HV4032A-2 is mounted such that the board may be swung upward with all cable assemblies installed. This facilitates trouble shooting from both sides of the board while the unit is operating within the mainframe.

HV4032A-3

Low voltage Power Supply: Lift the HV4032A-2 Digital Board as above. Disconnect the Molex-type connector at J14. This is located on the left side of the HV4032A-3 board and connects the transformer to the Supply. Unscrew two captive screws: one at the top rear of the LVPS, and the other at the bottom front of the board. Unplug the board from the rear edge connector and rotate it 90° CCW. It can now be lifted out of the chassis.

HV4032A-4

Front Panel Board: Follow the above procedure and remove the HV4032A-3 LVPS. Remove the eight 4-40 screws securing the front panel board to the HV4032A Front Panel. Gently pull rearward on the Front Panel Board until the switches are free of the front panel cutouts and the board perimeter has cleared the fan shrouds. The four flat cable DIP connector assemblies may be removed and then the board is free of the mainframe. Note: These connector cables are of sufficient length to allow the board to be gently mounted at the top of the front panel to provide easy access to both sides of the board. Effective trouble shooting may be done while the board is operating within the mainframe.

SECTION 6

REMOTE CONTROL OF HV4032A AND HV4032 FAMILY MAINFRAMES

6.1 General Information

The HV4032A utilizes the same communication structure that was established by the HV4032 family mainframes. The 5 pair daisy chained bus (HVSB) for the HV4032 mainframes maintains the signal pair pinouts, logic convention and interpretation of the older units.

It is possible to configure a system containing one controller and up to 16 mainframes. These mainframes may be any combination of HV4032, HV4032H, HV4032P or HV4032A units.

The differences between the two systems are minor. The daisy chain cable for the HV4032A utilizes different retention hardware at the cable ends. The mainframe addressing has been limited to the usable limit of 16 mainframes. The HV4032A allows use of a less tedious TTY mode command structure. Schematic drawings and other documentation for the HV4032A have adhered to the positive logic convention in an effort to make them easier to understand. When comparing schematics for the HV4032 and the HV4032A what may seem to be differences are most likely labeling or logic symbol corrections. The 4032A INTERLOCK is edge triggered while the 4032 GATE is sensitive to a level. If these two types of inputs are daisy chained, all mainframes will turn high voltage off when the INTERLOCK/GATE line is pulled low. However, only the 4032 units will turn HV back on immediately when that line goes high.

6.2 Mixed Family System Interconnection

Cabling a mix of mainframe types should follow the scheme established in Section 3.4.1 To cope with the differences in retention hardware now supplied with the interconnection accessories and on the front panels of both the HV4032A and the 2132 certain adapter kits are available.

If an existing HV4032 daisy chain is being expanded with HV4032A mainframes the following approach may be taken. Order one HVDC-14-L for each of the HV4032A mainframes. The HVTC-14 originally used can be easily modified to terminate the last HV4032A by swapping retention hardware with one of a new style HVDC-14-L. The jack screws of the HVTC-14 are removed by pushing the pin through the jack screw. Be careful to maintain the same sexes of guide pins and jack screws as they are interchanged. Remove the guide pins and locking springs from one end of the HVDC-14-L. These guide pins and locking springs from one end of the HVDC-14-L. These guide pins can be installed on the HVTC-14 connector block creating a terminator that will plug into the J2 connector of the last HV4032A in the chain. The jack screws originally on the HVTC-14 are then installed on the end of the HVDC-14 which can then be connected between the last HV4032 and the first HV4032A.

If a spare HVDC-14 of the old style is available, the HVAC-14 will adapt this cable to the HV4032A front panel. A new style HVTC-14 may also be ordered.

The HVAK kit provides the jack screws to convert one end of the new style HVDC-14-L cable to connect to the old style front panels.

6.3 Operating the Mixed Family Remote Control

a. For TTY operation the HV4032A mainframes must be toward the end of the daisy chain (on the upstream side) in order to utilize the shorthand allowing the selection of mainframes without always respecifying the mainframe address with a M## command.

b. The HV4032A Family uses mainframe address 16 to terminate the daisy chain. The terminus mainframe number for the HV4032 family is 63. ONLY ONE TERMINUS MAINFRAME ADDRESS MAY BE ASSIGNED IN THE SYSTEM. It is suggested that a HV4032A with a mainframe address of 16 terminate the daisy chain and that no HV4032 be assigned address 63. If a HV4032 must terminate the daisy chain then it should be address 63 and no HV4032A should be assigned as mainframe 16.

c. For TTY operation, verify the baud rate programming of mainframes to be certain that the entire system is operating at a common baud rate. HV4032A mainframes are factory set to operate at 110 baud. If possible, it is suggested that 300 baud be selected for system operation.

TECHNICAL INFORMATION

(PARTS LIST, SCHEMATICS)

PART NUMBER	DESCRIPTION REMARK	QTY PER
377011000	LABEL "DANGER ---- VAPOR"	1
377011005	LABEL: "CAUTION HAZ VOLT"	1
403010040	CONN KIT FLAT CABL 40-PIN	4
485021001	BUMPER W/BRASS INSERT BLK	1
512041013	COVER BOTTOM HV MAIN ASSY	1
512241011	TOP COVER "A" (FRONT)	1
512241012	TOP COVER "B" (REAR)	1
512241027	SIDE PANEL(RIGHT) HV4032A	1
512241030	BRACKET (REAR PANEL)	2
512241031	BRACKET DIGITAL BD CENTER	1
512241102	BRACKET DIGTAL BD SUPPORT	1
512241182	GUARD RAIL (BOTTOM SKID)	2
521400012	SPACER ROUND #4 3/8	2
521400020	SPACER ROUND #4 5/8	2
530301002	HANDLE ROUND 5/16 DIA 4"	1
530309004	BOX SLIDES (PR) 20" LOCKG	1
555892024	SCREW FL BRISTOL HD 8-32	4
560032008	SCREW PHILIPS 10-32X1/2	10
560440003	SCREW PHILIPS 4-40X3/16	4
560440004	SCREW PHILIPS 4-40X1/4	16
560440005	SCREW PHILIPS 4-40X5/16	35
560440006	SCREW PHILIPS 4-40X3/8	14
560440007	SCREW PHILIPS 4-40X7/16	3
560440008	SCREW PHILIPS 4-40X1/2	5
560440010	SCREW PHILIPS 4-40X5/8	16
560440016	SCREW PHILIPS 4-40X1"	8
560632006	SCREW PHILIPS 6-32X3/8	15
560832006	SCREW PHILIPS 8-32X3/8	4
567440004	SCREW FLAT PHIL 4-40X1/4	2
567632007	SCREW FLAT PHIL 6-32X7/16	6
575410002	WASHER FLAT SS .250 OD #4	53
576010001	WASHER SPLIT LOCK SIZE 10	10
576410001	WASHER SPLIT LOCK SIZE 4	98
576610001	WASHER SPLIT LOCK SIZE 6	11
576810001	WASHER SPLIT LOCK SIZE 8	4
580006001	NUT HEX 10-32	1
580440001	NUT HEX STANDARD 4-40	28
592030040	CABLE FLAT AWG 28 40-COND	0
594240001	CLAMP CABLE HALF 1/4" DIA	1
597403201	SHIPPING CARTON 4032	1
597403202	SHIPPING CARTON END CAP 4032	2
597403203	SHIPPING SLEEVE 4032	1
704032103	LATCHING STRIP LO VOLT BD	1
HV4032A-2B	HV CONTROLLER BOARD	1
HV4032A-3	LOW VOLTAGE POWER SU	1
HV4032A-4	HV FRONT PANEL BOARD	1
HV4032A-5	MECH SUBASS'Y HV4032A-5	1
HV4032A-6	PC BD SUBASS'Y HV4032A-6	1
HV4032A-8	FR PNL SUBASS'Y HV4032A-8	1

End of report. 49 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
102412068	CAP CERA DISC 100V 6.8 PF	1
103317222	CAP CERA MONO 50V 2200 PF	1
103427104	CAP CERA MONO 100V .1 UF	2
106425103	CAP CERA MONO .01UF	50
141838335	CAP TANT DIP REEL 3.3UF	20
142824685	CAP TANT DIP CASE 6.8 UF	1
161225101	RES CARBON FILM 100 OHMS	2
161225102	RES CARBON FILM 1 K	1
161225103	RES CARBON FILM 10 K	19
161225105	RES CARBON FILM 1 MEG	1
161225153	RES CARBON FILM 15 K	2
161225221	RES CARBON FILM 220 OHMS	2
161225244	RES CARBON FILM 240 K	1
161225274	RES CARBON FILM 270 K	2
161225391	RES CARBON FILM 390 OHMS	1
161225395	RES CARBON FILM 3.9 MEG	2
161225473	RES CARBON FILM 47 K	1
161225512	RES CARBON FILM 5.1 K	2
161225753	RES CARBON FILM 75 K	1
168031571	RES PREC "UAR" TYP 71.5 K	1
168531393	RES PREC RN55D 1.00 K	1
168531410	RES PREC RN55D 1.50 K	1
168531417	RES PREC RN55D 1.78 K	1
168531513	RES PREC RN55D 17.8 K	1
168531529	RES PREC RN55D 26.1 K	1
168531573	RES PREC RN55D 75.0 K	2
181447103	RES VARI CERMET 10 K	4
190042103	RESISTOR NETWORK 10 K	7
190042221	RESISTOR NETWORK 220 OHMS	6
200031046	IC HEX INVERTER SN74LS04N	1
200031101	IC BIN COUNTER SN74LS393N	1
200071373	IC D-TYP LATCH 74LS373N	2
200071645	IC BUS TRANSCVR SN74LS645	1
200301401	DIODE ARRAY SWITCH DAN401	2
200302401	DIODE ARRAY SWITCH DAP401	2
200331074	IC D-TYP FLOP 74HCT74	2
200331108	IC 2-INPUT AND GATE 74HCT08N	1
200372374	IC 8-BIT REGIST 74LS374	6
200570688	IC 8-BIT COMPARATR LS688	1
205270256	IC 32K X 8 RAM 62256	2
205370001	IC CMOS UV EPROM 27C256	2
205782210	IC PAL 22V10 DO NOT INCLUDE ON KIT, GIVE TO PROGRAMMING CENTER FOR PROGRAMMING.	2
207170541	IC BUFF/LINE DRIV 74LS541	2
207294201	IC 16-BIT SAMPLING ADC ADC4201	1
207340408	IC 8-CH ANALOG MPLX DG408	1
207480543	IC REGISTR TRANSCVR F543	6
208011006	IC SINGLE OP AMP LM318N	1
208011010	IC PMOS ANALOG SW TL604CP	2

PART NUMBER	DESCRIPTION REMARK	QTY PER
208130347	IC QUAD JFET OP AMP LF347	1
208211002	IC VOLT REF REF-02DP	1
208541210	IC NONVOL CONTROLLER 1210	1
209129001	IC 16-BIT D/A CONV DAC70	1
227790030	IC SERIAL COM CONTROLLER Z85C30	1
229020055	TRANS VOLT SUPPR P6KE6.8	2
230110005	DIODE SWITCHING 1N4448	3
235010005	DIODE RECTIFIER 1N4005	2
280170306	TRANSISTOR FET N VN1306N3	1
300050001	CHOKE FERRITE SINGLE LEAD	1
309041032	CRYSTAL OSCILLATOR 32 MHZ	1
312682430	BATTERY LITHIUM 3V	1
313080105	BATTERY HOLDER	1
400031016	SOCKET IC SOLD TAIL DIP-16	1
400040024	SOCKET IC SOLD TAIL DIP-24	1
400041024	SOCKET IC SOLD TAIL DIP-24	2
400061040	SOCKET IC SOLD TAIL DIP-40	1
400360028	SOCKET IC SOLD TAIL DIP-28	2
400419068	IC SOCKET GRID TYPE 68-PIN	1
403111040	HEADER ASSEMBLY 40-PIN	2
403181003	HDR SINGL ROW 3	2
403980002	SHUNT ASSEMBLY 2-POS	2
454311002	HDR SOLD TAIL/MALE 2	6
454311005	HDR SOLD TAIL/MALE 5	1
454312010	HDR SOLD TAIL/MALE 10	1
521440028	SPACER HEX 4-40X7/8	1
524440001	STANDOFF HINGED 4-40X1 IN	2
560440004	SCREW PHILIPS 4-40X1/4	3
577400001	WASHER SHAKEPROOF SIZE 4	3
714032233	PC BD PREASS'Y HV4032-2B	1
SM227060186	IC 16-BIT MICROPROC 80C186	1

End of report. 83 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
102145104	CAP CERA DISC 12V .1 UF	1
102245103	CAP CERA DISC 25V .01 UF	4
102745201	CAP CERA DISC 500V 200 PF	2
103437334	CAP CERA MONO 100V .33 UF	5
103626102	CAP CERA MONO 100 .001 UF	1
142824685	CAP TANT DIP CASE 6.8 UF	15
148236152	CAP ALU METAL CAN 1500 UF	1
148580581	CAP ALU METAL CAN 5800 UF	3
148860103	CAP ALU METL CAN 10000 UF	2
161225101	RES CARBON FILM 100 OHMS	2
161225102	RES CARBON FILM 1 K	1
161225103	RES CARBON FILM 10 K	2
161225104	RES CARBON FILM 100 K	1
161225133	RES CARBON FILM 13 K	1
161225153	RES CARBON FILM 15 K	6
161225181	RES CARBON FILM 180 OHMS	2
161225202	RES CARBON FILM 2 K	5
161225393	RES CARBON FILM 39 K	1
161225472	RES CARBON FILM 4.7 K	5
161225513	RES CARBON FILM 51 K	1
161225561	RES CARBON FILM 560 OHMS	2
161225751	RES CARBON FILM 750 OHMS	1
161335100	RES CARBON FILM 10 OHMS	3
161335162	RES CARBON FILM 1.6 K	2
161335203	RES CARBON FILM 20 K	1
161445010	RES CARBON FILM 1 OHM	1
161665272	RES COMP 2W 5% 2.7 K	1
168531393	RES PREC RN55D 1.00 K	1
168531417	RES PREC RN55D 1.78 K	1
168531439	RES PREC RN55D 3.01 K	4
168531458	RES PREC RN55D 4.75 K	4
168531468	RES PREC RN55D 6.04 K	1
168531489	RES PREC RN55D 10.0 K	2
168531518	RES PREC RN55D 20.0 K	1
168531545	RES PREC RN55D 38.3 K	2
175235005	RES PWR WW 2.5W 5% .5 OHM	2
175351001	RES PWR WW 3W 1% 0.1 OHM	4
181467102	RES VARI CERMET 1 K	1
181467203	RES VARI CERMET 20 K	1
181467501	RES VARI CERMET 500 OHMS	2
206033000	IC 2-IN NAND GT MM74C00N	1
208011004	IC TIMER NE555	1
208021323	VOLT REGULATOR 323AT	2
208031004	IC PREC VOLT REG UA723C	2
208031514	IC QUAD OP AMP NE5514N	1
208123002	IC +12 VOLT REG LM340T-12	1
208124002	IC VOLT REG -5V UA7905UC	1
230110005	DIODE SWITCHING 1N4448	9
235010005	DIODE RECTIFIER 1N4005	2
235050001	DIODE RECTIFIER 1N4139	2
235050002	DIODE RECTIFIER 1N4140	4
235930001	DIODE PWR DUAL COMMN CATH	1

PART NUMBER	DESCRIPTION REMARK	QTY PER
240423966	DIODE ZENER 16V 1N966B	2
270110003	TRANSISTOR NPN PN2222A	4
270180004	TRANSISTOR NPN PWR 2N5882	4
271130002	TRANSISTOR NPN PWR TIP31C	1
275110001	TRANSISTOR PNP P2N2907	2
275130001	TRANSISTOR PNP PWR TIP32A	1
275130042	TRANSISTOR PNP TIP42C	1
275150003	TRANSISTOR PNP 40319	1
286120125	TRANS PNP DARLINGT TIP125	1
286220120	TRANS NPN DARLINGT TIP120	1
400010008	SOCKET IC SOLD TAIL DIP-8	1
400020014	SOCKET IC SOLD TAIL DIP-14	4
405193003	CONNECTOR BLOCK (SOCKET)	1
405542001	CONNECTOR PIN (FEMALE)	15
405764010	SOCKET SINGLE WIRE - OPEN	10
433220001	FUSE PICO II 125V 10 AMP	1
454311002	HDR SOLD TAIL/MALE 2	1
500120009	TRANSIPAD LO PROFIL LARGE	1
500860302	INSULATOR FOR TO-220	9
500860442	INSULATOR FOR TO-3	5
510110006	LOCKING TERMINAL LUG #6	1
512241202	BRACKET REAR FOR 4032A-3	1
512241203	BRACKET FRONT FOR 4032A-3	1
512341101	HEAT SINK FOR LO VOLT BD	1
515403001	CLAMP,CAPACITOR MTG 1 3/8	3
515403008	CAPACITOR CLAMP 2" DIA	2
520000510	STANDOFF GLASS 8MM	8
555611001	CAPTIVE SCREW 6-32	1
555631001	CAPTIVE SCREW 6-32X5/8	1
555662001	NUT SELF-CLINCHING 6-32	11
560032010	SCREW PHILIPS 10-32X5/8	10
560632006	SCREW PHILIPS 6-32X3/8	1
560632008	SCREW PHILIPS 6-32X1/2	14
574109005	WASHER SHOULDER NYLON #10	10
574409005	WASHER SHOULDER NYLON #4	9
574809005	WASHER SHOULDER NYLON #8	5
575449005	WASHER FLAT SIZE #4 NYLON	12
576610001	WASHER SPLIT LOCK SIZE 6	15
577000002	WASHER SHAKEPROOF SIZE 10	10
577600001	WASHER SHAKEPROOF SIZE 6	1
594240001	CLAMP CABLE HALF 1/4" DIA	1
704032103	LATCHING STRIP LO VOLT BD	1
714032353	SEPARATOR BOARD HV4032A-3-SB	1
714032363	PC BD PREASS'Y HV4032A-3	1

End of report. 96 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
102245103	CAP CERA DISC 25V .01 UF	4
102745271	CAP CERA DISC 500V 270 PF	1
142824685	CAP TANT DIP CASE 6.8 UF	6
161225101	RES CARBON FILM 100 OHMS	6
161225102	RES CARBON FILM 1 K	2
161225103	RES CARBON FILM 10 K	4
161225151	RES CARBON FILM 150 OHMS	1
161225242	RES CARBON FILM 2.4 K	1
161225243	RES CARBON FILM 24 K	1
161225472	RES CARBON FILM 4.7 K	8
161225512	RES CARBON FILM 5.1 K	1
161225683	RES CARBON FILM 68 K	1
161335151	RES CARBON FILM 150 OHMS	6
161335162	RES CARBON FILM 1.6 K	1
161335181	RES CARBON FILM 180 OHMS	1
161335270	RES CARBON FILM 27 OHMS	2
161335301	RES CARBON FILM 300 OHMS	1
161445161	RES CARBON FILM 160 OHMS	1
161445681	RES CARBON FILM 680 OHMS	2
168531385	RES PREC RN55D 825 OHMS	1
190132472	RESISTOR NETWORK 4.7 K	1
200031005	IC HEX INVERTER SN7406N	1
200031085	IC DUAL LIN RCVR SN75108A	1
200031091	IC LINE DRIVER SN75112N	1
200041060	IC BCD-7 SEG L/D/D F34511	5
206033000	IC 2-IN NAND GT MM74C00N	2
206033002	IC 2-IN NOR GATE MM74C02N	1
206033004	IC HEX INVERTER MM74C04N	1
206033074	IC D-TYPE FL-FL MM74C74N	1
206043042	IC BCD-DEC DECOD MM74C42N	1
206043048	IC BCD-7 SEG DEC MM74C48N	1
208011006	IC SINGLE OP AMP LM318N	1
208031556	IC DUAL TIMER LM556CN	1
240225704	DIODE ZENER 4.3V 1N5991A	1
257230074	DISPLAY LED RED 7-SEGMENT	6
260020035	OPTICAL ISOLATOR 4N35	3
270110003	TRANSISTOR NPN PN2222A	1
400010008	SOCKET IC SOLD TAIL DIP-8	1
400020014	SOCKET IC SOLD TAIL DIP-14	18
400030016	SOCKET IC SOLD TAIL DIP-16	9
403111040	HEADER ASSEMBLY 40-PIN	1
403181003	HDR SINGL ROW 3	1
403980002	SHUNT ASSEMBLY 2-POS	1
405812002	SOCKET STRIP SOLDR 20 POS	1
416151002	SWITCH PUSHBUT 2-POS SPST TO BE PACKED IN STYROFOAM	1
416151003	SWITCH PUSHBUT 6-POS SPST TO BE PACKED IN STYROFOAM	1
420292007	SWITCH SLIDE PC MTG DPDT	1
520000510	STANDOFF GLASS 8MM	8

PART NUMBER	DESCRIPTION REMARK	QTY PER
714032011	PC BD PREASS'Y HV4032A-4S	3
714032413	PC BD PREASS'Y HV4032A-4	1

End of report. 54 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
195212001	VARISTOR 275V 40 JOULES	1
195212003	VARISTOR 130V 20 JOULES	2
315910010	LINE FILTER - RFI 10 A	1
405193003	CONNECTOR BLOCK (SOCKET)	1
405193004	CONNECTOR BLOCK (PIN)	1
405442014	CONNECTOR PIN (MALE)	15
405532014	CONNECTOR PIN (FEMALE)	10
420282001	SWITCH SLIDE DPDT	1
434242001	FUSEHOLDER IN-LINE	2
440040004	TRANSFORMER (POWER)	1
485013110	GROMMET 1/8 PANEL 5/16 ID	1
512241028	SIDE PANEL (LEFT) HV4032A	1
512241029	BRACKET SIDE (INNER)	1
521400015	SPACER ROUND #4 15/32	1
521440012	SPACER HEX 4-40X3/8	2
530301002	HANDLE ROUND 5/16 DIA 4"	1
555465001	SCREW HEX HEAD 1/4-20X3/4	4
555465002	WASHER LOCK SPLIT 1/4	4
555465003	NUT HEX 1/4-20	4
560032008	SCREW PHILIPS 10-32X1/2	6
560440004	SCREW PHILIPS 4-40X1/4	4
560440007	SCREW PHILIPS 4-40X7/16	3
567440006	SCREW FLAT PHIL 4-40X3/8	2
575110002	WASHER FL 1/4 ID .500 OD	8
576010001	WASHER SPLIT LOCK SIZE 10	6
576410001	WASHER SPLIT LOCK SIZE 4	9
580440001	NUT HEX STANDARD 4-40	5
589203416	CORD PWR JUMPER 1 METER	1
589223118	CORD PWR 3-COND 7 1/2 FT	1
590001018	WIRE TEFLON 19/30 BLK 18	1
590111018	WIRE TEFLON 19/30 BRN 18	4
590111022	WIRE TEFLON 7/30 BRN 22	1
590221014	WIRE TEFLON 19/27 RED 14	4
590441022	WIRE TEFLON 7/30 YEL 22	2
590551022	WIRE TEFLON 7/30 GRN 22	2
590661018	WIRE TEFLON 19/30 BLU 18	4
590661022	WIRE TEFLON 7/30 BLU 22	1
590771018	WIRE TEFLON 19/30 VIO 18	4
590771022	WIRE TEFLON 7/30 VIO 22	1
590881018	WIRE TEFLON 19/30 GRAY 18	5
590881022	WIRE TEFLON 7/30 GRAY 22	1
590991018	WIRE TEFLON 19/30 WHT 18	1
594120001	TIEWRAP	10
594120002	TIEWRAP BASE AM2-C	1
594230001	CABLE CLAMP 5/16 DIA	3
595003102	SLEEVING SHRINK BLK 1/8"	0
595003103	SLEEVING SHRINK BLK 1/4"	0

End of report. 47 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
147976150	CAP ALUM METAL CAN 150 UF	4
206033164	IC 8-BIT SH REG MM74C164N	1
229020055	TRANS VOLT SUPPR P6KE6.8	1
229020145	TRANS VOLT SUPPR P6KE18	2
240225704	DIODE ZENER 4.3V 1N5991A	1
403116040	HEADER WIREWRAP 40-PIN	1
404150020	CONN PC EDG/SOLDTAIL20	8
404150030	CONN PC EDG/SOLDTAIL30	1
454320020	HDR SOLD TAIL/FEM 20	1
512041011	GUIDE BAR HV CONN ALIGNMT	8
512241106	BRACKET DISTRIBUTN BOARD	2
521440020	SPACER HEX 4-40X5/8	2
522632900	SPACER (SPECIAL ORDER)	1
560632008	SCREW PHILIPS 6-32X1/2	1
575610002	WASHER FLAT REG OD SIZE 6	1
576610001	WASHER SPLIT LOCK SIZE 6	1
714032613	PC BD PREASS'Y HV4032A-6	1

End of report. 17 Details encountered.

LECROY CORPORATION
HV4032A-8 PARTS LIST
Proprietary information of LeCroy Corporation

PART NUMBER	DESCRIPTION REMARK	QTY PER
187235102	RES VARI WW 10-TURN 5% 1K	1
320240003	BULB INCANDESCENT T1 3/4	2
402030000	CONN CO-AX LEMO	1
402030002	SPANNER NUT SMALL OD LEMO	1
402030003	GROUND LUG NONLOCK LEMO	1
402030066	INSUL WASHER LEMO BLU	2
402080000	CONN ISOLATED GND BULKHD BNC	1
405161001	CONN BLOCK PIN OR SOCKET	2
405193004	CONNECTOR BLOCK (PIN)	2
405232004	GUIDE PIN (MALE)	2
405332003	GUIDE PIN (FEMALE)	2
405442014	CONNECTOR PIN (MALE)	10
405555001	CONNECTOR PIN (FEMALE)	22
405712001	LOCKING SPRING "FEMALE"	4
410391100	SWITCH TOGGLE 2-POS TPST	1
412020016	SWITCH ROTARY BCD 16-POS	1
416090116	BUTTON ILLUM HORIZ SPLIT	1
416142005	SWITCH DUAL ILLU MOM SPDT	1
433115000	FUSE SLO-BLO 250V 5 AMP	1
433172010	FUSE SLO-BLO 250V 10 AMP	1
434131003	FUSEHOLDER PANEL MTG	1
512040003	FOAM FOR AIR FILTER	2
512241200	BRACKET FRONT PNL TO LVS	1
512943026	FAN SHROUD	2
530301001	HANDLE OVAL 10-32 MTG 6" LONG	2
530309001	FAN AXIAL 50/60 HZ 115V	2
530419400	LOCK ASSEMBLY - TOGGLE SW	1
536221002	KNOB ASSEMBLY 10-TURN	1
536242004	KNOB MOLDED W/INDICATOR	1
567032006	SCREW FLAT PHIL 10-32X3/8	4
592921026	CABLE FL JUMP-PLUG DIP-14	3
592922026	CABLE FL JUMP-PLUG DIP-16	1
724032022	FRONT PNL PREASSY HV4032A	1
754032007	FILTER (LED) RED ACRYLIC	1

End of report. 34 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
102055332	CAP CERA DISC 3KV 3300 PF	4
102094330	CAP CERA DISC 6KV 33PF	4
102245103	CAP CERA DISC 25V .01 UF	6
102295104	CAP CERA DISC 25V .1 UF	1
102335104	CAP CERA DISC CK05 50V .1 UF	4
102444220	CAP CERA DISC 100V 22 PF	1
102745102	CAP CERA DISC 500V .001 UF	1
103327103	CAP CERA MONO 50V .01 UF	4
103427104	CAP CERA MONO 100V .1 UF	5
124076153	CAP POLYESTER FILM .015 UF	8
142124476	CAP TANT DIP CASE 47 UF	1
142824685	CAP TANT DIP CASE 6.8 UF	7
147956047	CAP ALUM METAL CAN 47 UF	4
161225103	RES CARBON FILM 10 K	5
161225124	RES CARBON FILM 120 K	4
161225202	RES CARBON FILM 2 K	1
161225203	RES CARBON FILM 20 K	2
161225244	RES CARBON FILM 240 K	4
161225390	RES CARBON FILM 39 OHMS	4
161225510	RES CARBON FILM 51 OHMS	4
161225512	RES CARBON FILM 5.1 K	1
161225753	RES CARBON FILM 75 K	4
161225822	RES CARBON FILM 8.2 K	1
161305512	RES COMP 1/4 5% 5.1 K	8
161335102	RES CARBON FILM 1 K	4
161505242	RES COMP 1W 5% 2.4 K	4
168439461	RES RN55C .1% 5.11 K	1
168531401	RES PREC RN55D 1.21 K	1
168531417	RES PREC RN55D 1.78 K	1
168531422	RES PREC RN55D 2.00 K	4
168531445	RES PREC RN55D 3.48 K	4
180417504	RES VARI CERMET 500 K	4
206042509	IC DIFFER MULTPLX DG509CJ	1
208011006	IC SINGLE OP AMP LM318N	1
208011008	IC VOLT COMPARATOR LM311N	4
208031514	IC QUAD OP AMP NE5514N	2
230110005	DIODE SWITCHING 1N4448	18
235040060	DIODE RECTIFIER LM60	8
270110003	TRANSISTOR NPN PN2222A	4
270170001	TRANSISTOR NPN 2N5770	1
271130002	TRANSISTOR NPN PWR TIP31C	4
275110001	TRANSISTOR PNP 2N2907A	4
377011002	LABEL:"DANGER:HI VOLTAGE"	1
377011004	LABEL: "- NEGATIVE -"	1
400010008	SOCKET IC SOLD TAIL DIP-8	5
400020014	SOCKET IC SOLD TAIL DIP-14	2
400030016	SOCKET IC SOLD TAIL DIP-16	1
402070000	CONN CO-AX SHV	4
408030103	WIREWRAP PIN	4
433220003	FUSE PICO II 125V .5 AMP	4
440080001	TRANSFORMER HI V STEP-UP	4
500860302	INSULATOR FOR TO-220	4

PART NUMBER	DESCRIPTION REMARK	QTY PER
512241001	FRONT PANEL HV OUTPUT BD	1
512241003	COVER FOR OUTPUT BD	1
512341204	HEAT SINK	2
512543007	REAR PANEL FOR HV MODULE MAY SUBSTITUTE WITH 521241002 ONLY WHEN STOCK IS DEPLETED.	1
555048005	PLUNGER FOR RETAINER	2
555049004	GROMMET FOR RETAINER	2
560440004	SCREW PHILIPS 4-40X1/4	4
560440005	SCREW PHILIPS 4-40X5/16	8
574409005	WASHER SHOULDER NYLON #4 MAY SUBSTITUTE WITH 500-460-005.	4
575410002	WASHER FLAT SS .250 OD #4	4
576410001	WASHER SPLIT LOCK SIZE 4	12
591222122	WIRE SOLID TEF RED AWG 22	1
714032123	PC BD PREASS'Y HV4032A-1N	1
HR130A	UNCASED SUBSTRATE HR130A	4

End of report. 71 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
102055332	CAP CERA DISC 3KV 3300 PF	4
102094330	CAP CERA DISC 6KV 33PF	4
102245103	CAP CERA DISC 25V .01 UF	7
102295104	CAP CERA DISC 25V .1 UF	1
102335104	CAP CERA DISC CK05 50V .1 UF	4
102412330	CAP CERA DISC 100V 33 PF	1
102444270	CAP CERA DISC 100V 27 PF	1
102745102	CAP CERA DISC 500V .001 UF	1
103327102	CAP CERA MONO 50V .001 UF	4
103427104	CAP CERA MONO 100V .1 UF	5
124076153	CAP POLYESTER FILM .015 UF	8
142124476	CAP TANT DIP CASE 47 UF	1
142824685	CAP TANT DIP CASE 6.8 UF	9
147956047	CAP ALUM METAL CAN 47 UF MAY SUBSTITUTE WITH 148-797-047.	4
161225103	RES CARBON FILM 10 K	6
161225124	RES CARBON FILM 120 K	4
161225183	RES CARBON FILM 18 K	1
161225185	RES CARBON FILM 1.8 MEG	1
161225203	RES CARBON FILM 20 K	3
161225244	RES CARBON FILM 240 K	4
161225390	RES CARBON FILM 39 OHMS	4
161225393	RES CARBON FILM 39 K	2
161225510	RES CARBON FILM 51 OHMS	4
161225512	RES CARBON FILM 5.1 K	2
161225753	RES CARBON FILM 75 K	4
161305512	RES COMP 1/4 5% 5.1 K	8
161335102	RES CARBON FILM 1 K	4
161505242	RES COMP 1W 5% 2.4 K	4
168439461	RES RN55C .1% 5.11 K	3
168531389	RES PREC RN55D 909 OHMS	1
168531413	RES PREC RN55D 1.62 K	4
168531421	RES PREC RN55D 1.96 K	1
168531445	RES PREC RN55D 3.48 K	4
180417504	RES VARI CERMET 500 K	4
206042509	IC DIFFER MULTPLX DG509CJ	1
208011006	IC SINGLE OP AMP LM318N	1
208011008	IC VOLT COMPARATOR LM311N	4
208031514	IC QUAD OP AMP NE5514N	2
208044002	IC TRANS ARRAY HF CA3127E	1
230110005	DIODE SWITCHING 1N4448	26
235040060	DIODE RECTIFIER LM60	8
270110003	TRANSISTOR NPN PN2222A	5
271130002	TRANSISTOR NPN PWR TIP31C	4
275110001	TRANSISTOR PNP 2N2907A	4
275170002	TRANSISTOR PNP 2N5771	1
377011002	LABEL:"DANGER:HI VOLTAGE"	1
377011003	LABEL: "+ POSITIVE +"	1
400010008	SOCKET IC SOLD TAIL DIP-8	5
400020014	SOCKET IC SOLD TAIL DIP-14	2
400030016	SOCKET IC SOLD TAIL DIP-16	2

PART NUMBER	DESCRIPTION REMARK	QTY PER
402070000	CONN CO-AX SHV	4
408030103	WIREWRAP PIN	4
433220003	FUSE PICO II 125V .5 AMP	4
440080001	TRANSFORMER HI V STEP-UP	4
500860302	INSULATOR FOR TO-220	4
512241001	FRONT PANEL HV OUTPUT BD	1
512241003	COVER FOR OUTPUT BD	1
512341204	HEAT SINK	2
512543007	REAR PANEL FOR HV MODULE	1
555048005	PLUNGER FOR RETAINER	2
555049004	GROMMET FOR RETAINER	2
560440004	SCREW PHILIPS 4-40X1/4	4
560440005	SCREW PHILIPS 4-40X5/16	8
574409005	WASHER SHOULDER NYLON #4 MAY SUBSTITUTE WITH 500-460-005.	4
575410002	WASHER FLAT SS .250 OD #4	4
576410001	WASHER SPLIT LOCK SIZE 4	12
591222122	WIRE SOLID TEF RED AWG 22	1
593910001	CABLE CO-AXIAL RG178B/U	3
714032143	PC BD PREASS'Y HV4032A-1P	1
HR130A	UNCASED SUBSTRATE HR130A	4

End of report. 74 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
102094330	CAP CERA DISC 6KV 33PF	1
102095502	CAP CERA DISC 4KV .005 UF	4
161305103	RES COMP 1/4W 5% 10 K	2
235040060	DIODE RECTIFIER LM60	4
408030103	WIREWRAP PIN	2
519350001	BUSHING NYLON	2
714032021	PC PREASS'Y HV4032A7-2	1
714032173	PC BD PREASS'Y HV4032A7-1	1

End of report. 8 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
102095352	CAP CERA DISC 7.5KV .0035 UF	4
102245103	CAP CERA DISC 25V .01 UF	7
102335104	CAP CERA DISC CK05 50V .1 UF	4
102355224	CAP CERA DISC 16V .22 UF	1
102444220	CAP CERA DISC 100V 22 PF	1
102444270	CAP CERA DISC 100V 27 PF	2
102940202	CAP CERA DISC 1KV .002 UF	2
103327103	CAP CERA MONO 50V .01 UF	10
103427104	CAP CERA MONO 100V .1 UF	7
103626102	CAP CERA MONO 100 .001 UF	4
142124476	CAP TANT DIP CASE 47 UF	1
142824685	CAP TANT DIP CASE 6.8 UF	8
147956047	CAP ALUM METAL CAN 47 UF	2
161030000	RES COMP ZERO OHMS	2
161225102	RES CARBON FILM 1 K	5
161225103	RES CARBON FILM 10 K	4
161225123	RES CARBON FILM 12 K	1
161225125	RES CARBON FILM 1.2 MEG	1
161225162	RES CARBON FILM 1.6 K	2
161225163	RES CARBON FILM 16 K	4
161225203	RES CARBON FILM 20 K	2
161225242	RES CARBON FILM 2.4 K	4
161225243	RES CARBON FILM 24 K	2
161225244	RES CARBON FILM 240 K	2
161225272	RES CARBON FILM 2.7 K	1
161225390	RES CARBON FILM 39 OHMS	2
161225432	RES CARBON FILM 4.3 K	2
161225472	RES CARBON FILM 4.7 K	2
161225473	RES CARBON FILM 47 K	3
161225510	RES CARBON FILM 51 OHMS	2
161225511	RES CARBON FILM 510 OHMS	4
161225512	RES CARBON FILM 5.1 K	2
161225513	RES CARBON FILM 51 K	1
161225561	RES CARBON FILM 560 OHMS	1
161225562	RES CARBON FILM 5.6 K	2
161225681	RES CARBON FILM 680 OHMS	1
161225753	RES CARBON FILM 75 K	2
161225823	RES CARBON FILM 82 K	2
161305103	RES COMP 1/4W 5% 10 K	2
161335682	RES CARBON FILM 6.8 K	1
161505512	RES COMP 1W 5% 5.1 K	4
168139518	RES RN55E .1% 20.0 K	2
168139547	RES RN55E .1% 40.2 K	2
168139573	RES RN55E .1% 75.0 K	12
168139681	RES RN55E .1% 1.00 MEG	4
168439461	RES RN55C .1% 5.11 K	1
180417105	RES VARI CERMET 1 MEG	2
206033107	IC DUAL J-K FF MM74C107N	1
206042509	IC DIFFER MULTPLX DG509CJ	1
208011006	IC SINGLE OP AMP LM318N	1
208011008	IC VOLT COMPARATOR LM311N	2
208031064	IC J-FET OP AMP TL064ACN	3

PART NUMBER	DESCRIPTION REMARK	QTY PER
208031084	IC QUAD J-FET OP AMP 084	2
229020145	TRANS VOLT SUPPR P6KE18	4
230110005	DIODE SWITCHING 1N4448	31
235010005	DIODE RECTIFIER 1N4005	7
240225713	DIODE ZENER 9.1V 1N5999A	2
260070065	OPTOCOUPLER 11.6KV CNY65	2
270110003	TRANSISTOR NPN PN2222A	2
270170001	TRANSISTOR NPN 2N5770	2
270170002	TRANSISTOR NPN 2N5962	4
271130002	TRANSISTOR NPN PWR TIP31C	2
275110001	TRANSISTOR PNP 2N2907A	3
280170306	TRANSISTOR FET N VN1306N3	7
281170304	TRANSISTOR FET P VP1304N3	2
377011002	LABEL:"DANGER:HI VOLTAGE"	1
377011013	LABEL "NEGATIVE" - ETC	1
377011014	LABEL "7KV"	2
400010008	SOCKET IC SOLD TAIL DIP-8	3
400020014	SOCKET IC SOLD TAIL DIP-14	6
400030016	SOCKET IC SOLD TAIL DIP-16	1
402070000	CONN CO-AX SHV	2
402070002	CONN CO-AX BULKHD 10 KV	0
408030103	WIREWRAP PIN	2
430090484	RELAY 7KV (40V COIL) SPST	2
433220003	FUSE PICO II 125V .5 AMP	2
440080001	TRANSFORMER HI V STEP-UP	2
454710012	HDR SOLD TAIL/MALE 12	1
471112006	BUS BAR 2-CONDUCTOR	6
500460006	INSULATOR THERMALFILM	2
512341006	HEAT SINK FOR HV4032A-7KV	1
512543001	FRONT PANEL HV MODULE	1
512543002	SHIELD BOTTOM HV MODULE	1
512543003	COVER TOP HV MODULE	1
512543007	REAR PANEL FOR HV MODULE	1
521440006	SPACER HEX 4-40X3/16	4
555048005	PLUNGER FOR RETAINER	2
555049004	GROMMET FOR RETAINER	2
560440004	SCREW PHILIPS 4-40X1/4	4
560440005	SCREW PHILIPS 4-40X5/16	8
574409005	WASHER SHOULDER NYLON #4	2
575410002	WASHER FLAT SS .250 OD #4	4
576410001	WASHER SPLIT LOCK SIZE 4	12
593910001	CABLE CO-AXIAL RG178B/U	0
595003018	SLEEVING SHRINK BLK 3/32"	0
599050001	CONFORMAL COATING	0
714032073	PC BD PREASS'Y HV4032A7N	1
CH599064012	SILICONE SEALANT RTV162	1
HR170	HV DIVIDER NETWORK	2
HV4032A71	HV4032A7-1	2

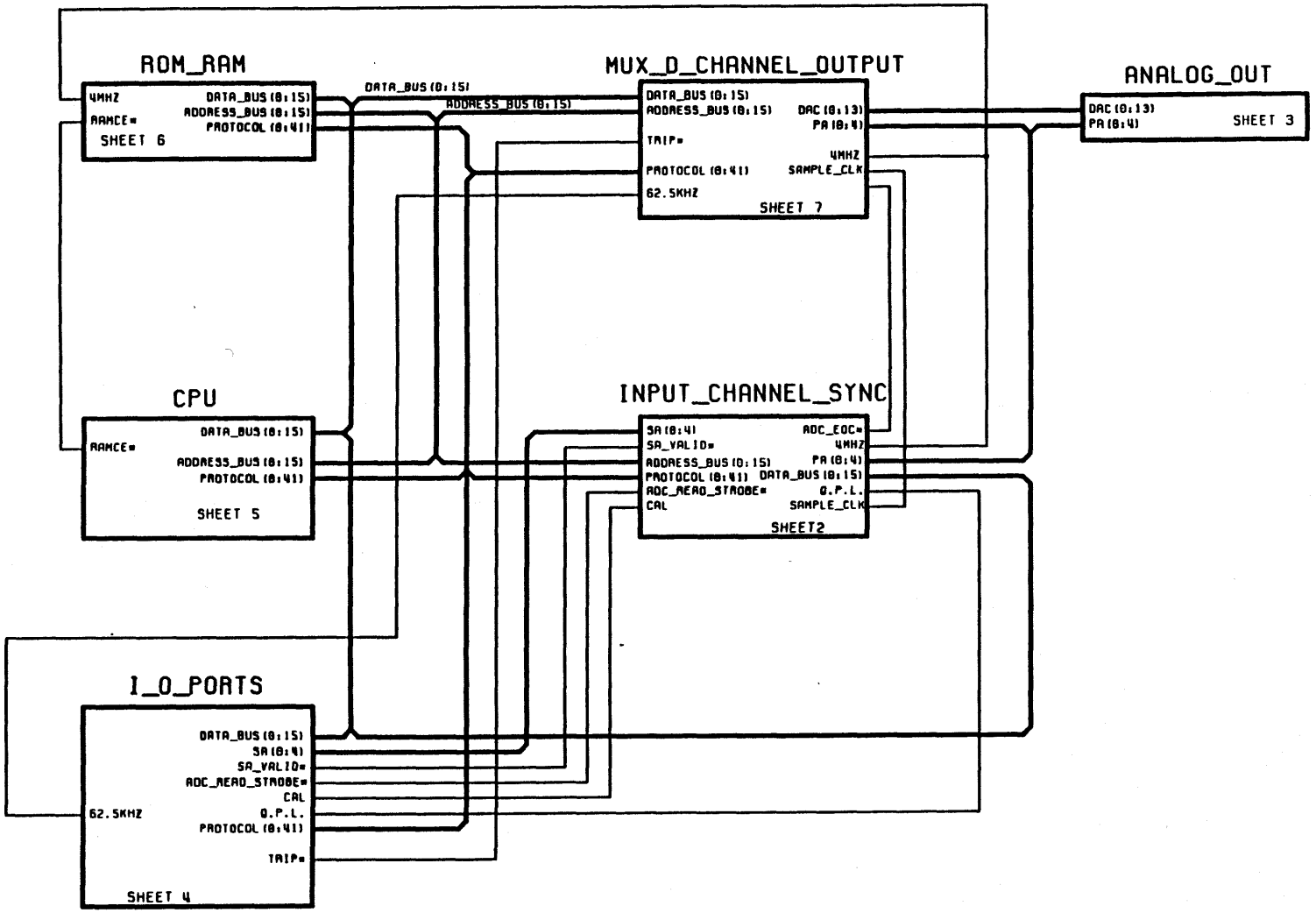
End of report. 100 Details encountered.

PART NUMBER	DESCRIPTION REMARK	QTY PER
102095352	CAP CERA DISC 7.5KV .0035 UF	4
102245103	CAP CERA DISC 25V .01 UF	5
102335104	CAP CERA DISC CK05 50V .1 UF	4
102355224	CAP CERA DISC 16V .22 UF	1
102444220	CAP CERA DISC 100V 22 PF	1
102444270	CAP CERA DISC 100V 27 PF	2
102940202	CAP CERA DISC 1KV .002 UF	2
103216333	CAP CERA MONO 50V .033 UF	2
103327103	CAP CERA MONO 50V .01 UF	13
103427104	CAP CERA MONO 100V .1 UF	7
103626102	CAP CERA MONO 100 .001 UF	5
116515330	CAP DIP MICA DM10 33 PF	1
142124476	CAP TANT DIP CASE 47 UF	1
142824685	CAP TANT DIP CASE 6.8 UF	8
147956047	CAP ALUM METAL CAN 47 UF	2
161030000	RES COMP ZERO OHMS	2
161225102	RES CARBON FILM 1 K	5
161225103	RES CARBON FILM 10 K	5
161225123	RES CARBON FILM 12 K	1
161225125	RES CARBON FILM 1.2 MEG	1
161225154	RES CARBON FILM 150 K	4
161225162	RES CARBON FILM 1.6 K	2
161225163	RES CARBON FILM 16 K	4
161225183	RES CARBON FILM 18 K	1
161225203	RES CARBON FILM 20 K	2
161225242	RES CARBON FILM 2.4 K	4
161225243	RES CARBON FILM 24 K	2
161225272	RES CARBON FILM 2.7 K	1
161225304	RES CARBON FILM 300 K	4
161225390	RES CARBON FILM 39 OHMS	2
161225393	RES CARBON FILM 39 K	2
161225432	RES CARBON FILM 4.3 K	2
161225472	RES CARBON FILM 4.7 K	2
161225473	RES CARBON FILM 47 K	3
161225510	RES CARBON FILM 51 OHMS	2
161225511	RES CARBON FILM 510 OHMS	4
161225512	RES CARBON FILM 5.1 K	3
161225513	RES CARBON FILM 51 K	1
161225561	RES CARBON FILM 560 OHMS	1
161225562	RES CARBON FILM 5.6 K	2
161225681	RES CARBON FILM 680 OHMS	1
161225753	RES CARBON FILM 75 K	2
161225823	RES CARBON FILM 82 K	2
161305103	RES COMP 1/4W 5% 10 K	2
161335682	RES CARBON FILM 6.8 K	1
161505512	RES COMP 1W 5% 5.1 K	4
168139518	RES RN55E .1% 20.0 K	2
168139547	RES RN55E .1% 40.2 K	2
168139573	RES RN55E .1% 75.0 K	4
168139681	RES RN55E .1% 1.00 MEG	6
168439461	RES RN55C .1% 5.11 K	3
180417105	RES VARI CERMET 1 MEG	2

PART NUMBER	DESCRIPTION REMARK	QTY PER
206033107	IC DUAL J-K FF MM74C107N	1
206042509	IC DIFFER MULTPLX DG509CJ	1
208011006	IC SINGLE OP AMP LM318N	1
208011008	IC VOLT COMPARATOR LM311N	2
208031064	IC J-FET OP AMP TL064ACN	3
208031084	IC QUAD J-FET OP AMP 084	2
208044002	IC TRANS ARRAY HF CA3127E	1
229020145	TRANS VOLT SUPPR P6KE18	4
230110005	DIODE SWITCHING 1N4448	39
235010005	DIODE RECTIFIER 1N4005	7
240225713	DIODE ZENER 9.1V 1N5999A	2
260070065	OPTOCOUPLER 11.6KV CNY65	2
270110003	TRANSISTOR NPN PN2222A	2
270170001	TRANSISTOR NPN 2N5770	2
270170002	TRANSISTOR NPN 2N5962	2
271130002	TRANSISTOR NPN PWR TIP31C	2
275110001	TRANSISTOR PNP 2N2907A	3
275170001	TRANSISTOR PNP 2N5087	4
275170002	TRANSISTOR PNP 2N5771	1
280170306	TRANSISTOR FET N VN1306N3	7
281170304	TRANSISTOR FET P VP1304N3	2
377011002	LABEL:"DANGER:HI VOLTAGE"	1
377011012	LABEL "POSITIVE" - ETC	1
377011014	LABEL "7KV"	2
400010008	SOCKET IC SOLD TAIL DIP-8	3
400020014	SOCKET IC SOLD TAIL DIP-14	6
400030016	SOCKET IC SOLD TAIL DIP-16	2
402070000	CONN CO-AX SHV	2
402070002	CONN CO-AX BULKHD 10 KV	0
408030103	WIREWRAP PIN	4
430090484	RELAY 7KV (40V COIL) SPST	2
433220003	FUSE PICO II 125V .5 AMP	2
440080001	TRANSFORMER HI V STEP-UP	2
454710012	HDR SOLD TAIL/MALE 12	1
471112006	BUS BAR 2-CONDUCTOR	6
500460006	INSULATOR THERMALFILM	2
512341006	HEAT SINK FOR HV4032A-7KV	1
512543001	FRONT PANEL HV MODULE	1
512543002	SHIELD BOTTOM HV MODULE	1
512543003	COVER TOP HV MODULE	1
512543007	REAR PANEL FOR HV MODULE	1
521440006	SPACER HEX 4-40X3/16	4
555048005	PLUNGER FOR RETAINER	2
555049004	GROMMET FOR RETAINER	2
560440004	SCREW PHILIPS 4-40X1/4	4
560440005	SCREW PHILIPS 4-40X5/16	8
560440007	SCREW PHILIPS 4-40X7/16	4
574409005	WASHER SHOULDER NYLON #4	2
575410002	WASHER FLAT SS .250 OD #4	4
576410001	WASHER SPLIT LOCK SIZE 4	12
581440001	NUT HEX SMALL OD SIZE 4	4
593910001	CABLE CO-AXIAL RG178B/U	0

PART NUMBER	DESCRIPTION REMARK	QTY PER
595003018	SLEEVING SHRINK BLK 3/32"	0
599050001	CONFORMAL COATING	0
714032083	PC BD PREASS'Y HV4032A7P	1
HR170	HV DIVIDER NETWORK	2
HV4032A71	HV4032A7-1	2

End of report. 109 Details encountered.



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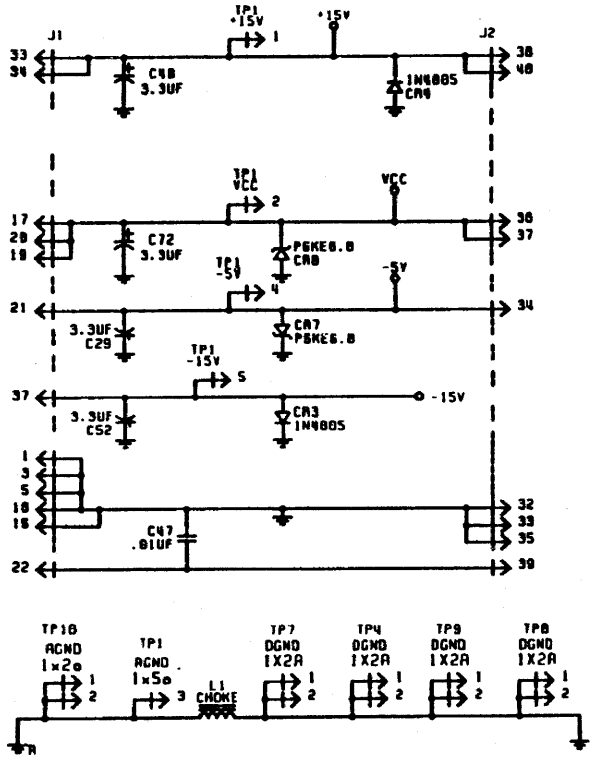
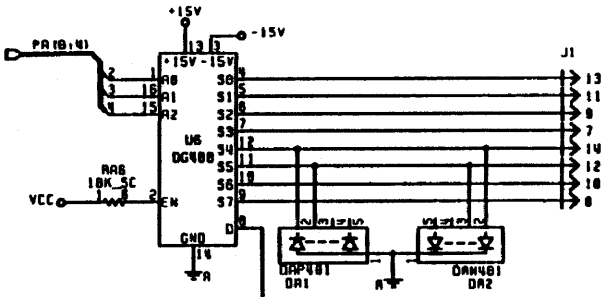
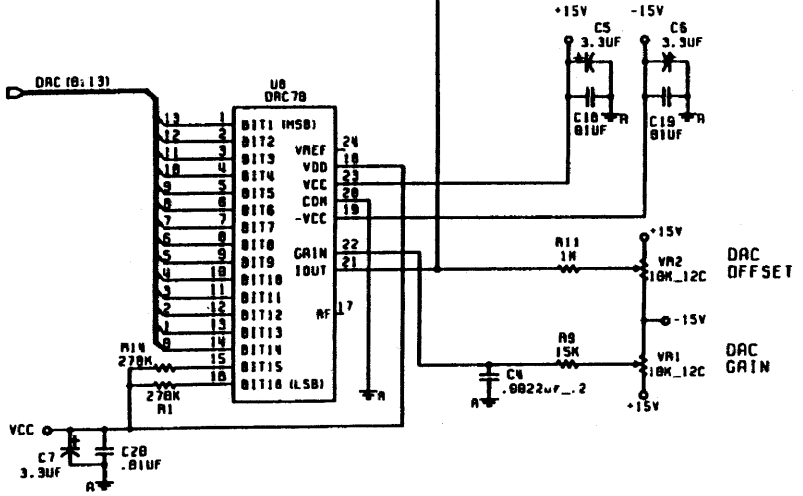
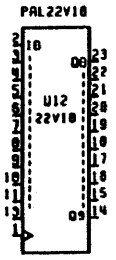
LeCroy Corp.	
DRAWN ALBERT_E	SCHEMATIC DIAGRAM
MODIFIED 22-NOV-93	HV4032A-2B
SHEET 1/7	DWG NO: HV4032A-2B-S01
	ECO NO: 1005

$HV4032A_2B sheet1









ANALOG_OUT

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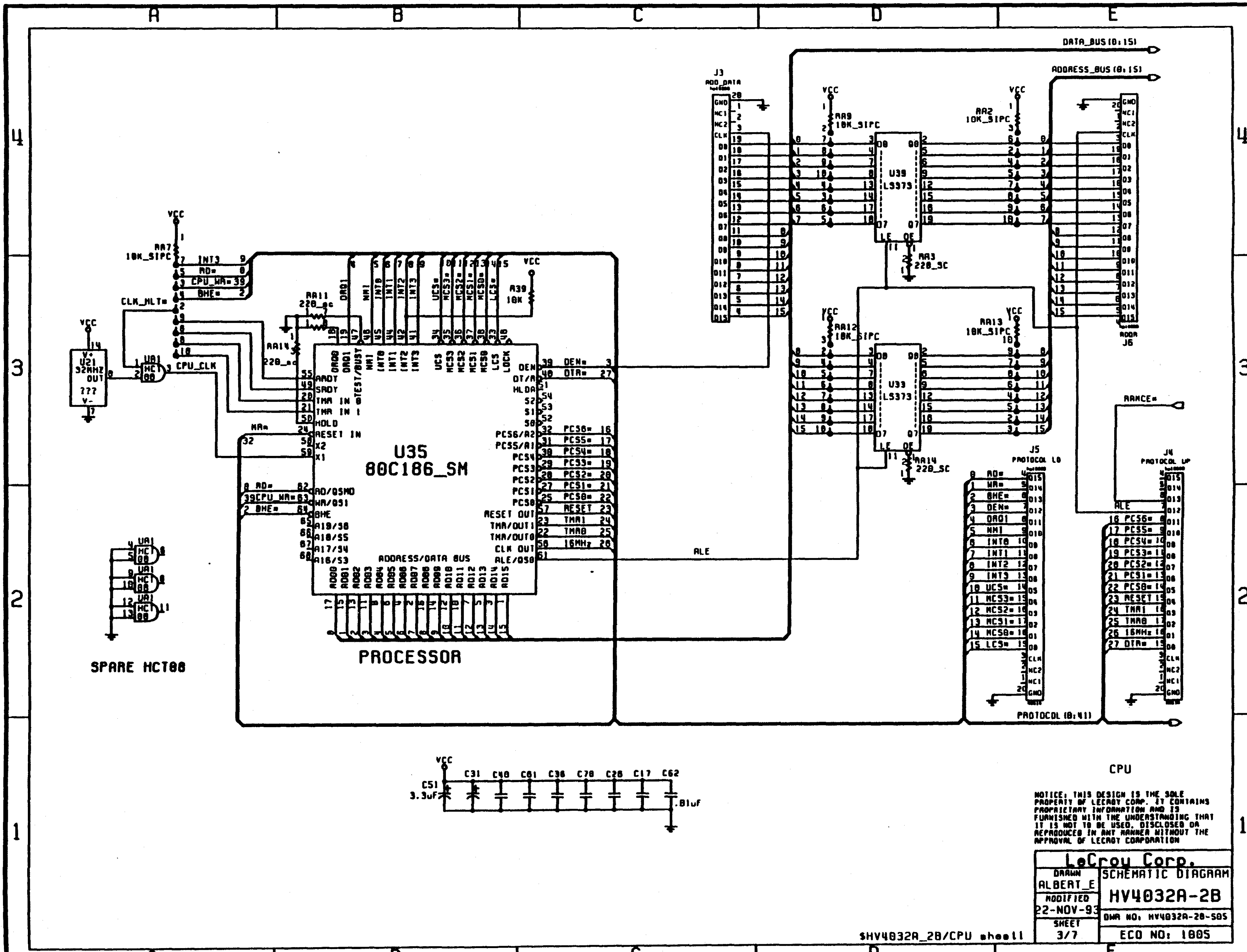
LeCroy Corp.

DRAWN ALBERT_E	SCHEMATIC DIAGRAM HV4032A-2B
MODIFIED 22-NOV-93	DWR NO: HV4032A-2B-S03
SHEET 2/7	ECO NO: 1005

$HV4032A_2B/ANALOG_OUT sheet1



CPU

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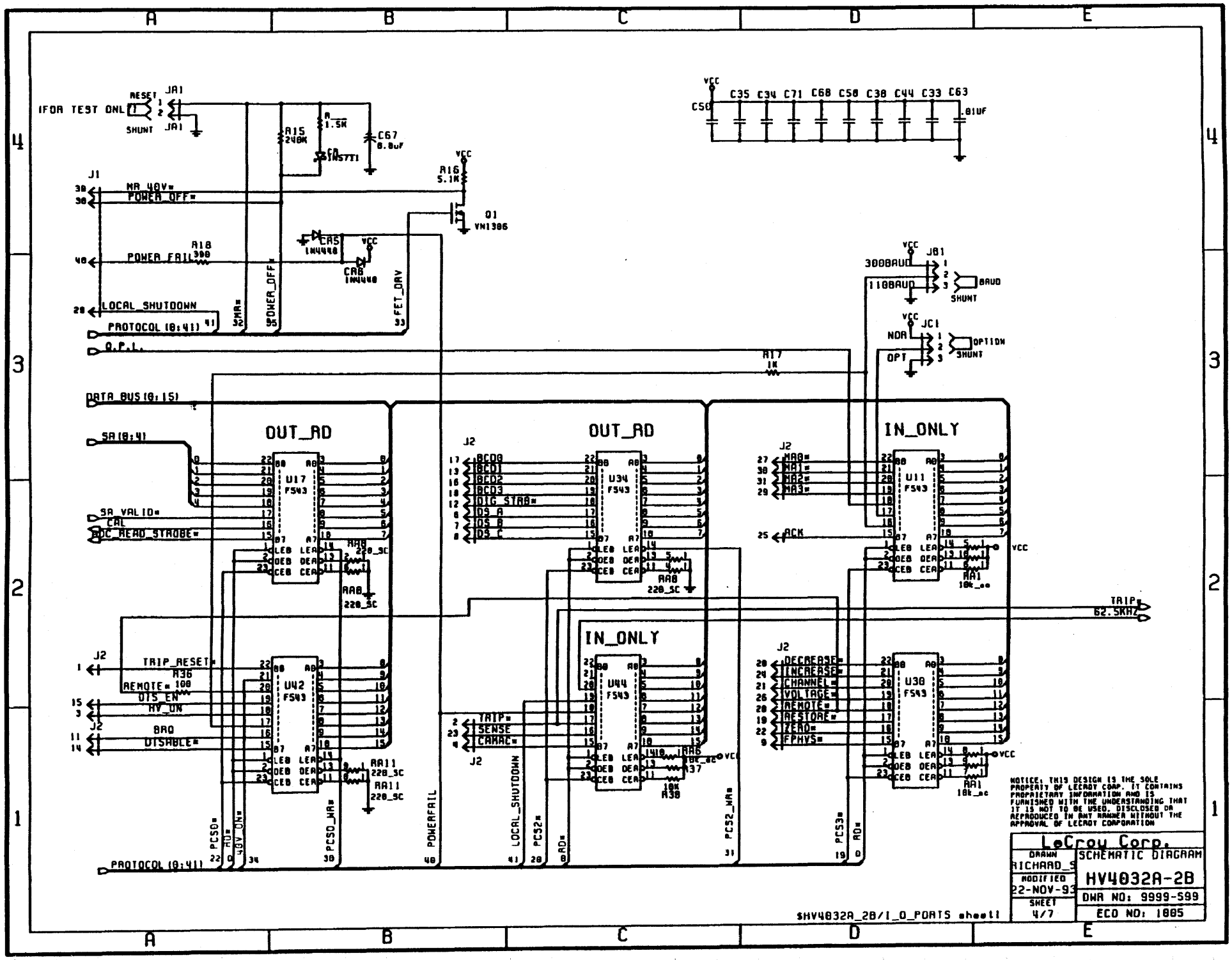
LeCroy Corp.	
DRAWN ALBERT_E	SCHEMATIC DIAGRAM
MODIFIED 22-NOV-93	HV4032A-2B
	DWR NO: HV4032A-2B-SOS
SHEET 3/7	ECO NO: 1005

$HV4032A_2B/CPU sheet1



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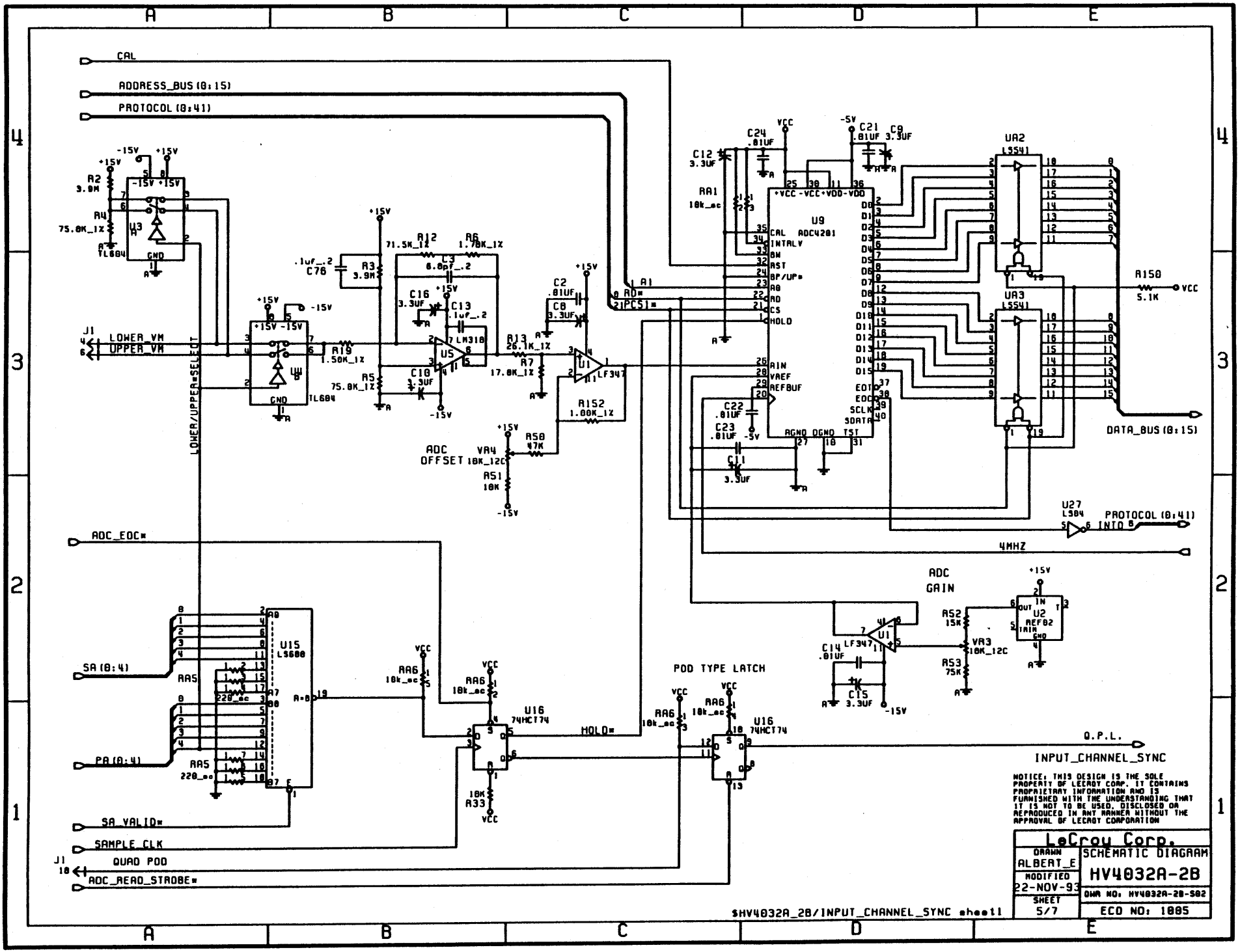
LeCroy Corp.	
DRAWN RICHARD_S	SCHEMATIC DIAGRAM
MODIFIED 22-NOV-93	HV4032A-2B
SHEET 4/7	DWG NO: 9999-599
	ECO NO: 1805

$HV4032A_2B/I_O_PORTS sheet1


CAL
ADDRESS_BUS(0:15)
PROTOCOL(0:4)
LOWER_VM
UPPER_VM
LOWER/UPPER*SELECT
ADC_EOC*
SA(0:4)
PA(0:4)
SA_VALID*
SAMPLE_CLK
QUAD POD
ADC_READ_STROBE*
ADC OFFSET
ADC GAIN
POD TYPE LATCH
HOLD*
Q.P.L.
INPUT_CHANNEL_SYNC
DATA_BUS(0:15)
4MHZ
U9 ADC4281
U15 LS688
U16 74HCT74
U27 LS04
LF347
LM318
TL684
LS541
REF02
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LeCroy Corp.
DRAWN ALBERT_E
MODIFIED 22-NOV-93
SHEET 5/7
SCHEMATIC DIAGRAM
HV4032A-2B
DWG NO: HV4032A-2B-S02
ECO NO: 1085
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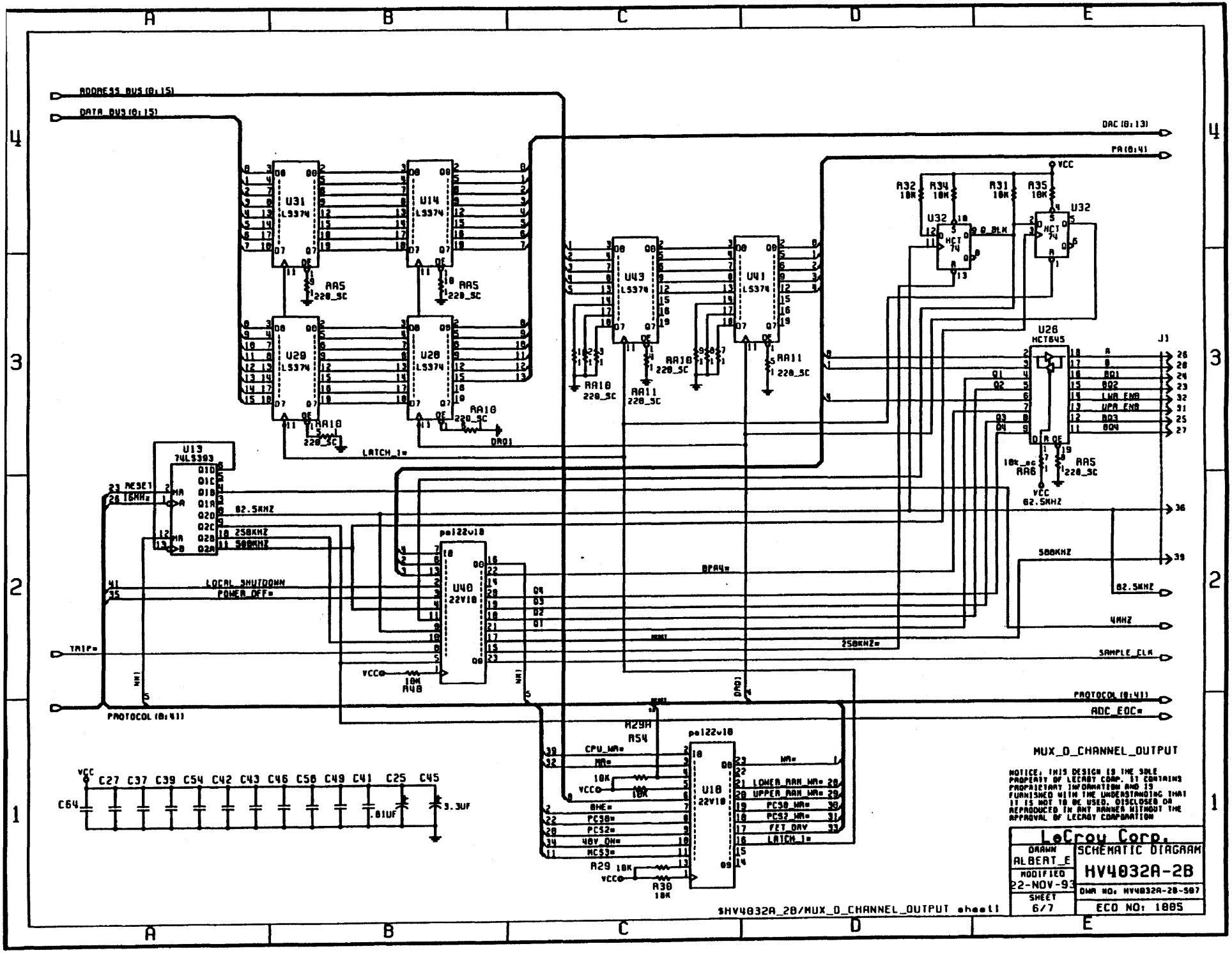
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DATA BUS(0:15)
DAC(0:13)
PA(0:4)
VCC
U31 LS374
U14 LS374
U29 LS374
U28 LS374
U43 LS374
U41 LS374
RA5 220_SC
RA10 220_SC
RA11 220_SC
U32 HCT 74
A32 10K
A34 10K
A31 10K
A35 10K
U26 HCT645
J1
LATCH_1=
DRQ1
U13 74LS393
RESET
15MHz
82.5KHZ
250KHZ
500KHZ
LOCAL_SHUTDOWN
POWER_OFF=
TRIP=
PROTOCOL(0:4)
U40 22V10
U18 22V10
R48 10K
R29A
R54
R29 10K
R30 10K
CPU_WR=
WR=
BHE=
PCS0=
PCS2=
48V_ON=
MCS3=
LOWER_RAM_WR=
UPPER_RAM_WR=
PCS0_WR=
PCS2_WR=
FET_DRV
LATCH_1=
BPA4=
4MHZ
SAMPLE_CLK
ADC_EOC=
C64
C27 C37 C39 C54 C42 C43 C46 C58 C49 C41 C25 C45
.01UF
3.3UF
MUX_D_CHANNEL_OUTPUT
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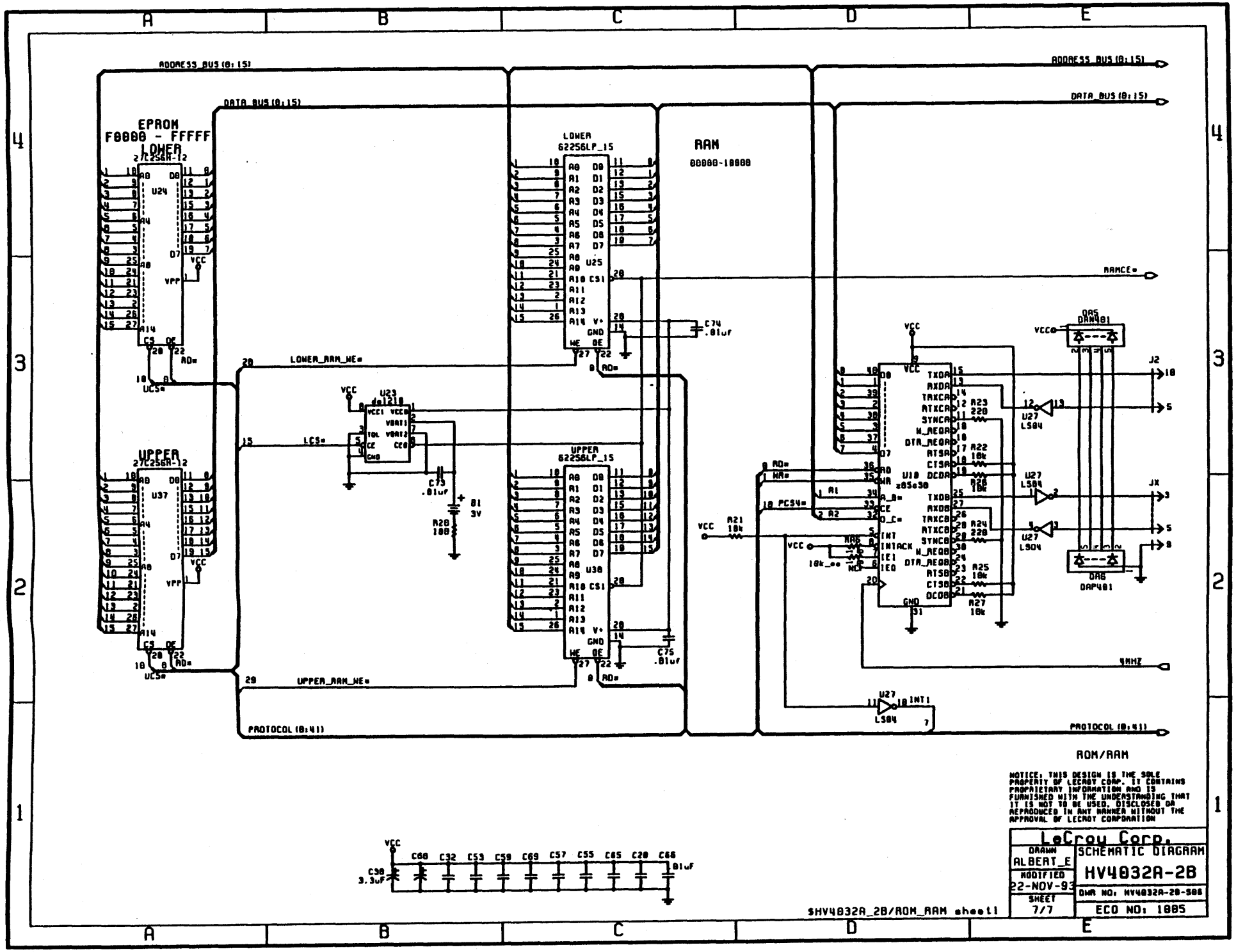
LeCroy Corp.
DRAWN ALBERT_E
MODIFIED 22-NOV-93
SHEET 6/7
SCHEMATIC DIAGRAM
HV4032A-2B
DWG NO: HV4032A-2B-507
ECO NO: 1885
$HV4032A_2B/MUX_D_CHANNEL_OUTPUT sheet1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DATA_BUS(0:15)
EPROM
F0000 - FFFFF
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U24
UPPER
27C256R-12
U37
UCS=
AD=
LOWER_RAM_WE=
UPPER_RAM_WE=
LCS=
PROTOCOL(0:41)
LOWER
62256LP_15
U25
UPPER
62256LP_15
U30
RAM
80000-18000
C74
.01uF
C75
.01uF
C73
.01uF
U23
dal210
B1
3V
R20
10Ω
RAMCE=
VCC
R21
10k
U18
z85c30
RD
WR
A/B=
CE
D/C=
INT
INTACK
IEI
IEO
TXDA
RXDA
TRXCA
RTXCA
SYNCA
W_REQA
DTR_REQA
RTSA
CTSA
DCDA
TXDB
RXDB
TRXCB
RTXCB
SYNCB
W_REQB
DTR_REQB
RTSB
CTSB
DCDB
GND
R22
10k
R23
220
R24
220
R25
10k
R26
10k
R27
10k
10k_ea
U27
LS04
DAS
DAP401
J2
JX
PCS4=
RD=
WR=
A1
A2
INT1
$MHZ
PROTOCOL(0:41)
ROM/RAM
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LeCroy Corp.
DRAWN
ALBERT_E
MODIFIED
22-NOV-93
SHEET
7/7
SCHEMATIC DIAGRAM
HV4032A-2B
DWG NO: HV4032A-2B-SCH
ECO NO: 1085
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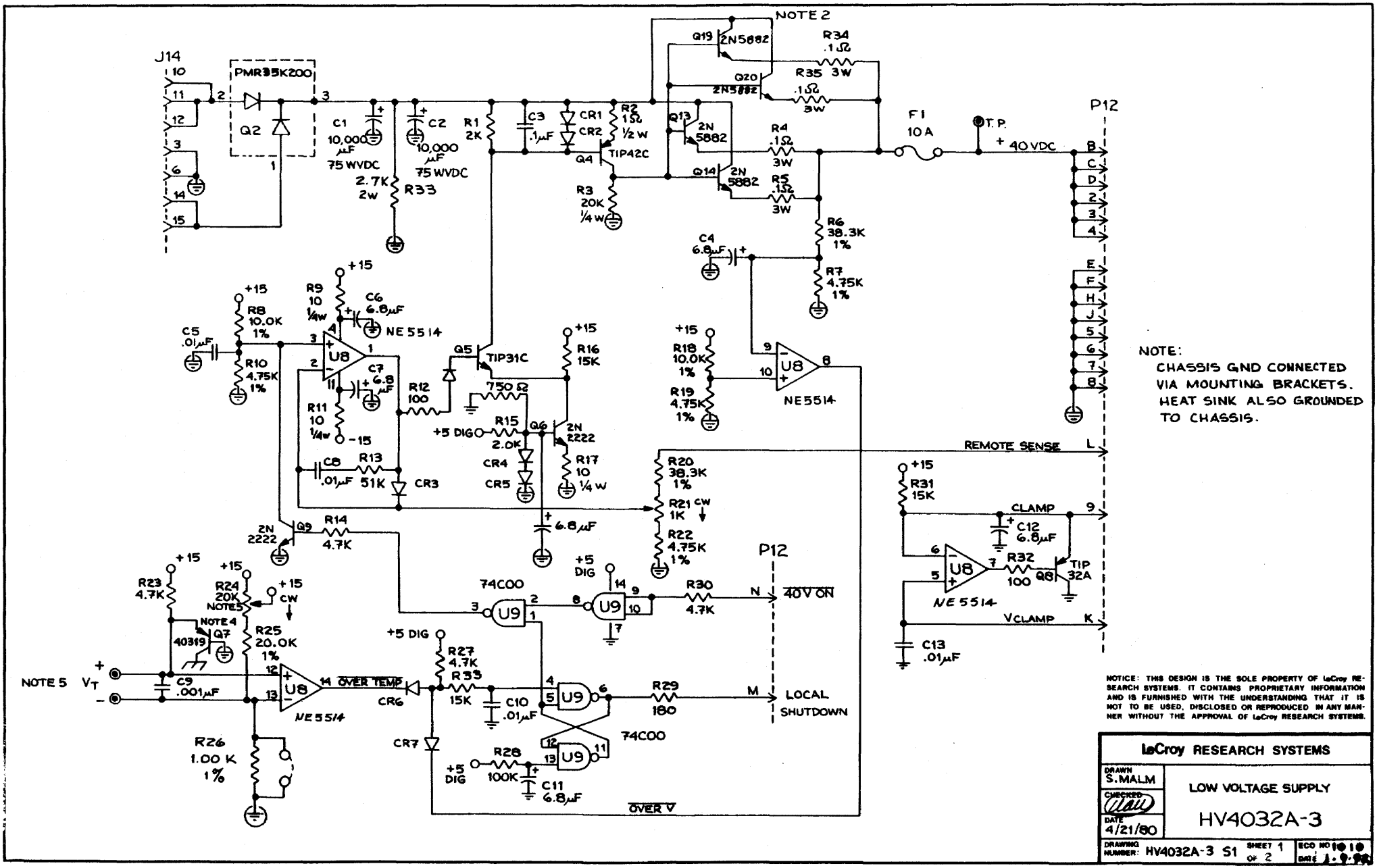
C68
C32
C53
C59
C69
C57
C55
C45
C28
C66
.01uF



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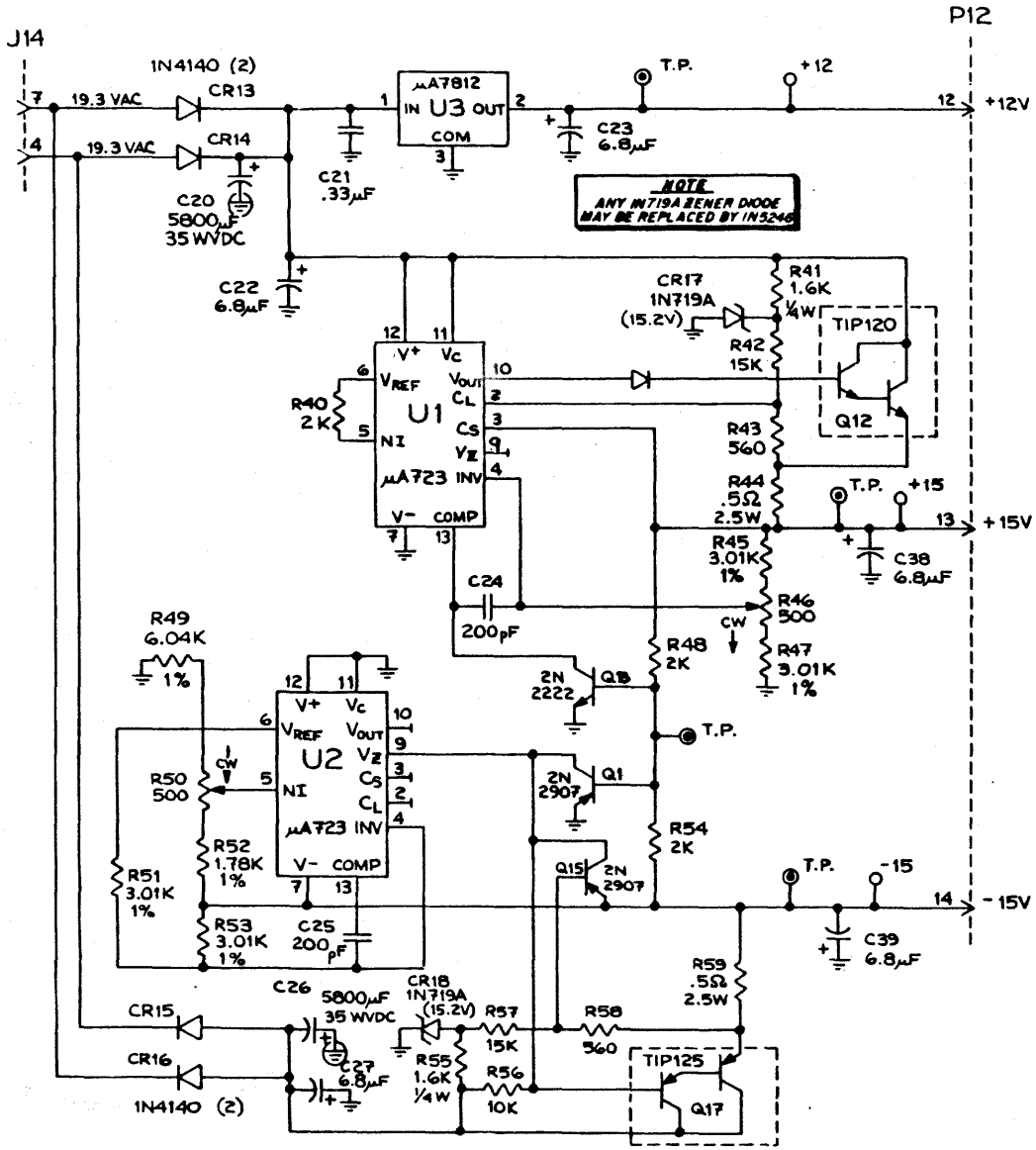
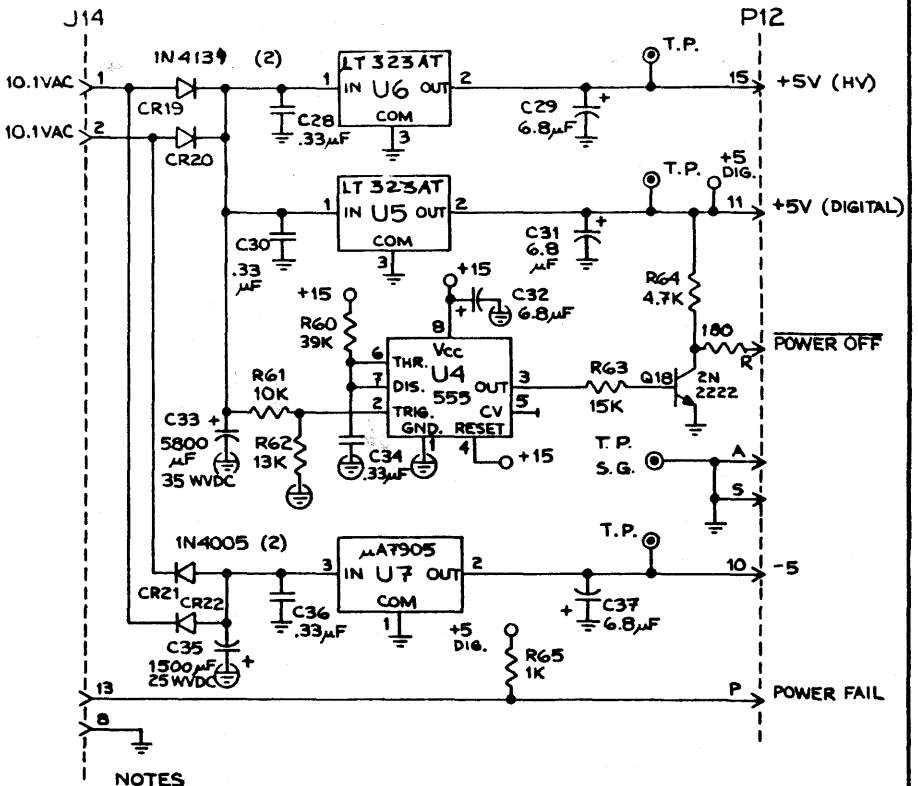
LeCroy RESEARCH SYSTEMS

DRAWN S.MALM	LOW VOLTAGE SUPPLY
CHECKED	HV4032A-3
DATE 4/21/80	
DRAWING NUMBER: HV4032A-3 S1	SHEET 1 OF 2
ECO NO 1010 DATE 1-9-85	





NOTES

1) ALL UNMARKED DIODES ARE 1N4448
2) Q13, Q14, Q19, Q20, 2N5882 MUST ALL BE OF SAME MANUFACTURER TO AID IN MATCHING.
3) REFERENCE DESIGNATION:

	USED	OMITTED
SHT. 1	R1-32, C1-13	R-39, C14-19
	CR1-7	CR8-12
SHT. 2	R40-65, C20-39, CR13-22	R66-, C40-, CR23-

4) Q7 (40319 TEMP. TRANSDUCER) MOUNTED IN PROXIMITY TO Q13
5) ADJUST R24 FOR V_T = 170 mV @ 25°C (HEAT SINK TEMP)
6) µAF 774 MAY BE SUBSTITUTED WITH, TL084

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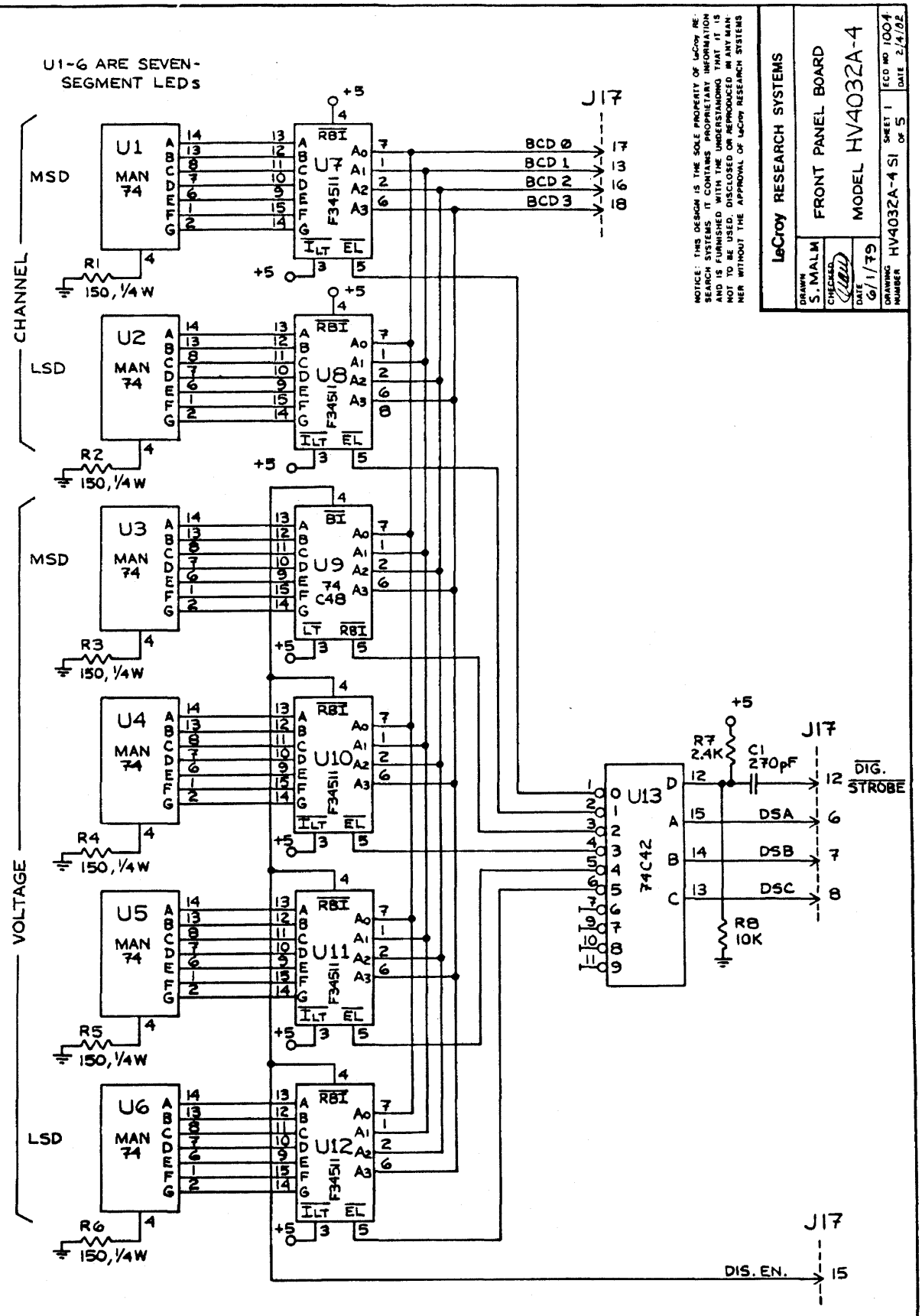
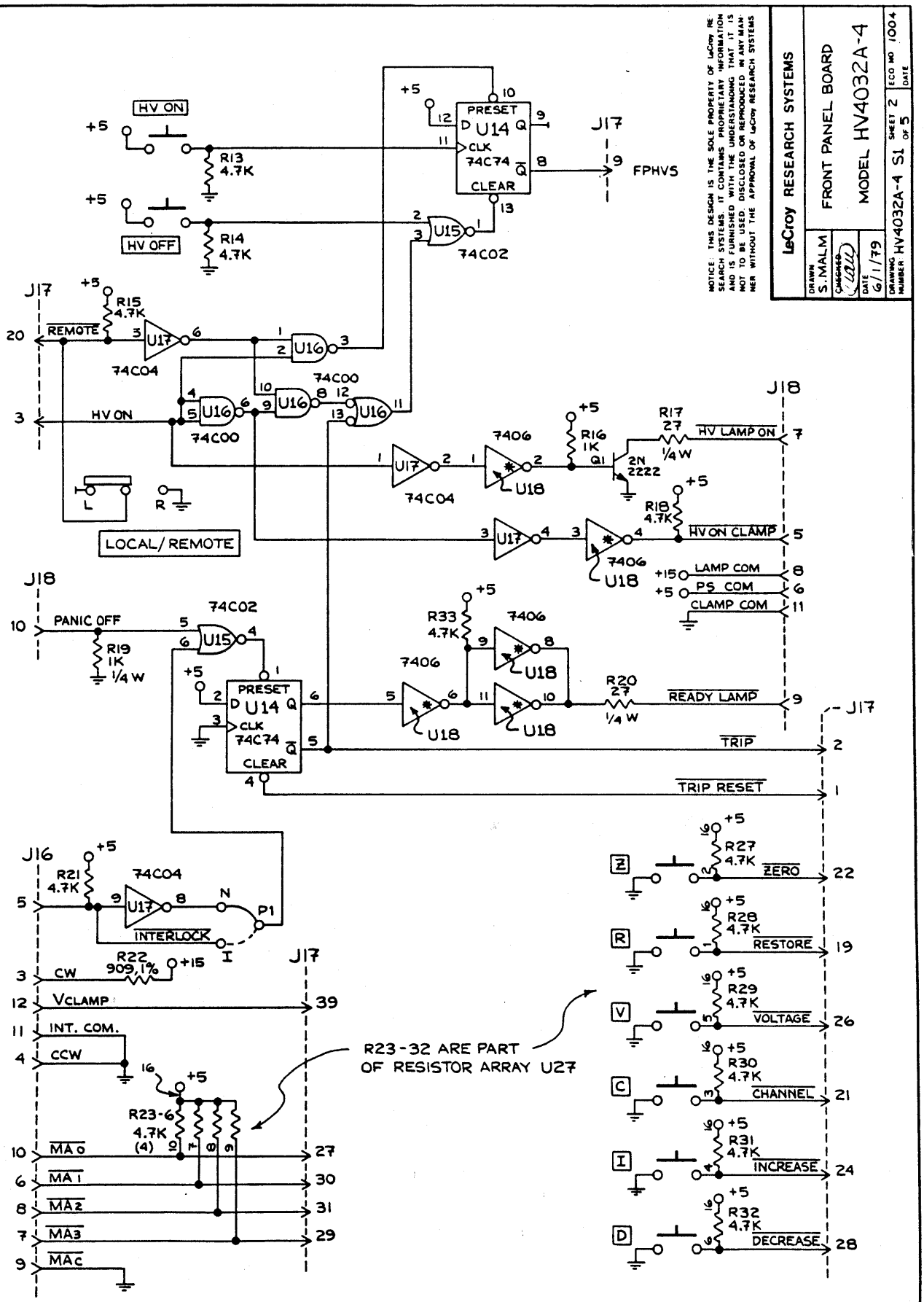
LeCroy RESEARCH SYSTEMS

DRAWN S. MALM	LOW VOLTAGE SUPPLY
CHECKED	HV4032A-3
DATE 4/21/80	
DRAWING NUMBER: HV4032A-3 S1	SHEET 2 OF 2
	ECO NO 1010 DATE 1-9-98


U1-6 ARE SEVEN-SEGMENT LEDs
CHANNEL
VOLTAGE
MSD
LSD
MSD
LSD
U1 MAN 74
U2 MAN 74
U3 MAN 74
U4 MAN 74
U5 MAN 74
U6 MAN 74
R1 150, 1/4W
R2 150, 1/4W
R3 150, 1/4W
R4 150, 1/4W
R5 150, 1/4W
R6 150, 1/4W
U7 F34511
U8 F34511
U9 74C48
U10 F34511
U11 F34511
U12 F34511
U13 74C42
+5
RBI
BI
LT
ILT
EL
J17
BCD 0
BCD 1
BCD 2
BCD 3
R7 2.4K
C1 270pF
R8 10K
DIG. STROBE
DSA
DSB
DSC
DIS. EN.
LeCroy RESEARCH SYSTEMS
FRONT PANEL BOARD
MODEL HV4032A-4
DRAWN S. MALM
CHECKED
DATE 6/1/79
DRAWING NUMBER HV4032A-4 SI
SHEET 1 OF 5
ECO NO 1004
DATE 2/4/82



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LeCroy RESEARCH SYSTEMS

FRONT PANEL BOARD

MODEL HV4032A-4

DRAWN S.MALM

CHECKED

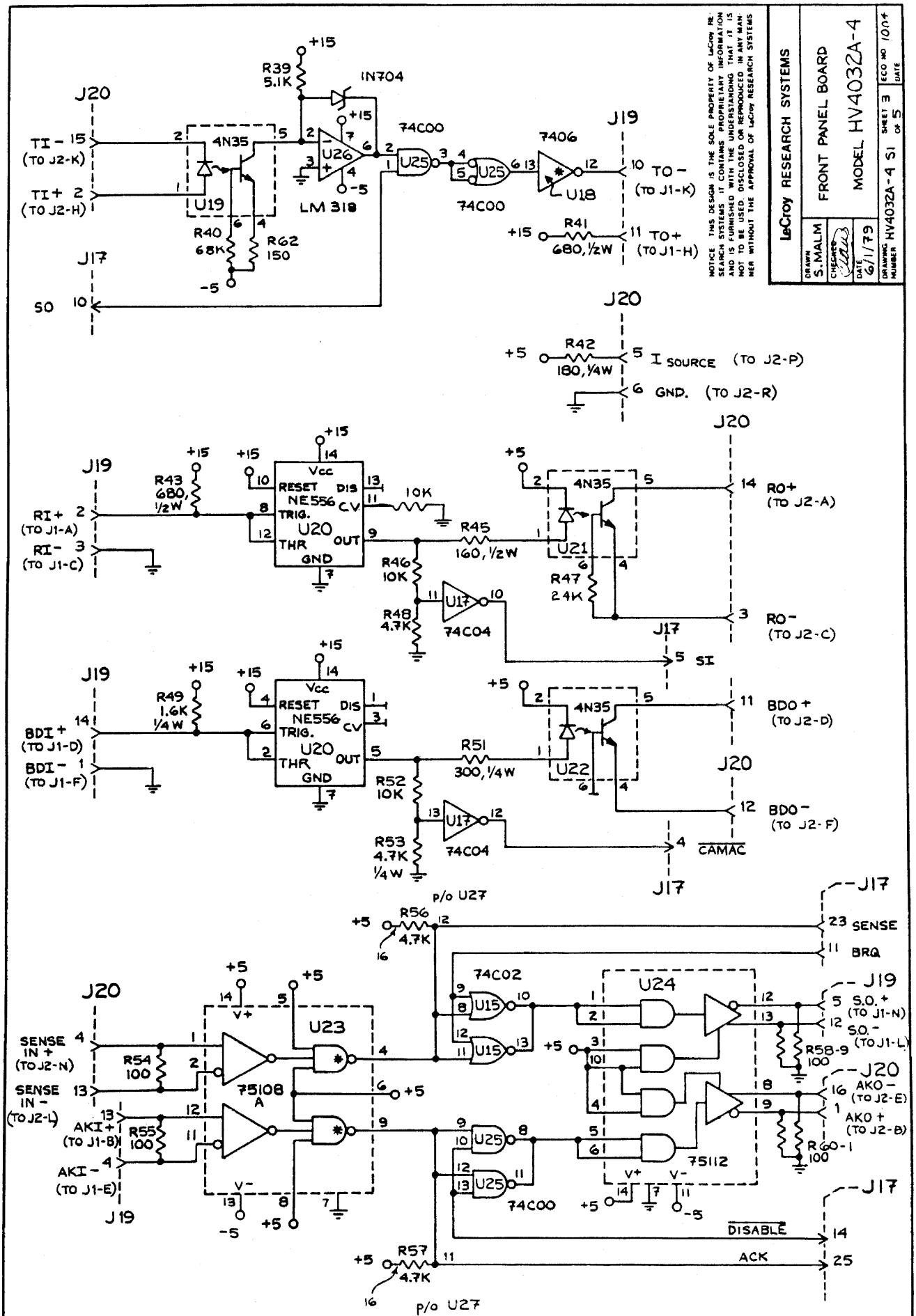
DATE 6/1/79

DRAWING NUMBER HV4032A-4 SI

SHEET 2 OF 5

ECO NO 1004

DATE


LeCroy RESEARCH SYSTEMS
FRONT PANEL BOARD
MODEL HV4032A-4
DRAWN S.MALM
DATE 6/1/79
DRAWING NUMBER HV4032A-4 SI
SHEET 3 OF 5
ECO NO 1004
DATE
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J20
TI - 15 (TO J2-K)
TI + 2 (TO J2-H)
4N35
U19
R40 68K
R62 150
-5
R39 5.1K
+15
IN704
U26
LM 318
74C00
U25
74C00
7406
U18
J19
TO - (TO J1-K)
R41 680, ½W
TO + (TO J1-H)
J17
SO 10
J20
+5
R42 180, ¼W
I SOURCE (TO J2-P)
GND. (TO J2-R)
J19
RI + 2 (TO J1-A)
RI - 3 (TO J1-C)
R43 680, ½W
NE556
Vcc
RESET
DIS
TRIG.
CV
THR
OUT
GND
U20
10K
R45 160, ½W
R46 10K
R47 24K
R48 4.7K
U17
74C04
U21
4N35
RO+ (TO J2-A)
RO - (TO J2-C)
SI
J19
BDI + (TO J1-D)
BDI - (TO J1-F)
R49 1.6K ¼W
R51 300, ¼W
R52 10K
R53 4.7K ¼W
U22
BDO + (TO J2-D)
BDO - (TO J2-F)
CAMAC
p/o U27
R56 4.7K
R57 4.7K
SENSE
BRQ
74C02
U15
U24
S.O. + (TO J1-N)
S.O. - (TO J1-L)
R58-9 100
AKO - (TO J2-E)
AKO + (TO J2-B)
R60-1 100
75112
J20
SENSE IN + (TO J2-N)
SENSE IN - (TO J2-L)
AKI + (TO J1-B)
AKI - (TO J1-E)
R54 100
R55 100
U23
75108 A
V+
V-
DISABLE
ACK
J17
J19
J20

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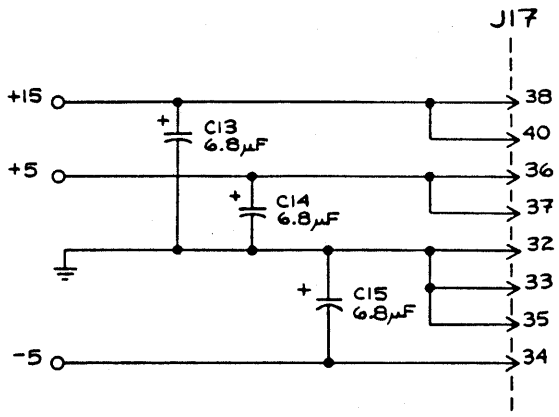
LeCroy RESEARCH SYSTEMS

FRONT PANEL BOARD

MODEL HV4032A-4

DRAWN S.MALM | CHECKED | DATE 6/1/79 | DRAWING NUMBER HV4032A-4 SI | SHEET 4 OF 5 | ECO NO 1004 | DATE



	DEVICE	DESIGNATION	+15	+5	GND.	-5	-15
	74C00	U16, 25		14	7		
	74C02	U15		14	7		
	74C04	U17		14	7		
*	7406	U18		14	7		
	74C42	U13		16	8		
	74C74	U14		14	7		
	75108A	U23		14	7	13	
*	75112	U24		14	7	11	
	F34511	U7,8,10,11,12		16	8		
	NE556	U20	14		7		
	μA741	U26	7			4	
	74C48	U9		16	8		
	4N35	U19,21,22		2			
	898-1-R4.7K	U27		16			

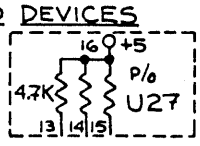
NOTES:

1) * REFERS TO OPEN-COLLECTOR OUTPUTS
2) UNMARKED DIODES ARE IN4448
3) ADDITIONAL .01μF AND 6.8μF, NOT SHOWN, MAY BE USED ON VOLTAGE LINES.
4) REFERENCE DESIGNATIONS:

SHT.#	USED	OMITTED
1	R1-8, C1	R9-R12, C2-4
2	R13-33	R34-38, C5-7
3	R39-62	R63- , C8-12
4	C13-15	C16 -

5) ALL RESISTORS ARE 1/8 W, 5% UNLESS OTHERWISE SPECIFIED.

UNUSED DEVICES



J17

1	$\overline{\text{TRIP RESET}}$
2	$\overline{\text{TRIP}}$
3	HV ON
4	$\overline{\text{CAMAC}}$
5	SI
6	DS_A
7	DS_B
8	DS_C
9	FPHVS
10	SO
11	BRQ
12	$\overline{\text{DIGIT STROBE}}$
13	BCD_1
14	$\overline{\text{DISABLE}}$
15	DIS. EN.
16	BCD_2
17	BCD_0
18	BCD_3
19	$\overline{\text{RESTORE}}$
20	$\overline{\text{REMOTE}}$
21	$\overline{\text{CHANNEL}}$
22	$\overline{\text{ZERO}}$
23	SENSE
24	$\overline{\text{INCREASE}}$
25	ACK
26	$\overline{\text{VOLTAGE}}$
27	$\overline{MA_0}$
28	$\overline{\text{DECREASE}}$
29	$\overline{MA_3}$
30	$\overline{MA_1}$
31	$\overline{MA_2}$
32	SIG. GND.
33	SIG. GND.
34	-5 V
35	SIG. GND.
36	+5V
37	+5V
38	+15V
39	V_{CLAMP}
40	+15V

J16

1	N/C
2	N/C
3	CW
4	CCW (SIG. GND.)
5	$\overline{\text{INTERLOCK}}$
6	$\overline{MA_1}$
7	$\overline{MA_3}$
8	$\overline{MA_2}$
9	$\overline{MA_C}$ (SIG. GND.)
10	$\overline{MA_0}$
11	INT. COM. (SIG. GND)
12	V CLAMP
13	N/C
14	N/C

J18

1	N/C
2	N/C
3	N/C
4	N/C
5	$\overline{\text{HV ON CLAMP}}$
6	P.S. COM. (+5)
7	$\overline{\text{HV LAMP ON}}$
8	LAMP COM. (+15)
9	$\overline{\text{READY LAMP}}$
10	PANIC OFF
11	CLAMP COM. (SIG. GND.)
12	N/C
13	N/C
14	N/C

J19

1	BDI −
2	RI +
3	RI −
4	AKI −
5	SENSE OUT +
6	N/C
7	N/C
8	N/C
9	N/C
10	TO −
11	TO +
12	SENSE OUT −
13	AKI +
14	BDI +

J20

1	AKO −
2	TI +
3	RO −
4	SENSE IN +
5	I SOURCE
6	SIG. GND.
7	N/C
8	N/C
9	N/C
10	N/C
11	BDO +
12	BDO −
13	SENSE IN −
14	RO +
15	TI −
16	AKO +

J16-20 PIN ASSIGNMENTS

N/C - NO CONNECTION

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LeCroy RESEARCH SYSTEMS

DRAWN S.MALM

CHECKED

DATE 6/1/79

FRONT PANEL BOARD

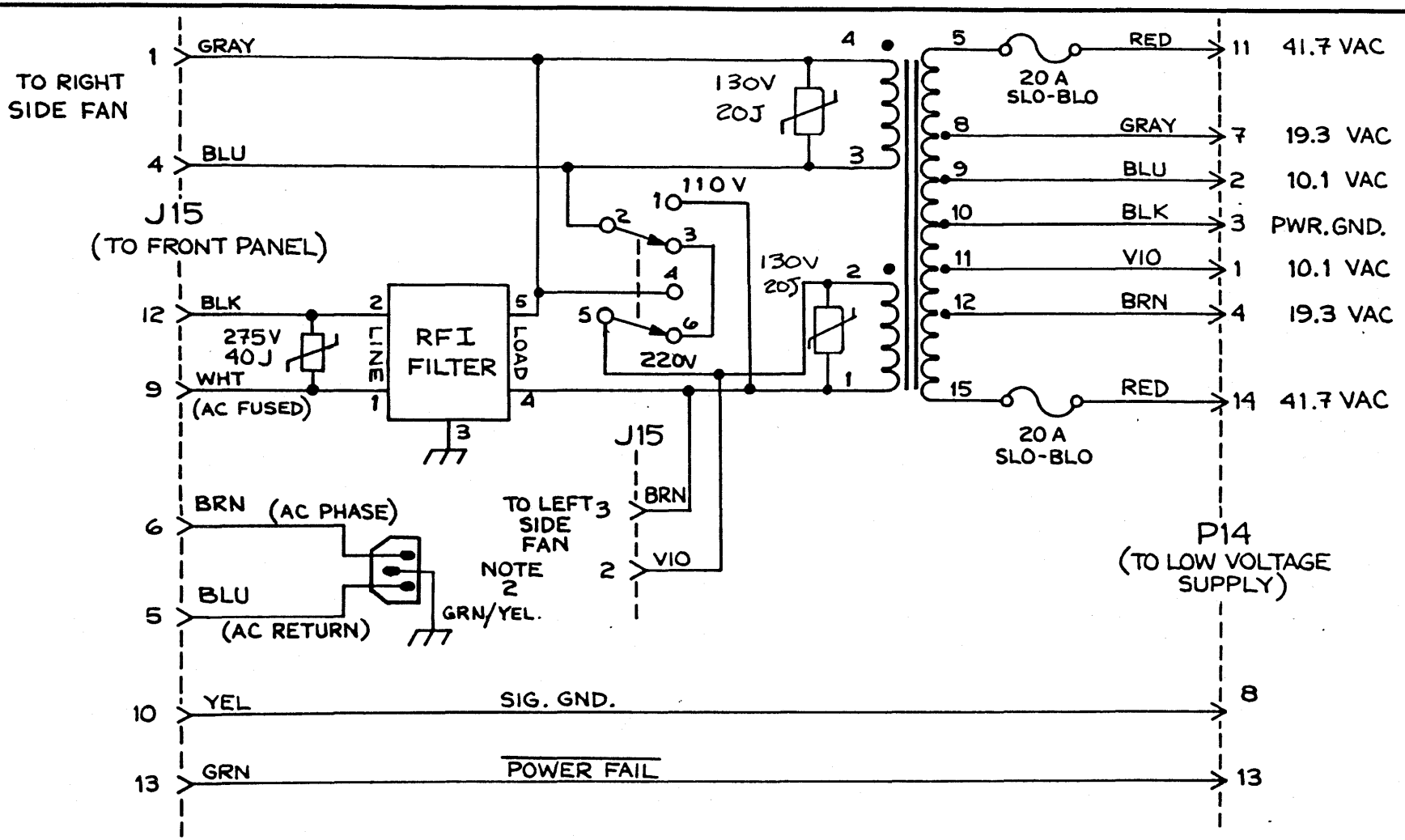
MODEL HV4032A-4

DRAWING NUMBER HV4032A-4 S1

SHEET 5 OF 5

ECO NO 10

DATE



NOTES:

1) ⏚ DENOTES CHASSIS GND.
2) INPUT MAY BE 110 VAC, 50/60 Hz
   OR 220 VAC, 50/60 Hz
3) A.C. VOLTAGES FOR REFERENCE ONLY;
   MEASURED UNLOADED WITH RESPECT TO PWR. GND.

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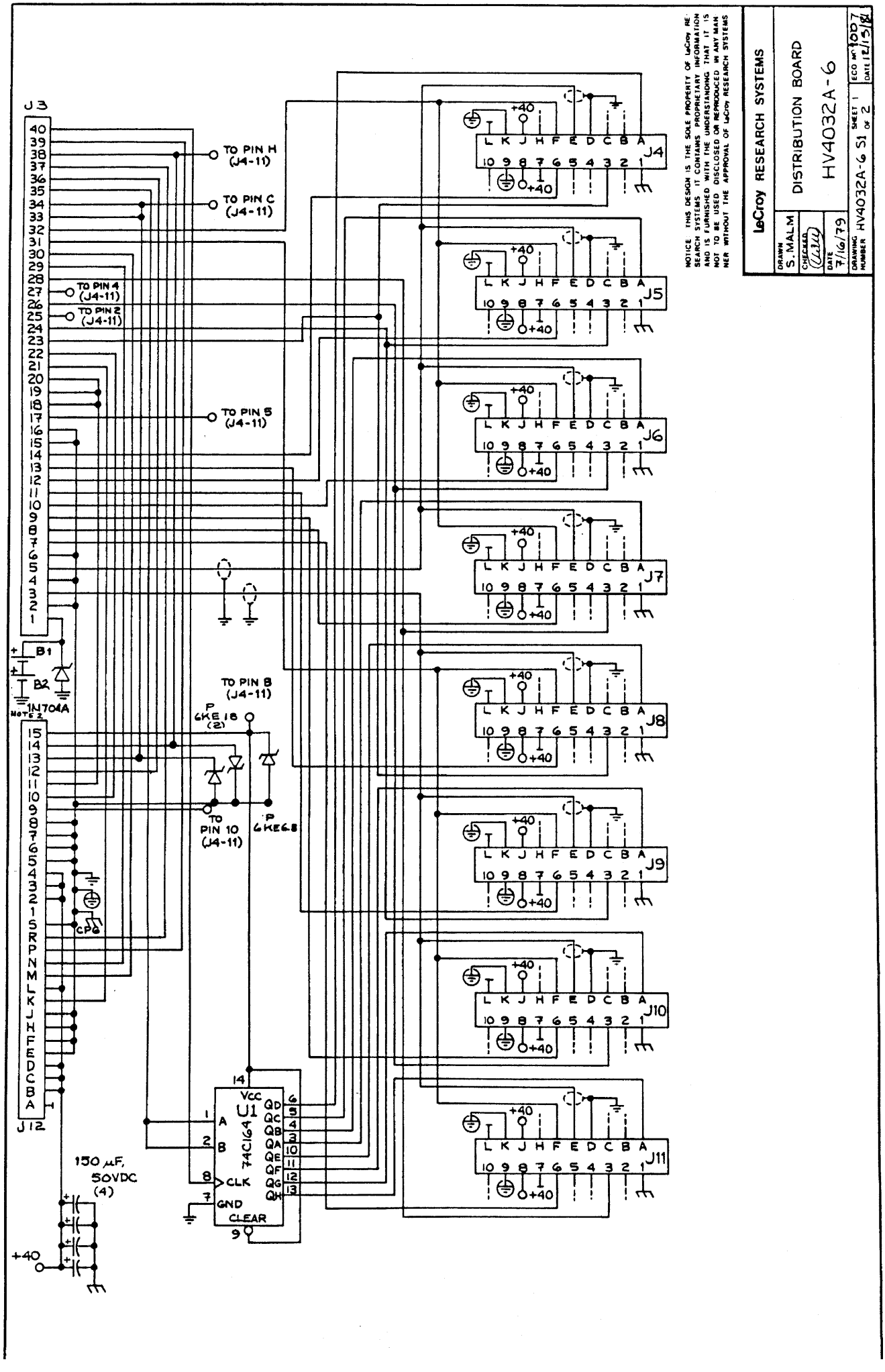
LeCroy RESEARCH SYSTEMS		
DRAWN S.MALM	LEFT SIDE PANEL POWER DISTRIBUTION	
CHECKED		
DATE 8/21/79	HV4032A-5	
DRAWING HV4032A-5-S1	SHEET 1	ECO NO 1006

VIE PRESS BUFFALO NY


LeCroy RESEARCH SYSTEMS
DRAWN S.MALM
CHECKED
DATE 7/16/79
DISTRIBUTION BOARD
HV4032A-6
DRAWING NUMBER HV4032A-6 S1
SHEET 1 OF 2
ECO # 1007
DATE 12/15/81
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J3
J12
J4
J5
J6
J7
J8
J9
J10
J11
TO PIN H (J4-11)
TO PIN C (J4-11)
TO PIN 4 (J4-11)
TO PIN 2 (J4-11)
TO PIN 5 (J4-11)
TO PIN 8 (J4-11)
TO PIN 10 (J4-11)
B1
B2
1N704A
NOTE 2
P6KE18 (2)
P6KE6.8
CP9
150 µF, 50VDC (4)
+40
U1
74C164
VCC
GND
CLEAR
CLK
QA
QB
QC
QD
QE
QF
QG
QH

J3 PIN ASSIGNMENTS

1	BATTERY +	21	V CLAMP
2	SIGNAL GND.	22	-5V
3	LOWER VM	23	Q1
4	SIGNAL GND.	24	Q2
5	UPPER VM	25	A
6	SIGNAL GND.	26	Q3
7	J11 CONTROL	27	B
8	J7 "	28	Q4
9	J10 "	29	$\overline{\text{40V ON}}$
10	J6 "	30	LOCAL SHUTDOWN
11	J9 "	31	LOWER ENABLE
12	J5 "	32	UPPER ENABLE
13	J8 "	33	+15 V
14	J4 "	34	+15 V
15	SIGNAL GND.	35	62.5 KHz
16	SIGNAL GND.	36	+12 V
17	QUAD POD	37	$\overline{\text{POWER OFF}}$
18	+5V (DIGITAL)	38	-15 V
19	+5V "	39	$\overline{\text{POWER FAIL}}$
20	+5V "	40	500 KHz

J4-11 PIN ASSIGNMENTS

1	CHASSIS GND.
2	A
3	Q
4	B
5	QUAD POD
6	DAC
7	N/C
8	+40V
9	POWER GND.
10	CLAMP
A	SYNC. PULSE
B	+5V (HV)
C	+15V
D	SIGNAL GND.
E	VM
F	ENABLE
H	-15V
J	+40V
K	POWER GND.
L	N/C

J12 PIN ASSIGNMENTS

1	N/C	A	N/C
2	+40V	B	+40V
3	+40V	C	+40V
4	+40V	D	+40V
5	POWER GND.	E	POWER GND.
6	" "	F	" "
7	" "	H	" "
8	" "	J	" "
9	CLAMP	K	V CLAMP
10	-5V	L	REMOTE SENSE
11	+5V (DIGITAL)	M	LOCAL SHUTDOWN
12	+12V	N	$\overline{\text{+40V ON}}$
13	+15V	P	$\overline{\text{POWER FAIL}}$
14	-15V	R	$\overline{\text{POWER OFF}}$
15	+5 V (HV)	S	SIGNAL GND.

N/C = NO CONNECTION

NOTES:

1) GROUND SYMBOLS:

⏚ SIGNAL GND.

⊜ POWER GND.

⏚ CHASSIS GND.

CPG - COMMON POINT GND. - JUNCTION OF ALL GROUNDS

2) B_1, B_2 - EVEREADY NO. CH35 (1.2V, 1.2 AMP. HR.) - LOCATED ON RIGHT SIDE PANEL OF HV4032A MAIN FRAME.

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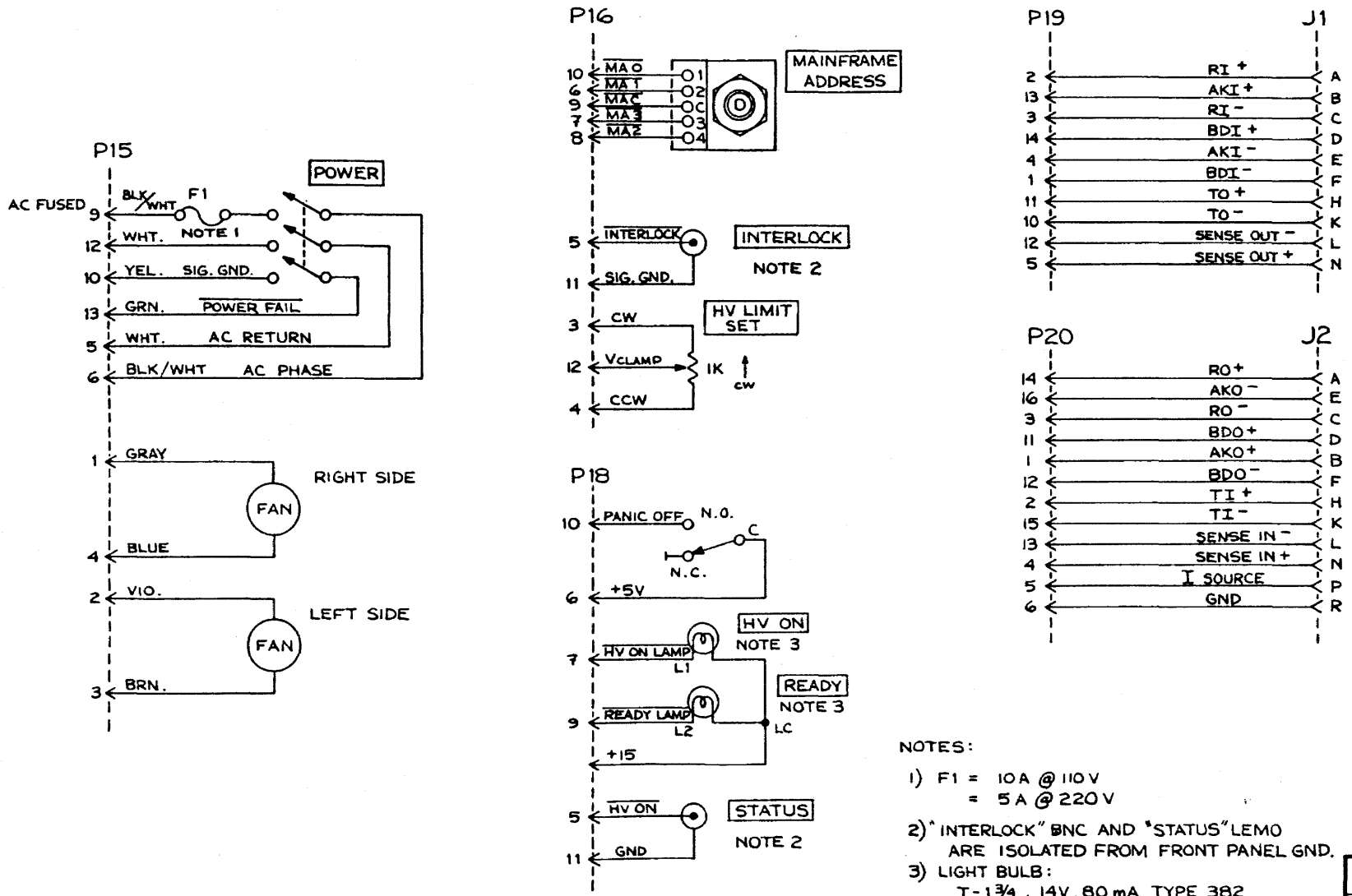
LeCroy RESEARCH SYSTEMS		
DRAWN S.MALM	DISTRIBUTION BOARD	
CHECKED	HV4032A-6	
DATE 7/16/79		
DRAWING NUMBER HV4032A-6 S1	SHEET 2 OF 2	ECO # 1007 DATE



NOTES:

1) F1 = 10A @ 110V
   = 5A @ 220V
2) "INTERLOCK" BNC AND "STATUS" LEMO ARE ISOLATED FROM FRONT PANEL GND.
3) LIGHT BULB:
   T-1 3/4, 14V, 80mA TYPE 382

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LeCroy RESEARCH SYSTEMS

DRAWN S.MALM	FRONT PANEL (NON-BOARD MOUNTED)
CHECKED	HV4032A-8
DATE 8/20/79	
DRAWING NUMBER HV4032A-8 S1	SHEET 1 OF 1
ECO NO 1004	DATE 10/30/81

ADDENDUM TO THE HV4032A HIGH VOLTAGE SYSTEM MANUAL

Introduction

As of July 1991, the CPU board in the HV4032A/M high voltage mainframe (designated as HV4032A-2) has been replaced by a new CPU board (HV4032A-2B). Although the theory of operation description in the manual is no longer completely accurate, the functionality of the two are identical. The user will not observe any differences between systems using the old or new version CPU boards.

The new CPU board is a drop-in replacement for the original F8 microprocessor board. Due to the loss of availability of the F8 chip set and other parts, the new board was designed to use fewer and more commonly available parts based on the Intel 80186 microprocessor. The higher clock speed and increased functionality of the 80186 over the F8 allowed the internal DMA feature and a simple two stage pipeline latch to replace the recirculating FIFO's of the old design. Also a modern 16-bit DAC and ADC replace many discreet components with increased accuracy and make the board easier to assemble.

By maintaining the boards functional identities, the Operators Manual is affected in only 4 areas. These are:

1) the Baud Rate for TTY I/O; 2400 Baud was added.
2) the location of Baud Rate and Option jumpers.
3) the CMOS memory battery-life length and replacement.
4) the self-test and TEST MODE features.

ADDITION OF THE 2400 BAUD RATE FOR TTY I/O

The original board had two detectable jumper positions for the TTY BAUD RATE option at JB1. The new board retains the original two options in the same relative configuration, but can also detect the removal of the jumper entirely, thereby envoking the new 2400 Baud Rate fir TTY/Terminal connections. However the current-loop front end is maintained for compatibility, and there are low cost commercially available RS-232 voltage to current-loop converters which may be used to interface the entire mainframe daisy-chain to modern terminals. The selection of 2400 Baud is because the most available and reliable phone-line modems are 2400 Baud, for the really remote applications.

THE LOCATION OF BAUD RATE AND OPTION JUMPERS

Due to the new physical layout dictated by the new components of the CPU board, all of the option jumpers and diagnostic connections were grouped together for easy location in the front right corner of the CPU board.

JA1: RESET, is a LeCroy diagnostic forcing the 80186 into a Reset-state by shorting the pins together; the user should never use this jumper option. (If for any reason these pins are shorted together, the processor will not run until they are seperated.)

JB1: BAUD, is a 3-position jumper - placing the shunt jumper to the left (pins 2 and 3) selects 110 Baud; placing the shunt jumper to the right (pins 1 and 2) selects 300 Baud; if the shunt is removed and left hanging off one pin (for storage) 2400 Baud is selected.

JC1: OPTION, is a 3-position jumper - placing the shunt jumper to the left (pins 2 and 3) selects the Report Errors Option; placing the shunt jumper to the right (pins 1 and 2) will prevent errors from being reported until requested by a status command. (There should always be a jumper in place between two of the pins for the system to operate reliably, however a missing jumper will usually be treated as if one were present between pins 1 and 2.)

JX: Un-named, is a new LeCroy diagnostic 10-pin connector for a PC-AT serial port connection. The user should never try to attach anything to this connector.

Additionally, several test points were added:

TP1: +15V, for checking the +15 volt power supply.
VCC, for checking the +5 volt power supply.
AGND, analog ground reference point.
-5V, for checking the -5 volt power supply.
-15V, for checking the -15 volt power supply.

THE CMOS MEMORY BATTERY-LIFE LENGTH AND REPLACEMENT

The original design used Ni-Cad batteries and a recharger circuit which was capable of 24 hours of memory back-up, once the unit had been powered on for a considerable time. The new design uses much lower drain CMOS RAM memories and a Lithium Coin Cell in a battery holder. There is no recharge circuit because Lithium cells cannot be recharged, and the lower memory current drain means the cell life can be measured in months (possibly years). Additionally, there is no minimum power-on time required to recharge the batteries because the Lithium cell is always ready to work. The cells are low cost and replacable (with power on to save memory contents if needed), and a battery-minder IC only uses battery power when the mainframe is powered off. For long term storage, the Lithium cells can be removed and stored seperately. The Lithium cell is located adjacent to the jumper section in the front right corner of the CPU board, and is installed with the "+" side facing up.

SELF-TEST AND TEST MODE FEATURES

Additional in-field self-testing and user invoked Test Modes were programmed into the firmware on the new CPU board. The new self-testing programmed into the firmware is internal, extensive, continuous, and transparent to the user. The new Test Mode features that are available to the user are invoked the same way as the old board, namely, holding the VOLTAGE push-button depressed during a power-up cycle (usually front-panel key switch activated). The following is the new full check-out procedure to allow the user to verify the functionality of all the front panel controls.

NEW HV4032A BUILT-IN-TEST FORMAT

(IMPORTANT: the procedure outlined below requires the LOCAL/REMOTE slide switch to be in the LOCAL position.)

The HV4032A is put into the test mode by depressing the VOLTAGE push-button while turning on the unit via the key switch. The red HV-ON Lamp should blink on and off twice ending in the display:

00 8421, as long as the VOLTAGE push-button is held.

Release the VOLTAGE push-button, the red HV-ON Lamp should blink, cycling on for 0.1 seconds and off for 0.1 seconds. The on time is used to scope the HV-ON (U42-18) signal to make sure that the DELAY software is operating at 1 mSec per call, or 100 mSec in this case. The LED's should show:

00 00xx, where xx is the position of the MAINFRAME ADDRESS rotary switch.

Twist the MAINFRAME ADDRESS rotary switch through the 16 address positions, observing the value of the VOLTAGE(current) display LED's.

Depress and hold the RESTORE push-button and observe:
1) the HV-ON Lamp goes out
2) the DISPLAY LED's read 00 0357

Release the RESTORE push-button and the system returns to the HV-ON blinking mode with the MAINFRAME ADDRESS displayed.

Depress and hold the CHANNEL push-button and observe:
1) the HV-ON Lamp goes out
2) the DISPLAY LED's read 00 1842

Release the CHANNEL push-button and the system returns to the HV-ON blinking mode with the MAINFRAME ADDRESS displayed.

Depress and hold the INCREASE push-button and observe:
1) the HV-ON Lamp goes out
2) the DISPLAY LED's read 00 2184

Release the INCREASE push-button and the system returns to the HV-ON blinking mode with the MAINFRAME ADDRESS displayed.

Depress and hold the VOLTAGE push-button and observe:
1) the HV-ON Lamp goes out
2) the DISPLAY LED's read 00 8421

Release the VOLTAGE push-button and the system returns to the HV-ON blinking mode with the MAINFRAME ADDRESS displayed.

Depress and hold the DECREASE push-button and observe:
1) the HV-ON Lamp goes out
2) the DISPLAY LED's read 00 4218

Release the DECREASE push-button and the system returns to the HV-ON blinking mode with the MAINFRAME ADDRESS displayed.

Depress and hold the HV ON push-button and observe:

1) the HV-ON Lamp stays on
2) the DISPLAY LED's read 00 c793

Release th HV ON push-button and the system remains in this state because the HV ON push-button sets a flip-flop.

Depress the HV OFF push-button and observe that the system returns to the HV-ON blinking mode with the MAINFRAME ADDRESS displayed.

Depress and hold the PANIC push-button and observe:

1) the HV-ON Lamp goes out
2) the READY Lamp goes out
3) the DISPLAY LED's read 00 8888

Release the PANIC push-button and the system returns to the HV-ON blinking mode with the MAINFRAME ADDRESS displayed.

Slide the REMOTE/LOCAL switch to REMOTE and observe:

1) the HV-ON Lamp goes out
2) the DISPLAY LED's read 00 3579

Return the REMOTE/LOCAL switch to LOCAL and the system returns to the HV-ON blinking mode with the MAINFRAME ADDRESS displayed.

Depress the ZERO push-button and observe:

1) the HV-ON Lamp goes out
2) the DISPLAY LED's read 00 .... (blank display)

The system is now in the normal TEST MODE. Use the INCREASE push-button to select a test. Test selection only goes up, but wraps around.

Tests above #3 require a terminal (or PC in XTALK) operating at 4800 BAUD attached to the Diagnostic Port, JX. These tests are for internal LeCroy Test Department usage only, and are documented elsewhere.

The following new command is for the HV4032A-2B board to stop the digital regulation loop.

LOCAL mode: From the front panel, press the C and V buttons simultaneously and the digital regulation will stop.

REMOTE mode, TTY: Issue a Z from TTY to stop the loop.

REMOTE mode, CAMAC: Issue the HV on/off command with a value of 2 (T=5, M=16, S=2).

Any command that performs a write to the HV4032A/M will cause the loop to start over again. The freeze command must then be issued again to stop the regulation loop.