CICADA SYSTEM SPECIFICATION	DOCUMENT NO. TFTR-H336-REV1	
	PAGE 1 OF	
	DATE- 02/06/86	
SUBJECT Power Conversion Link Repeater Module	PREPARED BY Hsi Feng	

APPROVED BY

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REVISIONS

DATE	DESCRIPTION
2/6/86	To incorporate change to figure 11.6.

1.0 Abstract

The purpose of this specification is to set forth the physical, operational, and electrical characteristics of the Power Conversion Link Repeater Module. This document in conjunction with the reference documents listed in Section 2.0 herein shall set forth the design and construction criteria.

2.0 Reference Documents

2.1 Power Conversion Data Link Protocol, Document #TFTR-10B3-H335.

2.2 IEEE Standard, Modular Instrumentation and Digital Interface System (CAMAC). IEEE Standard #583-1975.

2.3 Printed Circuit Artwork Specification, Document #TFTR-10A2-H53.

2.4 Printed Circuit Board Fabrication and Assembly, Document #TFTR-10A2-H54.

2.5 Electronic Schematic Specification, Document #TFTR-10A2-H55.

2.6 Reliability, Quality Control and Temperature Cycling, Document #TFTR-10A2-H58.

2.7 Power Conversion Power Supply Control Module, Document #TFTR-10B3-H337.

3.0 Introduction

The module, as defined, shall be used to receive, regenerate, retransmit, and analyze encoded data transmissions from which information is to be ultimately used for the control of power conversion power supplies. This module, in conjunction with power supply control modules (reference 2.7), shall be an element of the Central Instrumentation Control and Data Acquisition (CICADA) System to implement a distributed control system through the use of a single transmission cable loop around the Power Conversion area. The link repeater modules shall be stationed in CAMAC crates at the designated CICADA equipment racks in the Power Conversion area.

4.0 Basic Features

4.1 The module shall be equipped with pulse transformer coupled data link input and data link output ports for isolation and maximum common mode rejection.

4.2 The module shall receive and regenerate signal timing for retransmission with minimal delay. The receiver section of the module shall operate simultaneously with the regeneration of the serial data transmission at the module's output port.

4.3 The link repeater module shall contain serial-to-parallel holding registers for the house address and power supply address fields of the serial data word.

4.3.1 The 6 bit link repeater house address field shall be loaded serially into the house address register where it is checked for framing, parity and content. The content of the house address field shall be checked against a 6 bit digital comparator which is programmed to recognize 1 of 63 possible address codes. House address 63 ($3F_{16}$) is the house aggregate address. All link repeater modules shall recognize this address.

4.3.2 A recognized house address shall imply the following:

4.3.2.1 The "ACK" bit of the serial data transmission shall be changed from a "1" to a "0" for the return message that goes back to the source. This change of state in the ACK bit shall indicate that the transmission has been accepted by the link repeater module which shall pass the remaining part of the serial data transmission to the power supply controller module. (See reference 2.1).

4.3.3 The house address shall be programmed by a 6 PST "dip" switch on the link repeater module.

4.3.4 House Subaggregate Codes.

For special cases, it may be desired to implement control only on a specific set of power supplies via house subaggregate addressing. House subaggregate codes have been designated thus:

TF System; 111110_2

EF System; 111101_2

OH System; 111011_2

The subaggregate house address codes shall be implemented by isolating one input to the aggregate house detector NAND gate which represents the zero (0) bit in the subaggregate code. The isolated input shall be tied to a logic 1 level. For this method to be effective, only one zero bit per subaggregate code is permitted. See 5.10, and figure 11.6.

4.4 The module shall have front panel LED's that shall indicate the following. (See Figures 11.1 and 11.2).

4.4.1 House Address

Six (6) LED's shall continuously indicate for which binary house address the link repeater module has been set to recognize as programmed by an on board "dipswitch".

4.4.2 Link On

This LED shall light up for sustained series of serial data transmissions.

4.4.3 Local Test

Indicates if the module is in the local test mode (see paragraph 4.5).

4.4.4 HA

This LED shall flash for 200ms when the module has recognized the house address on a serial data transmission for which it has been programmed as per paragraph 4.4.1.

4.4.5 HA AGG

This LED shall flash for 200ms when the module has recognized the house aggregate address of $3F_{16}$. See reference 4.3.1.

4.4.6 PSA

This LED shall flash for 200ms when the power supply address field of the received serial data transmission has passed framing and parity checks.

4.4.7 PSA ERR

This LED shall flash for 200ms when a power supply field parity error has been detected.

4.4.8 PSA AGG

This LED shall flash for 200ms when the PSA aggregate address is detected.

4.4.9 HAP ERR

This LED shall flash when a house address field parity error has been detected.

4.5 The module shall have a local test mode whereby the module is taken off line without interrupting the continuity of the data link. The local test mode is selected via the local test input connector on the front panel. This connector (Lemo #RA1.306NYL) shall permit injection of test signals and messages for troubleshooting purposes. See Figures 11.1 and 11.2.

4.6 The module shall have the following test point output pin jacks for troubleshooting. See Figure 11.2.

4.6.1 IN

This test point shall allow the user to examine the incoming data link wave forms. This signal is extracted from a tertiary winding of the input pulse coupling transformer for isolation and is short circuit protected via a 470 ohm series resistor to prevent an accidental "loading down" of the data link.

4.6.2 RESHAPE

This test point allows the user to examine the regenerated return signal prior to the bi-polar encoding by the output driver stage.

4.6.3 OUTPUT

This test point allows the user to examine the data link wave form as generated by the bi-polar output driver stage of the module. This test point is extracted from a tertiary winding for isolation. The test point is short circuit protected by a 470 ohm series resistor.

4.7 The module shall relay all serial data transmissions received intact with the following exceptions.

4.7.1 If the module detects a house address parity error, the regeneration of the relayed transmission shall cease with the last clock pulse of the house address field.

4.7.2 If the module detects a power supply address parity error, the regeneration of the relayed transmission shall cease with the last clock pulse of the power supply address field.

4.7.3 If the module detects a data field parity error during a READ operation, the last clock pulse of the data field shall be suppressed.

4.8 The link repeater module shall interface up to six (6) power supply controller modules via a front panel shielded, multi-conductor connector (Lemo #RA0.304NYLS4.2) in a parallel circuit configuration. The signals that are carried by this cable are described in paragraph 6.7.

4.8.1 The I/O signals of the link repeater module shall drive the I/O ports of the Power Supply Controller modules (reference Figure 11.5 of document 2.7) in a parallel, daisy chain fashion via shielded 4 conductor cable and connectors. (See Figure 11.1 of reference 2.1).

4.8.2 The signals are patched from module to module via patch cord assemblies normally consisting of a three inch (3") length of Belden #83347 (or equivalent) 4 conductor shield cable terminated with a Lemo #F0.304NYLS/4.2 connector at each end. Maximum length of any one patch cord shall not exceed twelve inches (12").

5.0 Mechanical Characteristics

5.1 The module shall be a single width (single slot) module.

5.2 The module shall conform to the mechanical specifications as indicated in reference 2.2.

5.3 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. See reference specification 2.3.

5.4 This module shall be equipped with all of the necessary hardware for insertion into a standard CAMAC crate. See reference specification 2.2.

5.5 All electrical components are to be mounted on only one side of the board.

5.6 The status of the module is to be monitored by front panel LED indicators. Figures 11.1 and 11.2 illustrate the layout and designation of those LED's.

5.7 The test points mentioned in Section 4.6 shall be mounted and designated on the front panel as per Figure 11.2.

5.8 All components are to be assigned an identifying part number (i.e., R1, R2, C1, U20, etc.) which is to be cross referenced with the manufacturer's part number on the schematic.

5.9 The 36 pin card edge connector (auxiliary connector) must mate with a Viking 3V18 or equivalent. The pin assignments for this connector are listed in Figure 11.4.

5.10 Any Link Repeater Modeule which is programmed to implement house sub-aggregate codes as per 4.3.3 shall be labeled as such on the module front panel with a Di-graph (TF, EF, or OH). The Di-graph shall be applied with an engraver or punch.

6.0 Electrical Characteristics

6.1 The module shall derive its required power from the +6, -6, +24, and -24 volt CAMAC power supply voltages on the dataway.

6.2 The module shall not interfere with the CAMAC link for the crate in which the module is installed. This module uses the dataway for power only.

6.3 The module shall receive, decode, and relay serial data transmissions as per the protocol defined in reference 2.1.

6.4 The threshold of the data link receiver portion of this module shall be 4.4 volts P-P $\pm$ 10%.

6.5 The drive capability of the data link output stage shall conform to reference 2.1.

6.6 The +6 volt supply voltage must be bypassed to ground with an electrolytic capacitor of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed to ground by an electrolytic capacitor of at least 6.8 microfarads. In addition, there shall be at least one (1) Vcc (+5 volt) to ground ceramic bypass capacitor of .01 microfarad for every two (2) integrated circuits on the module. The .01 microfarad capacitors shall be located as close as possible to the integrated circuits.

6.7 The link repeater shall send the following four (4) signals to the power supply controller module(s) via the I/O front panel connector. See Figure 11.3.

6.7.1 CLOCK (Output)

This signal shall be derived and separated from the data pulses of the serial data transmission. (See Figure 11.3 and Figure 11.5).

6.7.2 DATA (Output)

The data pulses shall be derived from the serial data transmission and shall be clocked into the serial to parallel data holding registers of the power supply controller module(s). (See Figure 11.3 and Figure 11.5).

6.7.3 ENABLE (Output)

This signal shall assume the logic 0 level when the link repeater module has recognized the house address field of the serial data transmission. This logic level change shall change on the trailing edge of the tenth (10th) clock pulse of the serial data transmission if the condition mentioned is satisfied. Enable allows data to be clocked into the data registers of the power supply controller module.

6.7.4 CLOCK and DATA (Input)

The clock and data line is the logical "OR" of the signals described in references 6.7.1 and 6.7.2 for "WRITE" transmissions. For "READ" transmissions, this line is the logical "OR" of paragraph 6.7.1 with the logical "AND" of 6.7.2 and the data from the output parallel to serial register of the power supply controller module.

6.8 The operation of the link repeater module is illustrated by the block diagram in Figure 11.5.

6.9 The link repeater modules shall be capable of relaying transmissions over twinax cables (Trompeter #TWC-78-2) that shall not exceed 300 feet in length between modules.

6.10 Up to twenty (20) link repeater modules may be connected in series via the maximum cable lengths specified without signal amplitude, timing, or error rate degradation.

6.11 The modules shall be designed to limit transmission I/O errors to less than one in 10^9 transmissions.

7.0 Environmental Data

7.1 The module must operate, as defined, over an ambient temperature range of 0 to +50°C.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 100 gauss per second with a peak magnitude of 200 gauss in any direction.

7.4 The module must operate, as defined, in a radiation environment as follows:

Neutrons	2×10^{7} n/CM^2/sec
Rad-dose	5×10^{-2} rad (Si)/sec
Integrated Dose	200 rad (Si)

8.0 Safety

8.1 All components of this module must be of flame retardant materials.

9.0 Testing

The testing of this module shall be conducted with a test station that is capable of generating and receiving test transmissions as per the protocol in reference 2.1. The timing and control logic in the link repeater module shall be chekced with a calibrated oscilloscope as per the check points marked on the schematic. The full operational testing can be done with a known working power supply controller module (TFTR-10B3-H337). Test transmissions with house address fields either equal or not equal to the hardwired address code to which the link repeater is programmed shall be used to check its functional operation. After functional tests are completed, the link repeater module shall be tested while connected to a known good power supply module

(H337) and operated in an environmental chamber where the module shall undergo continuous operation between each temperature extreme (as per reference document 2.6). The timing of the serial data transmissions used in the test shall not deviate beyond the limits as per Figure 11.4 of reference 2.1.

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ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT: POWER CONVERSION LINK REPEATER MODULE H336 FRONT PANEL HOLE LAYOUT

NAME: J. POLLOCK

DATE: 10-08-80

REVISION DATE:

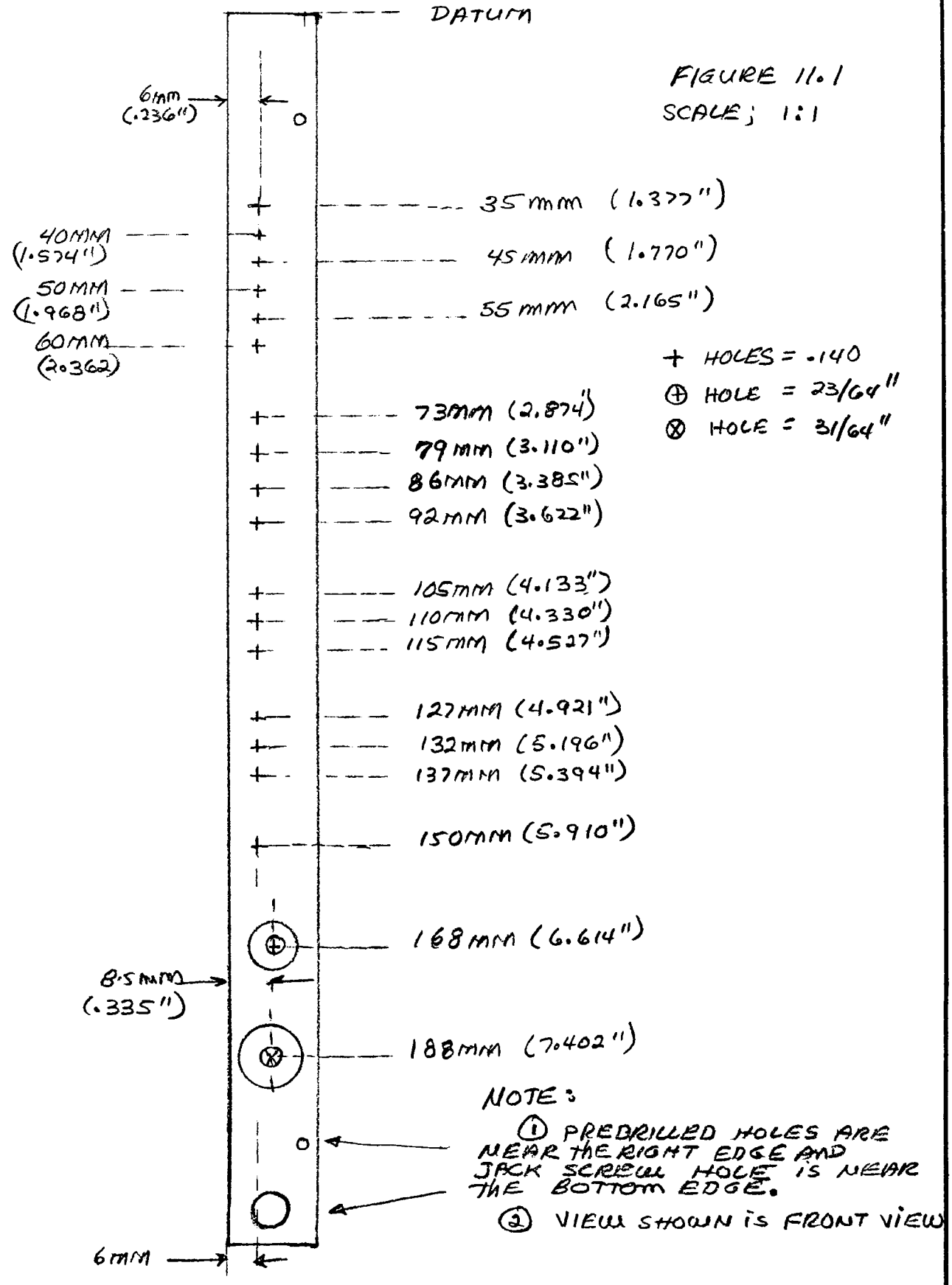

FIGURE 11.1

SCALE; 1:1

+ HOLES = .140

⊕ HOLE = 23/64"

⊗ HOLE = 31/64"

NOTE:

① PREDRILLED HOLES ARE NEAR THE RIGHT EDGE AND JACK SCREW HOLE IS NEAR THE BOTTOM EDGE.

② VIEW SHOWN IS FRONT VIEW

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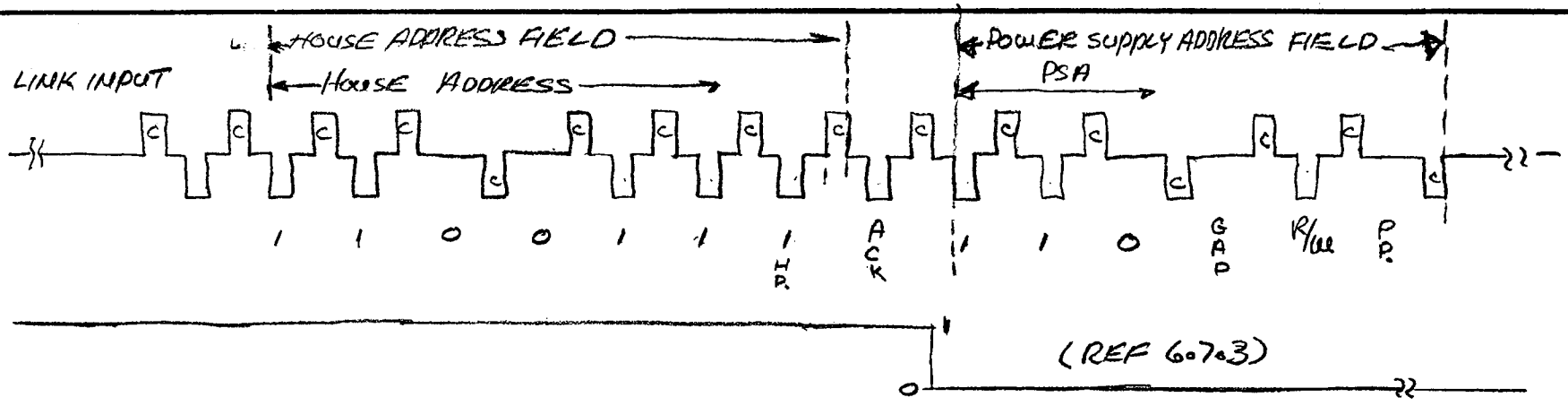
ENGINEERING NOTE

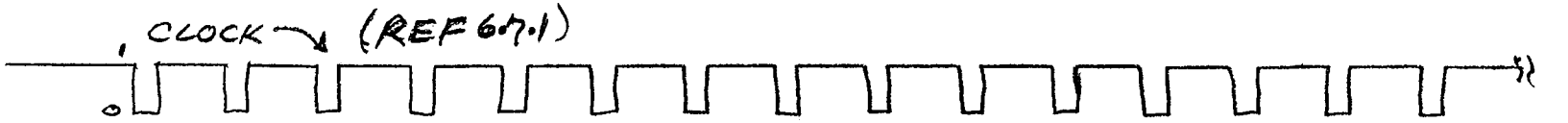
PROJECT | SERIAL-CATEGORY | PAGE

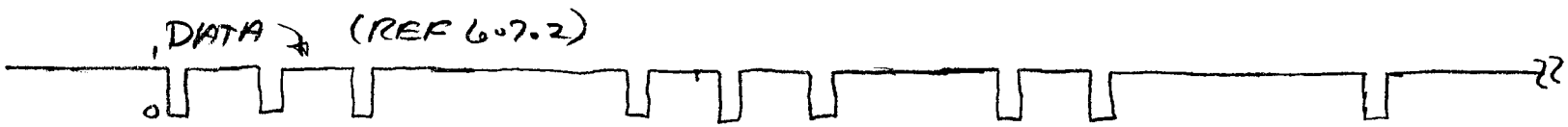
NAME J. Pollock
DATE 10-10-80

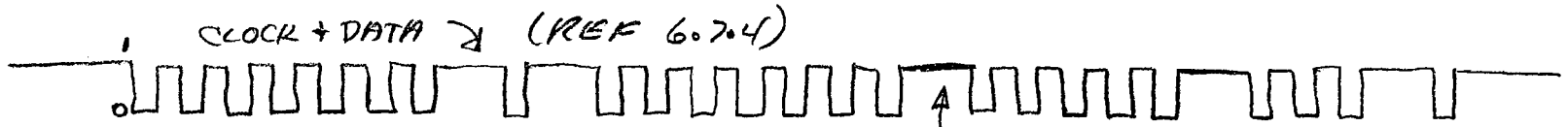
REVISION DATE

SUBJECT
Power Conversion Link Regenerative Module
I/O Connector Wave Forms.









NOTE THAT "ACK" BIT IS RETURNED AS A "Ø" SEE SPEC TFTR- - SECTION 6.7.2.4

FIGURE 1123

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ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT: POWER CONVERSION LINK REPEATER MODULE AUXICIARY CONNECTOR PIN ASSIGNMENT

NAME: J. POLLOCK

DATE: 10-10-80

REVISION DATE:

	B	A	
GROUND	1	1	GROUND
GROUND	2	2	GROUND
GROUND	3	3	GROUND
GROUND	4	4	GROUND
GROUND	5	5	GROUND
GROUND	6	6	GROUND
GROUND	7	7	GROUND
GROUND	8	8	GROUND
LINK INPUT →	9	9	GROUND
LINK INPUT →	10	10	GROUND
GROUND	11	11	GROUND
LINK OUTPUT	12	12	GROUND
LINK OUTPUT	13	13	GROUND
GROUND	14	14	GROUND
GROUND	15	15	GROUND
GROUND	16	16	GROUND
NC	17	17	NC
NC	18	18	NC

VIEW FROM REAR
OF
CRATE

FIGURE 11.4

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ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT: Power conversion Link Repeater Module Block Diagram

NAME: J. Pollock

DATE: 10-14-80

REVISION DATE:

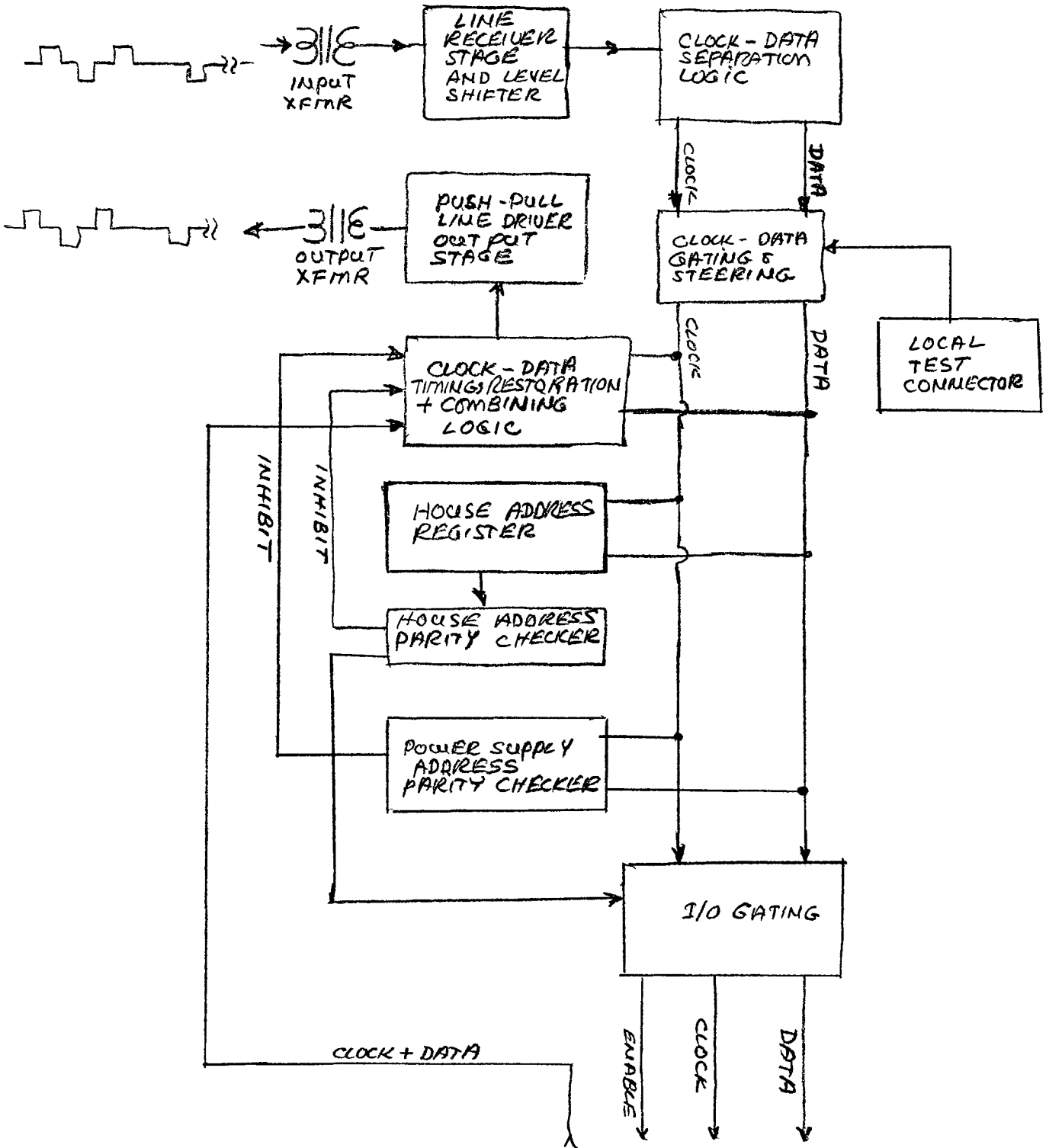


FIGURE 11.5

PRINCETON PLASMA PHYSICS LABORATORY

ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT: POWER CONVERSION LINK REPEATER H336 SUBAGGREGATE HOUSE ADDRESSING.

NAME: J. POLLOCK

DATE: JUNE 11, 1981

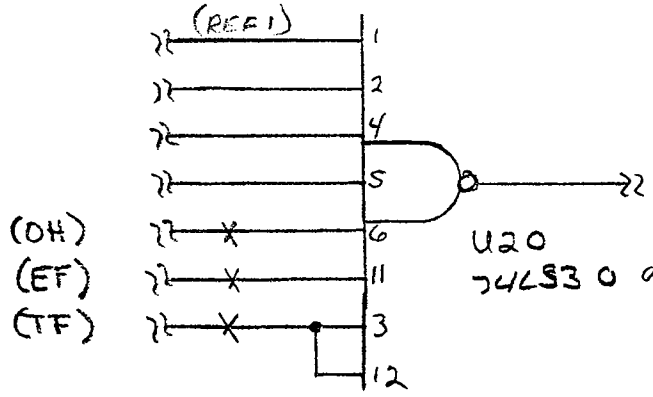
REVISION DATE: 2/5/86

SUB-AGGREGATE HOUSE ADDRESS CODES:

TF SYSTEM = 11110_2

EF SYSTEM = 11101_2

OH SYSTEM = 11011_2



U20
74LS30 on LINK REPEATER MODULE

HOUSE AGGREGATE CODE DETECTOR, U_{20}, on LINK REPEATER MODULE IS DIAGRAMMED TO SHOW WHICH INPUTS MUST BE ISOLATED TO PROVIDE SUBAGGREGATE HOUSE ADDRESSING.

FIGURE 11.6