| | | |
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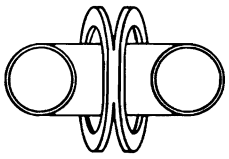
|  CICADA ENGINEERING SPECIFICATION | | DOCUMENT NO. TFTR-10B3-H313A |
| | | PAGE 1 OF |
| | | DATE - 3/30/83 |
| SUBJECT U-Port Adapter and LAM Grader | | PREPARED BY H Del Gatto H. Del Gatto |

## APPROVED BY

Joe Bosco

J. Malohney 4/15/83
CICADA/Computer Division QA

## REVISIONS

| DATE | DESCRIPTION |
|---|---|
| | |

## 1.0 Abstract

This specification, in conjunction with referenced documents, sets forth all characteristics of subject module. This specification shall take precedence where areas of overlap with referenced documents occur. The intended use of this document is to provide a minimum design goal for the module as well as a working document for subsequent users.

## 2.0 Reference Documents

2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975.

2.2 Printed Circuit Board Fabrication and Assembly Specification, Document TFTR-10A2-H54B.

2.3 Electronic Schematic Specification, Document TFTR-10A2-H55.

2.4 Printed Circuit Artwork Specification, Document TFTR-10A2-H53A.

2.5 Reliability, Quality Control and Temperature Cycling, Document TFTR-10A2-H58.

2.6 Facility Clock Subsystem, Document TFTR-10B4-H401.

## 3.0 Introduction

The CAMAC module specified will be used as part of the Central Instrumentation Control and Data Acquisition (CICADA) in support of the Tokamak Fusion Test Reactor (TFTR). The module will be used to interface CAMAC crate controllers with a high speed serial highway link, to intercept and repeat a coded clock system and to encode Look-at-Me (LAM) signals for use by L-2 crate controllers.

## 4.0 Basic Features

The module shall be a single width CAMAC module and shall perform the functions of a 5MHz "U-Port Adapter", 1MHz clock receiver and repeater and "LAM Grader". A block diagram of the module is shown in Figure 11.1 through 11.3.

4.1 The U-Port Adapter circuit shall be used to convert the NRZ data and clock signals to and from the type L-2 crate controllers to a bi-phase coded format as depicted by Figure 11.5. Interface to the crate controller shall be accomplished through use of a single "pig tail" type cable that shall connect to the "D-Output" of the crate controller. A turn around connector will be used on the "D-Input" connector tc make use of the feed through connections provided within the crate controller (See Figure 11.4). Interface to the serial highway shall employ 3-pin LEMO connectors. Pin 1 of the LEMO connectors shall be used for connection to the cable shield and shall be grounded at the transmitting end and open circuited at the receiving end.

The U-Port Adapter circuit of the module shall provide a means of interfacing L-2 Crate Controllers to a modified serial highway system (serial link). The link system shall be made up of two twisted pair transmission lines. The system shall transmit from crate to crate, data in Bi-Phase encoded format along with a synchronous data clock. The Bi-Phase encoding format shall be employed to defeat the low frequency component from the link that is present when NRZ data is used. Misalignment of the data clock and the Bi-Phase data shall be correctable on each U-Port through the use of ten (10) tap delay lines that shall be selectively utilized. The selection of the desired tap is made through use of a PC mounted rotary switch. The tap selection is required to compensate for propagation time differences that may occur between the Bi-Phase and the clock transmission lines. In addition, thecircuit shall have a second delay line that shall be used in a similar fashion to allow the output data link clock and the bi-phase data to be aligned in the same way as the data and clock input signals.

A block diagram of the U-Port Adapter circuit is given by Figure 11.1.

The U-Port Adapter shall make use of relays to "bypass" the U-Port circuitry. The relays shall be configured such that when the relays are in their deenergized (off) state the Bi-Phase Data input and the clock input are routed directly to their respective outputs. When the relays are off the pulse transformers of the U-Port circuitry shall be disconnected from the serial link. A high impedance path shall exist between the serial link and the U-Port receiver circuit. The purpose of the path is to allow an L-2 controller to receive commands even though its companion U-Port is in the "bypassed" state. Responses from crates in bypass will not, however, be transmitted. The bypass relays shall be powered through a series network of a front panel switch and a switching transistor. Both of these series elements must be in their "on" state to allow the relay to energize to put the U-Port/Controller into the "on-line" state. Figure 11.2 depicts the bypass relay coil configuration.

4.2 The Clock Receiver/Repeater circuit shall be used to distribute a nominally 1MHz bi-phase encoded signal. This circuit shall use front panel LEMO connectors to interface to the external clock system. The input and output circuits shall employ transformer coupling with bypass relay function identical to the U-Port Adapter.

The incoming encoded clock shall be interfaced through a front panel LEMO connector. This signal shall be then repeated and retransmitted to both a front panel output connector and to Dataway line P1. In addition, the circuit shall extract the fundamental clock signal from the facility clock and transmit this clock to both a front panel LEMO connector and to Dataway line P2.

4.3 The LAM Grader circuit shall interface to the L-2 crate controller through use of the L-2 SGL connector. The circuit shall encode the 24 bits of LAM data onto the five (5) SGL lines and initiate the generation of a "Demand" message if enabled.

4.3.1 The circuit shall encode in straight binary format the address (N) of the module issuing a LAM.

4.3.2 As LAM's occur the address (N) of the LAM will be "pushed" into a 16 word First In First Out (FIFO) memory for subsequent generation of Demand messages at the maximum speed the link and crate controller allow. If more than one LAM is sensed at any given time the FIFO will be loaded in order of LAM priority. The lowest slot (N) number shall have the highest priority LAM.

4.3.3 After a given LAM has been serviced (address pushed into FIFO) that specific LAM source shall be disabled to preclude the issuance of a second LAM from the same source (the specific problem that is avoided is the phenomenon of the LAM being momentarily suspended when a module generating the LAM is addressed). After a given LAM source has been serviced it may not issue another Demand message until the LAM grader module is rearmed.

4.3.4 The generation of the Demand Initiate (DNI) signal shall be subject to the state of bit 9 of the Crate Controller status register (Enable Demands).

4.3.5 The module shall contain a 24 bit mask register to cause any or all LAM sources to be ignored (logic true to include, logic 0 to ignore).

4.3.6 The crate controller STIM line will be held true for sufficient time for generation of the demand message and does not allow the use of "Hung Demand" generation. Crate controllers interfaced to the module should have the "time-out" feature disabled by the appropriate hardware straps.

## 5.0 Mechanical Characteristics

5.1 The module will conform to mechanical specifications as indicated in reference 2.1.

5.2 The module shall be a single width CAMAC module.

5.3 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. The circuit board shall be a two sided printed circuit board with etched conductors. The fabrication of the circuit board shall be in compliance with reference 2.2.

5.4 This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. See referece specification 2.1.

5.5 All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding) and shall have an exact replacement available from a second source manufacturer.

5.6 All electrical components are to be mounted on only one side of the board.

5.7 All lettering on the front panel shall be either engraved or silkscreened. The front panel material shall be aluminum with an iridite finish with contrasting colored lettering. Figure 11.7 depicts a suggested front panel layout.

5.8 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electronic schematic associated with this module. See reference specification 2.4.

5.9 The front panel connectors shall be LEMO size "0" connectors, part number RG0B303CAZZZ (mates with LEMO #FG0B303C0040). Pin utilization shall be as follows:

Pin 1: Ground for transmitters
No connection for receivers

Pin 2: Signal high

Pin 3: Signal low

5.10 The module shall be equipped with grounded, conductive side panels.

5.11 The front panel "Bypass" switch shall be a miniature locking type toggle switch (lever must be pulled to operate).

## 6.0 Electrical Characteristics

6.1 Dataway Interface shall conform to specification as indicated in reference 2.1.

6.2 Input Power shall be derived from the standard +/- 6 volt and +/- 24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used.

6.3 The +6 and -6 supply voltages must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits have connected contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be distributed on the circuit board and be located as close as possible to noise sensitive components.

6.4 The +5 volt and ground lines for TTL logic may be carried on insulated sandwich type busses which are located under the dual in-line IC packages.

6.5 All components on this module must have a MTBF rating as specified in reference 2.5.

6.6 U-Port Adapter

| | |
|---|---|
| Input/Output: | Transformer coupled impedance matched at 100 ohms |
| Signal Level: | 5 volt +/- .5 volt differential into 100 ohms |
| Cable Range: | Trompeter Electronics TWC-124-2 or equivalent |

6.7 Clock Repeater

| | |
|---|---|
| Frequency Range: | 800KHz to 1.6MHz |
| Input/Output: | Transformer coupled impedance matched at 100 ohms |
| Signal Level: | 5 volt +/- .5 volt differential into 100 ohms |
| Cable Range: | Trompeter Electronics TWC-124-2 or equivalent |
| Active Edge: | High to low transition at LEMO Pin 2 |
| P1 and P2: | TTL compatible open collector driver 47 ohms to +5V, 100 ohms to ground |

6.8 LAM Grader CAMAC Commands

6.8.1 Read Mask [F(0).A(0).Data Returned]

This command gates the contents of the 24 bit mask register onto Dataway read lines R1 through R24. Q=1 and X=1 are returned.

6.8.2 Read Module ID [F(6).A(0).Data Returned]

This command gates the module ID number, decimal 313, hexadecimal 139, onto the Dataway read lines R1 through R24. Q=1 and X=1 are returned.

6.8.3 Load Mask [F(16).A(0).Data]

This command loads the data from the Dataway write lines W1 through W24 into the module mask register. The logical convention shall be that bits to be ignored shall have their corresponding mask bits set to zero. Q=1 and X=1 are returned.

6.8.4 Clear FIFO [F(24).A(0)]

This command clears the contents of the LAM FIFO memory. Q=1 and X=1 are returned.

6.8.5 ARM Module [F(26).A(0)]

This command arms the module and, thus, enables the module to commence the generation of Demand requests. Q=1 and X=1 are returned.

6.8.6 The module will respond to CAMAC clear command Z by clearing the LAM FIFO memory.

6.9 Operation Notes

6.9.1 If a given crate is either "powered down" or if the U-Port is placed off-line through use of the front panel switch the CAMAC serial highway will be bypassed through relay contacts within the U-Port. When this condition exists the U-Port upstream of the bypassed crate will be required to drive the length of cable going both to the bypassed crate and to the next downstream crate. This potential problem is compounded if multiple consecutive crates are in bypass and may result in data errors if the sum cable length exceeds 500 feet.

6.9.2 Upon power up of a CAMAC crate all crate controllers will initialize to the off-line state with demand messages disabled. In cases where it is desirable to enable demand messages the following sequence of commands should be observed:

1. Crate controller put on line with demands disabled.

2. U-Port mask register loaded with desired mask.

3. U-Port FIFO cleared with "Clear FIFO" command.

4. U-Port armed to allow FIFO to begin to accummulate LAM's.

5. Crate controller demand enabled.

The above sequence will safe guard against spurious LAM signals that may have occurred during crate power up and that may have been stored in U-Port FIFO.

6.9.3 It should be noted that any given LAM source may issue only one demand message between times that the U-Port is armed. After a LAM source has initiated a demand message it may not initiate a second demand message until the U-Port is rearmed. If a LAM source is in the true state when the module is armed it will immediately initiate a demand message.

6.10 Delay Line Tap Selection

When the U-Port is installed both delay line taps must be "set up" by means of the PC board switches. The following is a suggested "set up" procedure.

I. Slave Station

a. Install module and connect the four (4) serial highway cables (Bi-Phase In, Bi-Phase Out, Clk In, Clk Out), set switch SW1B to "Slave" position. Do not connect D-Port pigtail at this time.

b. Using rotary switch SW2 (tap selector) and/or alternate action switch SW1A (clock/not clock) cause the waveforms on TP1 and TP2 to be aligned as depicted in Figure 11.6.

c. Connect D-Port pigtail along with "turn around" connector and verify that the crate "No Sync" LED is not illuminated.

d. Through the serial highway force L-2 controller "on-line".

e. Observe and note the phase relationship between the incoming clock and data as observed on test points TP3 and TP4.

f. Using rotary switch SW3 (tap selector) and/or alternate action switch SW1C (clock/not clock) cause the phase relationship between outgoing clock and data (TP5 and TP6) be the same (+/- 10ns) that of step "e" above.

II. Master Station

The first U-Port on a serial highway link will be connected to the system Serial Driver as opposed to being connected to an L-2 Controller. For such stations the link output clock must be derived from the Driver Clock as opposed to being received from the incoming clock.

a. Set switch SW1B to "Master" position.

b. Using rotary switch SW3 and/or alternate action switch SW1C cause the waveforms on TP5 and TP6 to be aligned as depicted by Figure 11.6.

c. The Link receiver circuit and the delay line switches associated with it may not be set up until the entire link is configured. After all "slave" U-Ports on the link are set up then the master station receiver may be set up by the following steps.

Ia and Ib in the same way as a slave station is set up. The pigtail connector, however, must be connected to the Serial Driver during Ia and Ib.

## 7.0 Environmental Data

7.1 The module must operate, as defined, over an ambient temperature range of 0 to +50oC.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 20 gauss per millisecond with a peak magnitude of 100 gauss in any direction.

7.4 The module must operate, as defined, in a radiation environment as follows:

| | |
|---|---|
| Neutrons: | 2 x 10 7 N/CM2/sec |
| Rad-Dose: | 5 x 10 -2 rad (Si)/sec |
| Integrated Dose: | 200 rad (Si) |

## 8.0 Safety

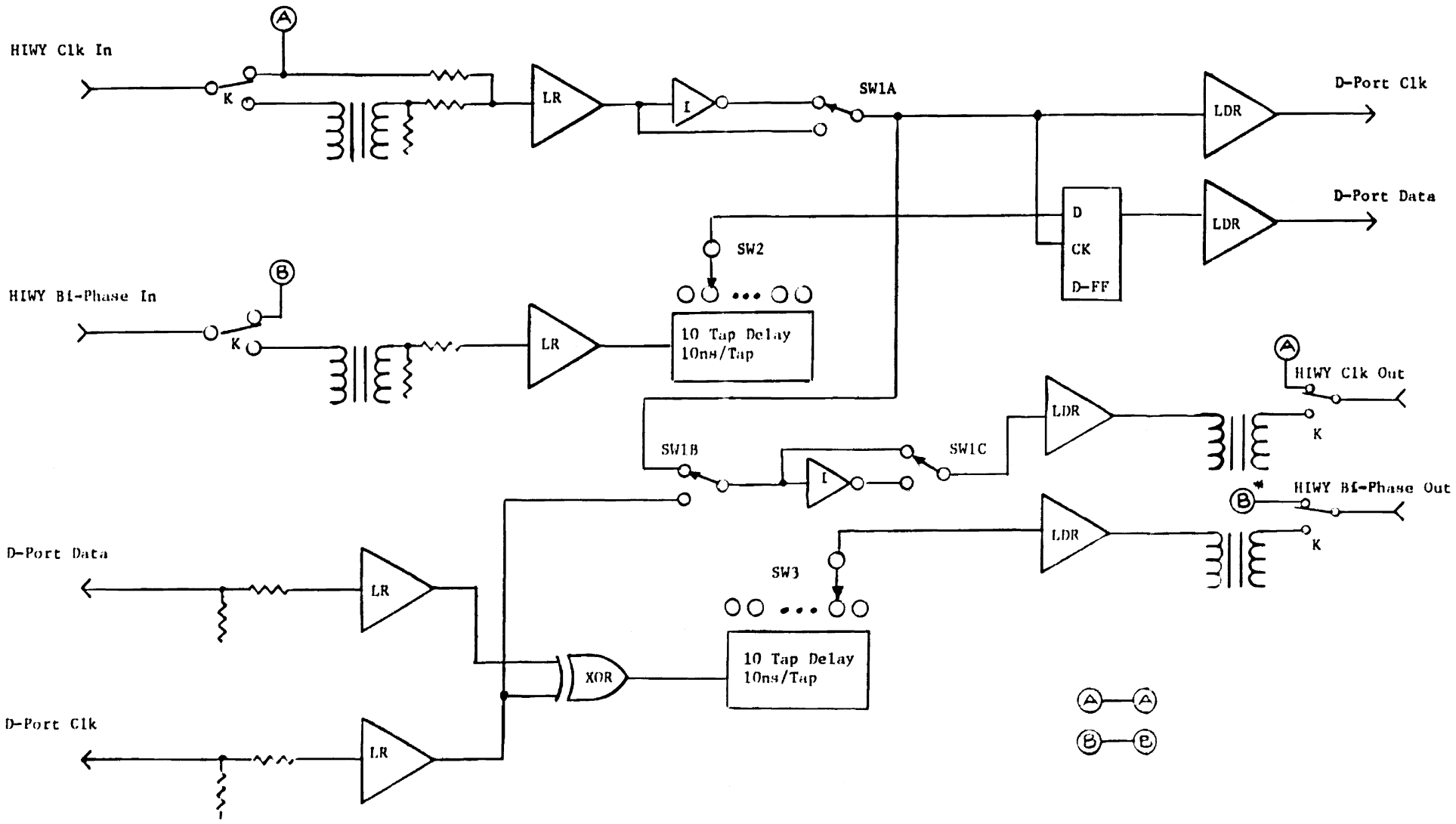
All components of this module must be of flame retardant materal.

## 9.0 Testing

All modules shall be subjected to a temperature cycling period followed by a functional test prior to shipment equivalent to tests delineated in reference 2.6. The functional test must test all components of the system including bypass relays and all delay line taps. The test shall be done at 5MHz link speed with link cables at maximum allowed cable lengths.

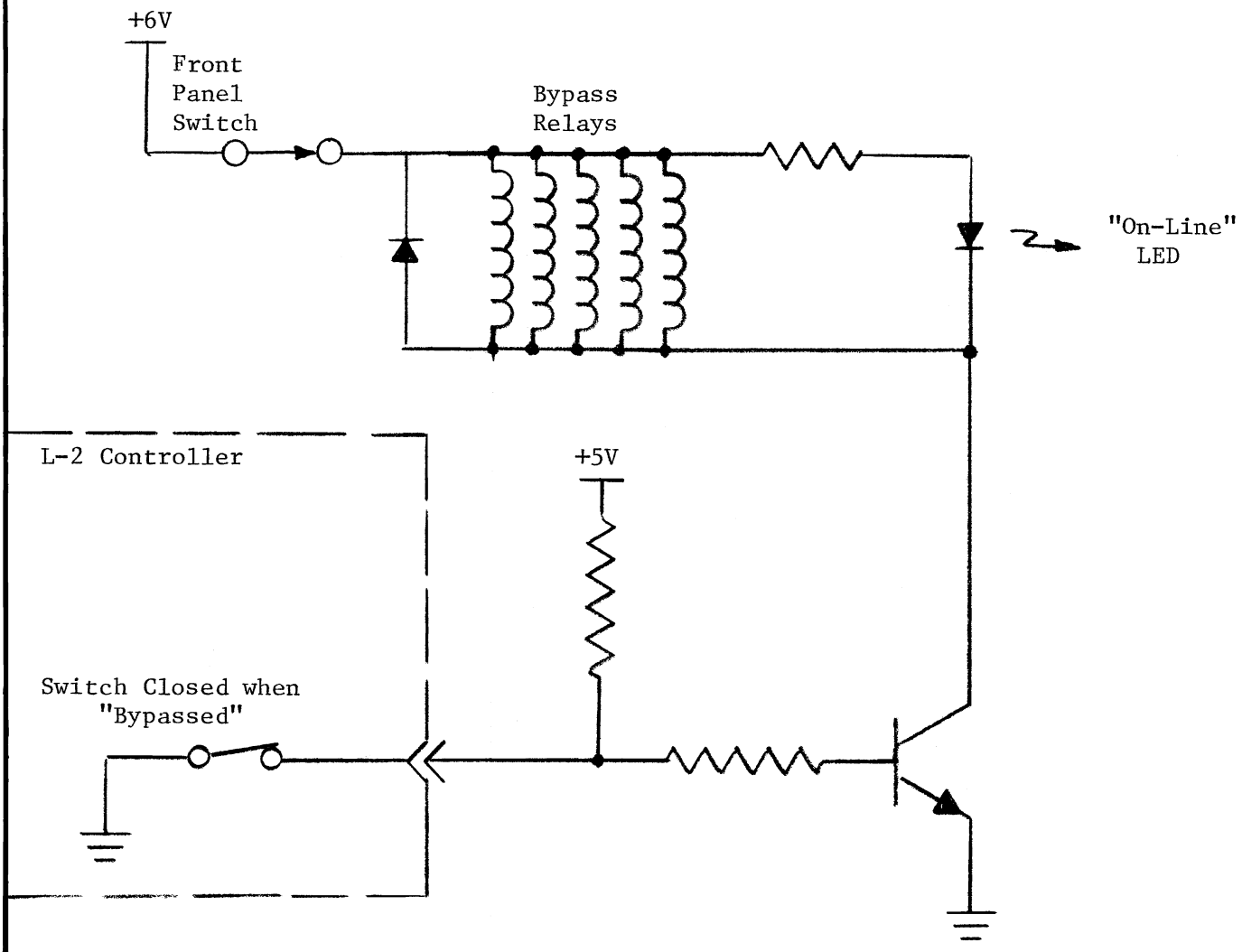
## 10.0 Reliability and Quality Control

The module shall meet all applicable requirements specified in reference 2.5.




U-Port Block Diagram

Figure 11.1




Bypass Control

Figure 11.2

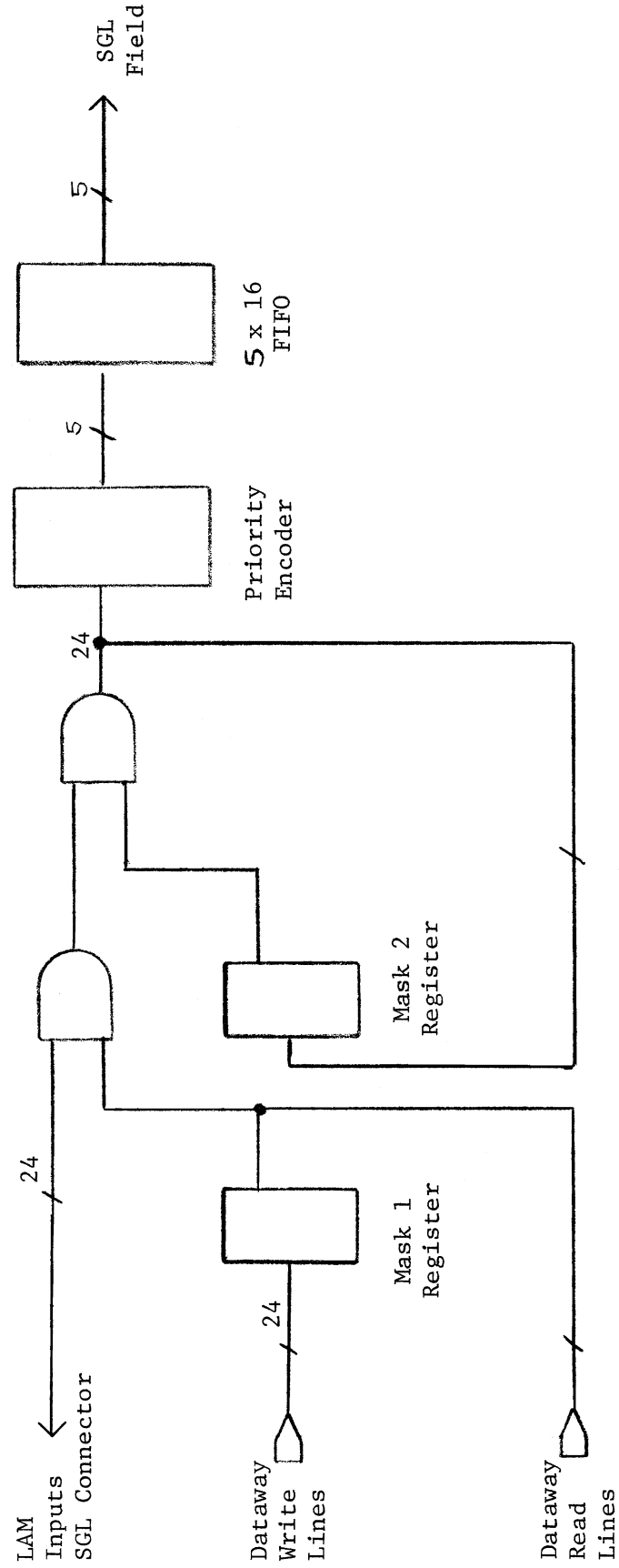



Figure 11.3

LAM Grader Circuit

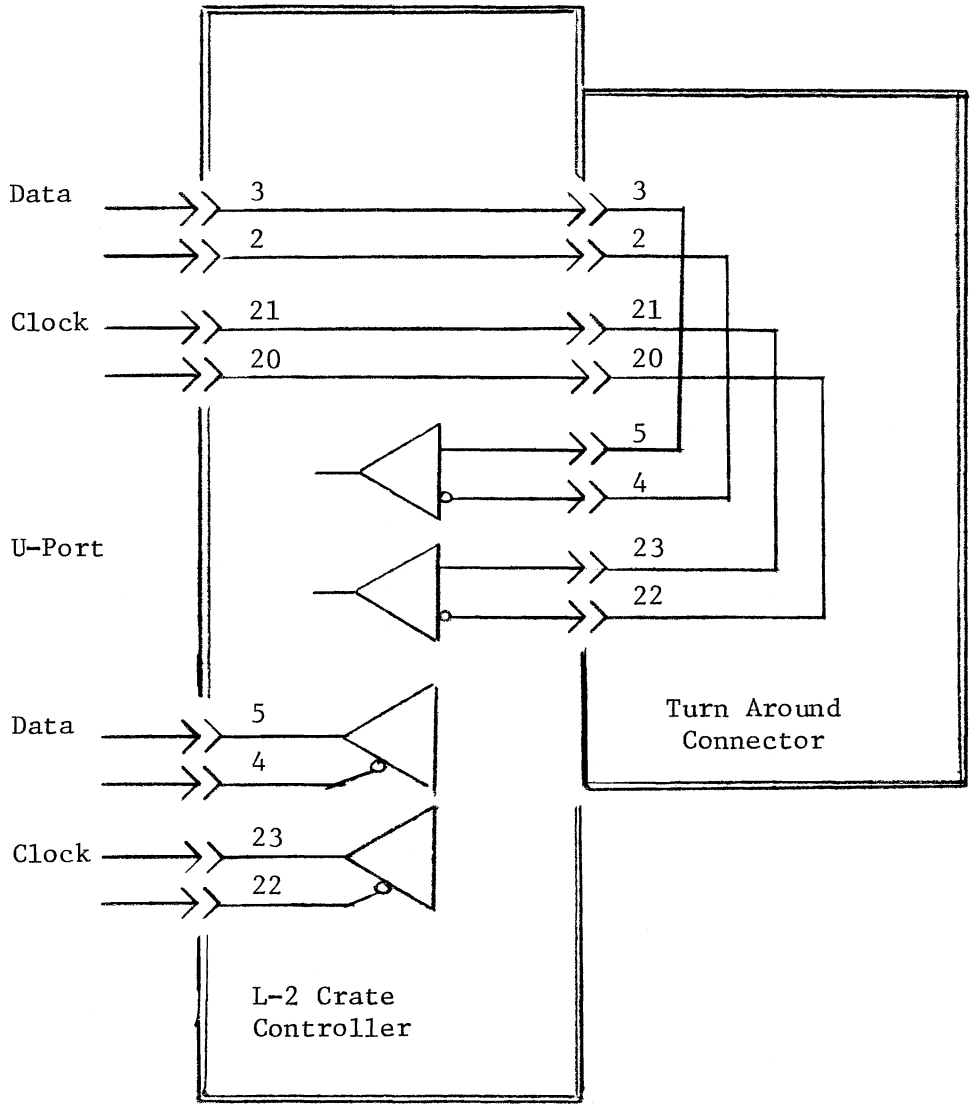
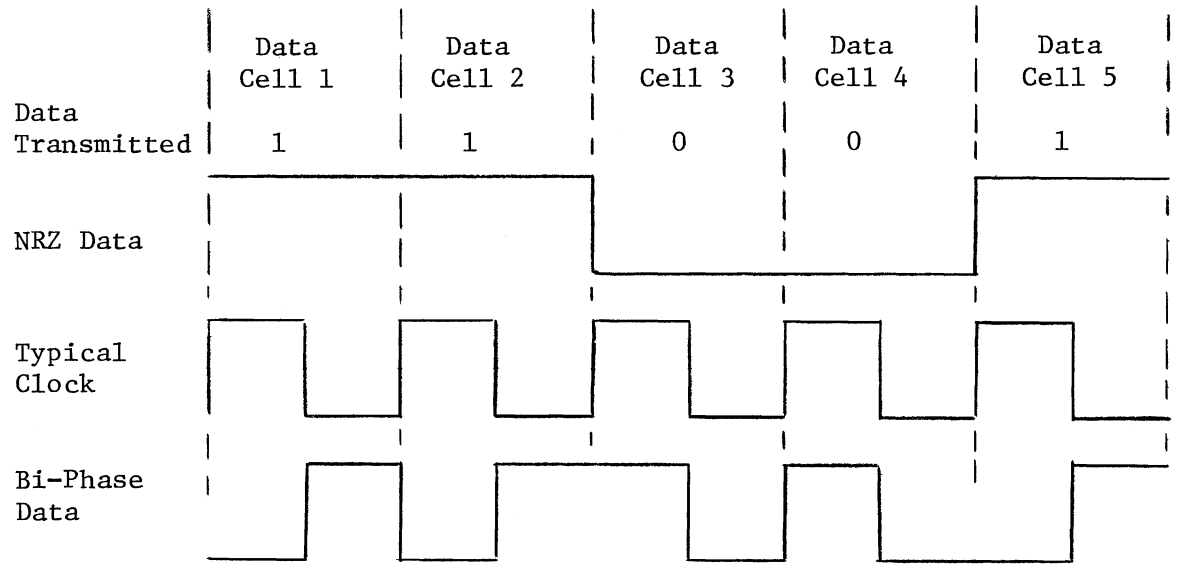


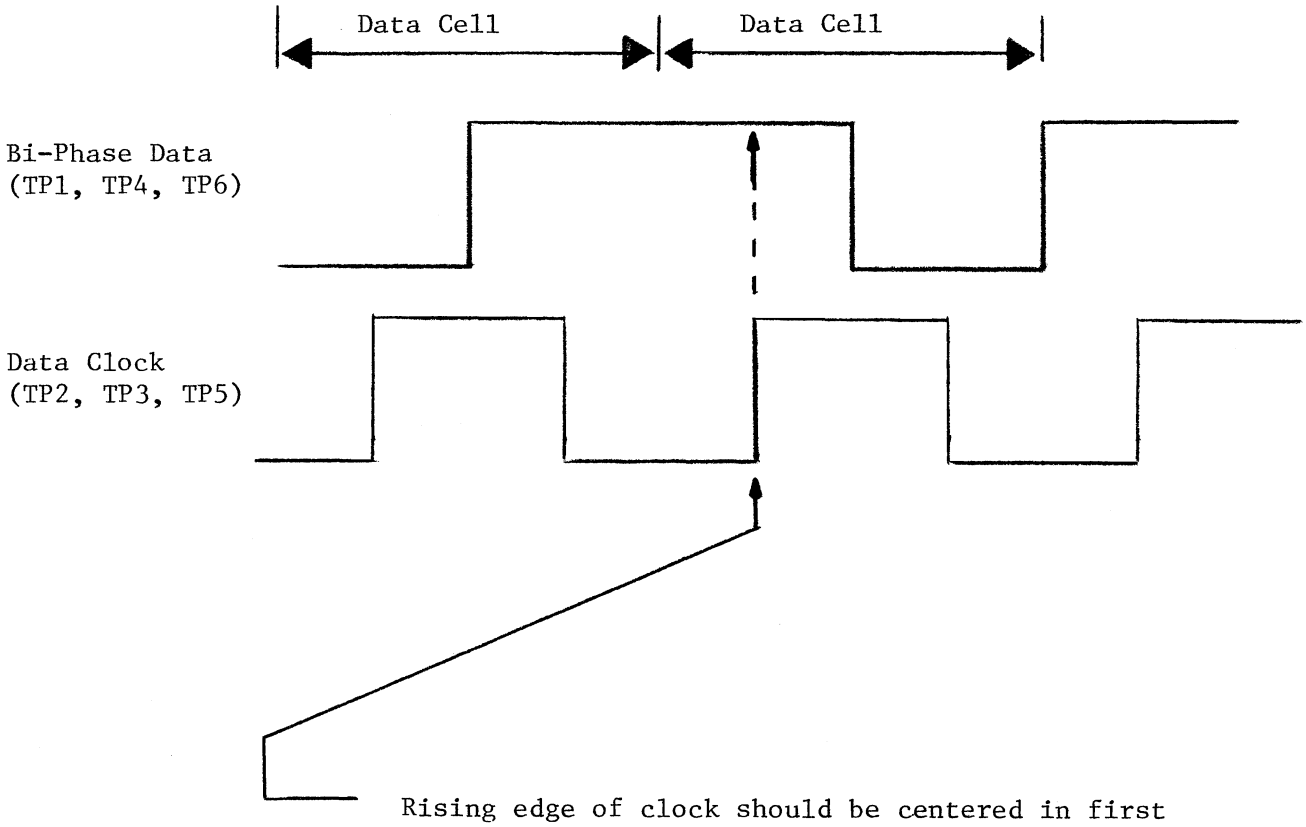

Figure 11.4

U-Port Interconnect




Example of Bi-Phase Encoding

Figure 11.5




Rising edge of clock should be centered in first half of data cell. The 10 Tap (10ns/Tap) delay line selection switch should be positioned to setting close as possible to center.

Clock/Data Phasing

Figure 11.6

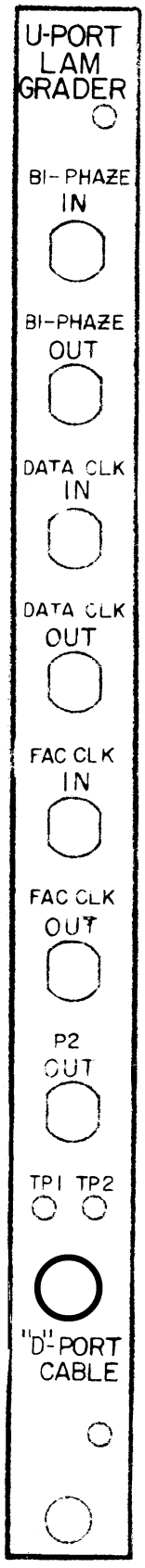



FIGURE 11.7

FRONT PANEL LAYOUT

# 313 U-Port Module Modifications

1/9/07

John Wertenbaker

## P2 Modification

It was found that the "low" level of the P2 line on the dataway was over 1V. This caused some modules to occasionally miss P2 clocks. To fix this, R6 was changed from 47Ω to 100Ω, and R5 was removed. Nearly all of the 313 U-Port modules have received this modification.

## R2 Modification

The 390Ω resistor that drives the base of Q1 delivers far too little current for Q1 to properly drive the relays. This has, in part, accounted for many Q1 failures. The modification replaces this resistor (R2) with 100Ω. Nearly all of the 313 U-Port modules have received this modification.

## Q1 Modification

Q1 is a 2N2222. Even with the R2 modification, failure of Q1 has accounted for many U-Port failures. The 2N5320 has better current transfer characteristics and better collector current ratings, and is therefore better suited for this application. However, with our current abundance of spare U-Port modules, no modules have received the Q1 modification.

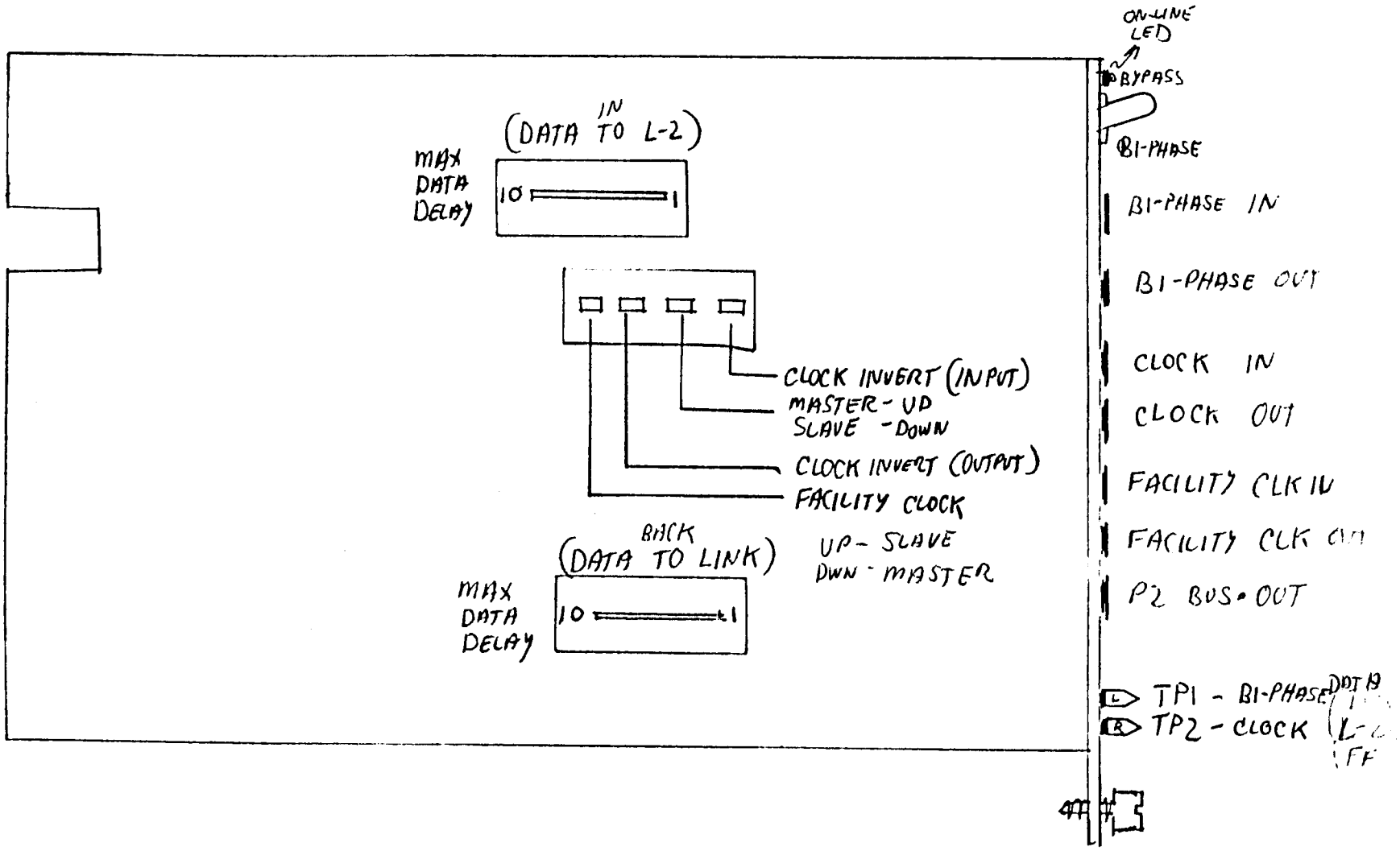
## P2 Glitch Modification

It was found that the P2 output on the 313 U-Port module does not completely strip out Facility Clock codes. The internal circuitry employed to execute this function consists of a one-shot driven by an edge detector. The P2 output comes from the one-shot. (U37) The edge detector is an excusive OR gate (U65) with one input tied to the Facility Clock Link, and the other input tied to a delayed version of the Facility Clock Link. The delay is achieved by 6 inverters in series. (U52) See the schematic below.

The one-shot is set to output a pulse of approximately 700nS. Due to the nature of the Bi-phase encoding, this one-shot receives a trigger pulse at intervals of either 500nSec or 1uSec. The one-shot is not retriggerable, and should output its 700nSec, regardless of whether it gets 1 or 2 trigger pulses. But sometimes it re-triggers anyway, causing extra pulses on the P2 output. The resistor value used (2.2K) is very close to the minimum value accepted by a 74LS221. (2K) This situation is stretching the 74LS221 beyond its design limitations.

The modification replaces the 2.2K resistor (R24) with a 27.4K 1% resistor, and it changes C12 from 500pf to 33pf 5%. The modification also removes R28 and C11. A blue dot shall be affixed to the front panel to indicate that it has been modified.

Since the problem is transparent to most systems, very few 313 U-Port modules have been modified.




H313 U-PORT SKETCH

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPROVED |
| | -001 | ORIGINAL ISSUE | 7-83 | |

+6V 42R
Y2 42
(+6V)
Q2 MJE3055
C25 33
C24 .47
(+5V)
C1-C10,C13,C14, C16-C23,C26 .01UF
+5V
JX1 DATA CLOCK IN (LOCATED ON FRONT PANEL)
JX2 DATA CLOCK OUT (LOCATED ON FRONT PANEL)
JX5 BI PHASE IN (LOCATED ON FRONT PANEL)
(SHLD)
C30 .01
C29 .01
(BLK)
(RED)
CAW-5
K3
K4
K1
*BYPASS
R22 1K
R20 1K
R21 150
R14 1K
R18 15
R19 15
R13 1K
R15 1K
R23 1K
R7 1K
R10 1K
R11 150
R12 1K
R9 1K
R8 1K
R17 1K
U23 PE8304
U8 PE8304
U16 AM26LS32
TP3
(LINK CLK)
U30 LS04
U4 DS8830
TP5
TP4
SW1
SW2 79C10
U15 DL6707
100NS
10NS/ TAP
(LOCATED ON FRONT PANEL)
SW4
CR1 1N4005
(RELAY COILS)
K1 K2 K3 K4 K5 K6
R3 390
L1 ONLINE
Q1 2N2222A
R2 100
R52 1K
R1 10
J1
24-BYPASS
TP1 (DATA)
U62 LS07
U59 LS74
U54 DS8830
(TWISTED PAIRS,W/SHLD. GND)
J1 DATA OUT (TO "D"-PORT CONNECTOR)
J1 CLOCK OUT (TO "D"-PORT CONNECTOR)
U30 LS04
R51 1K
TP2 (CLK)
0V 43
0V 43R
J1 DATA IN (TO "D"-PORT CONNECTOR)
J1 CLOCK IN (TO "D"-PORT CONNECTOR)
R41 1K
R45 1K
R46 150
R40 1K
R44 1K
R43 1K
R49 1K
R47 150
R42 1K
R48 1K
U64 AM26LS32
U59 LS74
U5 LS14
U65 S86
C28 300PF
U6-2
U61 DL6707
100NS
10NS/ TAP
SW3 79C10
DS8830
U53
R36 15
R37 15
U8 PE8304
CAW-5
K2
(SHLD)
(RED)
(BLK)
JX7 HIGHWAY OUT (LOCATED ON FRONT PANEL)
JX3 FACILITY CLK IN (LOCATED ON FRONT PANEL)
JX4 FACILITY CLK OUT (LOCATED ON FRONT PANEL)
C31 .01
K5
K6
R26 10K
R25 1K
R33 1K
R34 150
R27 1K
R35 1K
R32 15
R31 15
U30 AM26LS32
U46 PE8304
LS14
U52
U45 DS 8830
SW2 79C10
U65 S86
U37 74 LS221
C12 33pf 5%
R24 27.4K 1%
R30 10K
C15 100PF
U11 LS06
R29 100
R6 100
R45 100
R4 100
R38 15
R39 15
C11 33
R28 75
U46 PE8304
JX6 P2 OUT (LOCATED ON FRONT PANEL)
1 P1
2 P2
U60 LS123
C27 .01UF
U3 LS00
U1 K1114A
R50 10K

BiRa SYSTEMS INC.

TITLE: SCHEMATIC DIAGRAM U-PORT LAM GRADER MODULE NO. 313

SIZE: D

DRAWING NUMBER: 313-D-001

DRN BY L&M | SCALE NONE | SHEET 3 OF 3