Constant Fraction Discriminators

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Constant Fraction Discriminators
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1. We have several different kinds of Constant Fraction Discriminators in the lab: four Tennelec TC453 Single CFD's, an Ortec 453 and 473 Single CFD, two Ortec 934 Quad CFD's, two Ortec 935 Quad CFD's, lots of homemade CF4000 Quad CFD's, and one EG&G ESN CF8000 Octal CFD. The CF8000 uses much of the same circuitry as the CF4000, but with many settings fixed internally. The 935's are just faster versions of the 934's. The pulse pair resolution of these different units is very different, as indicated in the table at the end of this report.

2. CFD's are designed to produce accurate timing information from analog signals of varying heights but the same rise time. They do this specifically in the CF4000 by splitting the input signal, attenuating half of it and delaying the other half, then feeding the two halves into a fast comparato with the delayed input inverted. The effect is to trigger a timing signal at a constant fraction of th input amplitude, usually chosen to be around 20%. Since the input is DC coupled, small variation in the fraction can be compensated for by varying the DC level of the attenuated half of the signal. (Z/C, or Walk adjust). The output of the fast comparator (AD9687) is brought out to the front pan as the Z/C monitor, and can be observed while adjusting the Z/C Adjust. During the time when th input is at ground, both halves of the signal will be equal to zero and so the output of the 9687 will be at some DC level, but with lots of noise. The Z/C Adjust should be set so that this noisy DC level is midway between the high (-0.8V, ECL high) and low (-1.6V, ECL low) levels, while triggering on the output. To set this for optimum walk reduction, an actual detector signal has to b connected to the input. The possible improvements, however, are at most a hundred or so psec, so will be hard to see for most of our applications. More information on setting the walk adjust on th and other CFD units can be found in point 9 below or in the CFD manuals.

3. Historically, the drive to develop a constant fraction discrimination technique arose from the observation that leading edge timing with scintillation detectors and PMT's had an optimum value a particular fraction of amplitude, usually 10-15%. The constant fraction technique used this fact ; well as accomplished the virtual elimination of walk for signals of the same risetime but varying amplitudes. The particular fraction desired in a CFD determines the amount of attenuation of the attenuated input signal. Then, if the delay is chosen correctly, the CF will fire at the place where t maximum of the attenuated signal crosses the delayed signal. That point will be at a constant fraction of the delayed signal amplitude. The relationship between delay and rise time in such a case is as follows: $t_d = t_r(1 - f)$, where f is both the fraction desired (usually .2) and the attenuation factor of the input signal. If the delay is set to a value less than the shortest anticipated risetime, walk can be eliminated even when signals have varying risetimes. In what follows, f

$$t_d = t_r(1 - .2) \Rightarrow t_d = 0.8 t_r \quad t_d = 6 \text{ ns}$$

$$t_r = 8 \qquad 10/31/2005$$

will only represent the attenuation of the input signal. If the input signal is simulated by a linear ramp, its equation is $P_i = -mt$. The attenuated signal is then $P_a = -fmt$, and the delayed sigr is $P_d = -m(t - t_d)$. We want to set $P_a = P_d$ and solve for t , which results in

$$t_c = \frac{t_d}{(1 - f)} .$$

Note that this is independent of the slope m (and thus risetime). The amplitude fraction F in this general case can be found by calculating the ratio of P_d evaluated at the crossing time to the maximum value of P_d :

$$F = \frac{-m(t_c - t_d)}{-mt_r} = \frac{ft_d}{t_r(1 - f)} .$$

4. A detailed description of the circuit of the CF4000 follows. Refer to the schematic for component references. Note that most of the signals are at ECL logic levels (see point 2 above.) The input signal is actually split three ways. One part goes to the inverting input of half of the 9687 comparator. The noninverting input of that half is connected to a DC level set by the Threshold pot. Thus, if the input signal is below the threshold (both are negative voltages), Q goes high (-0.8V), while $\overline{Q}$ goes low (-1.6V) and stays low until the input signal rises back above the threshold. Another part of the input signal is attenuated by R4 and R7, then fed to the noninvertir input of the other half of the 9687. The final part of the input is delayed through Delay Out and Delay In FP connectors and fed to the inverting input of the 9687. When the input is at ground, th Q output of this half of the comparator is at some noisy DC level (see point 2 above). At the leading edge of the input signal, Q goes low, then goes back high when the attenuated input amplitude equals the delayed input amplitude. It stays high until the delayed signal returns to the baseline, at which time Q returns to the DC noise level. This Q output is brought to the front pane as the Z/C monitor. The output, of course, is just the complement of Q . Note that all outputs of tl 9687 are open emitter and so must be tied to -5 V through a resistor. The $\overline{Q}$ outputs of both halve of the 9687 take advantage of this open emitter configuration and are tied together to form a negative input NAND gate. If either of the $\overline{Q}$ outputs is at a high level, that output transistor will conduct enough current to bring its emitter to within a diode drop of its base. The transistor on the other output may shut down if it is trying to go low, but the first transistor alone will still maintain high output level. Only when both of the transistors are low will the total current through the resistor be such as to let the output go low. As a result, the signal going into pin 6 of half of the 10130 latch is low during the low overlap of the two $\overline{Q}$ signals, namely the time above threshold and the time from the constant fraction trigger to the end of the delayed pulse. The 10130 dual lat Q output goes low when its enable input goes low if the D input is low (the D input isn't shown on the schematic, but an unconnected input in MECL is low due to an internal pull-down resistor), an its $\overline{Q}$ goes high, and it will stay in that state indefinitely after the enable input returns high unless set or reset. An elaborate set of transistors (Q1-Q4) handles setting the width of these output signა (returning the output to the high state). By adjusting the width pot, R39, the bias current of Q4 caı

be set between 0.2 and 8.8 mA. If Q1 and Q3 are turned off, the 51pf CA will charge up at a rate determined by this current, and Q2 acts as a follower to deliver the rising signal to pin 5 of the 10130, the S input of the latch. If Q1 or Q3 are turned on, the capacitor is discharged and the S input is not high enough to set the latch. Q1 is turned on during the time the enable input of the 10130 is low, so charging doesn't begin until that input goes back high (remember this is the coincidence of the threshold and constant fraction discriminators). $\overline{Q}$ is high, so Q3 is turned off until S crosses the threshold to high. Then $\overline{Q}$ goes low, and Q3 is turned on and stays on until th₁ next signal. Note that, since CA charging doesn't begin until the enable input goes high, even wh₁ the width pot is set to a minimum (maximum charging current), the output width cannot be narrower than the enable input signal width. This is a factor when the input signal to the CFD is very wide. Note, too, that, since the 10130 is a latch and the output doesn't change no matter how many times the enable input goes low, a second pulse will only trigger the latch if the width settin₁ is such that the S input allows the latch to reset before the next pulse arrives. This is how the deadtime setting (blocking) works. Q from the 10130 turns on Q5 when low, which triggers a 96LS02 one shot to light the LED to indicate a trigger. Due to stray capacitance, it takes a finite amount of time to pull down the input (pin 11 or 5) of the 96LS02, and if the width of Q is less tha approximately 100 nsec, the 96LS02 will fail to trigger and the LED will not light. Q also drives the other half of the 10130 dual latch and charges C5 through R29 at the same time it drives the enable input pin 11 low. Since D starts out high, $\overline{Q}$ goes low at the leading edge of the enable input. As soon as input D charges up and crosses the threshold to low, which takes roughly 15 ns₁ $\overline{Q}$ goes back high. This provides the two fixed width fast outputs. The Q from the first half of th₁ latch provides the wide output. All three outputs are sent through transistors (Q6-Q8) to shift the levels from ECL to NIM. Note that the NIM levels depend on the level difference between ECL low and high, which for this board is something less than 800 mV, more like 700. The output signals thus start out low from this CFD, which could be a problem if further attenuated by long lines.

5. Note that the width of a pulse above threshold changes with threshold level, and since this width i₁ coincidence with the constant fraction width sets the minimum blocking pulse width, pulse pair resolution and output pulse width can be changed by the threshold setting. Also, with pulses close together, there can be some pileup on pulse tails, which changes pulse amplitude and therefore width above threshold, leading to strange behavior.

6. RG174 delay cable provides approximately 1.8 nsec/ft of delay. Some CFD units have an internal delay that must also be taken into account when calculating delay totals.

7. Some CFD units have an Update/Blocking switch (also called Update/Norm). The switch is internal on the 934 and 935 units, and doesn't exist on the CF4000 and CF8000. In Norm-Blockin mode, pulses coming in within the blocking period are ignored. This is the way the CF4000 alwa₁ works. In update mode, the widths of subsequent pulses are added, extending the deadtime by tha amount. Typically, we want update mode for best pulse pair resolution, and blocking mode to prevent ringing. On the 934-935 units, all three outputs are identical and their widths change with the width setting.

8. One consideration for setting the constant fraction level is noise on a signal. If there is a lot of noi at low levels, 20% could conceivably be too low and 40% might be needed.

9. There are two basic kinds of walk or Z/C monitors. The 934-935 has a well-shaped monitor signa which is the input to the crossover detector: the actual bipolar signal composed of the attenuated half of the input signal plus the delayed and inverted other half. While triggering on the output, se

the walk adjust so that all signals cross zero at the same time. For the CF4000 and TC453, the Z/C monitor is the output of the fast comparator, and the Z/C adjust should be set so that the DC noise level on either side of the central waveform is midway between the high and low level. Note: this signal is greatly attenuated, and so won't represent the actual ECL voltages. The high and low levels can be easily observed just by adjusting the Z/C pot.

10. The following is from a conversation with Dale Gedcke of Ortec (800-251-9750, X224) on May 2 2000. The idea of an optimal fraction as depicted in the Ortec catalog on pg. 2.137 is only for scintillation detectors. The theory for this is developed in the paper by Hyman & Schwartz, Rev. Sci. Instr. 35 (1964) pg. 393. For work with channel plates or SBD's, we care only about minimizing amplitude walk. Time resolution is relatively insensitive to the actual fraction set on t constant fraction. The reason that we want to set the delay so that the maximum of the attenuated pulse crosses at the desired fraction of the delayed pulse is just so that the CFD can trigger at the advertised fraction. A potential problem with the 0.2 fraction, as well as with using the CFD with short delay for ARC mode is that the initial negative lobe of the bipolar pulse is very small. It's tough to tell whether you're actually triggering on the zero crossing or on the leading edge. The walk can be adjusted on a 935 first with a fast scope by looking at the monitor while triggering on the output. All of the bipolar pulses will "neck down" at the trigger point, and we should set the walk adjust to make that point as close to zero as possible. To do it right, we should look at an MCA and watch the wings of the peak as the walk is adjusted. For fast channel plates, we might want to consider the Ortec 9307.

Table 1: Pulse Pair Resolutions

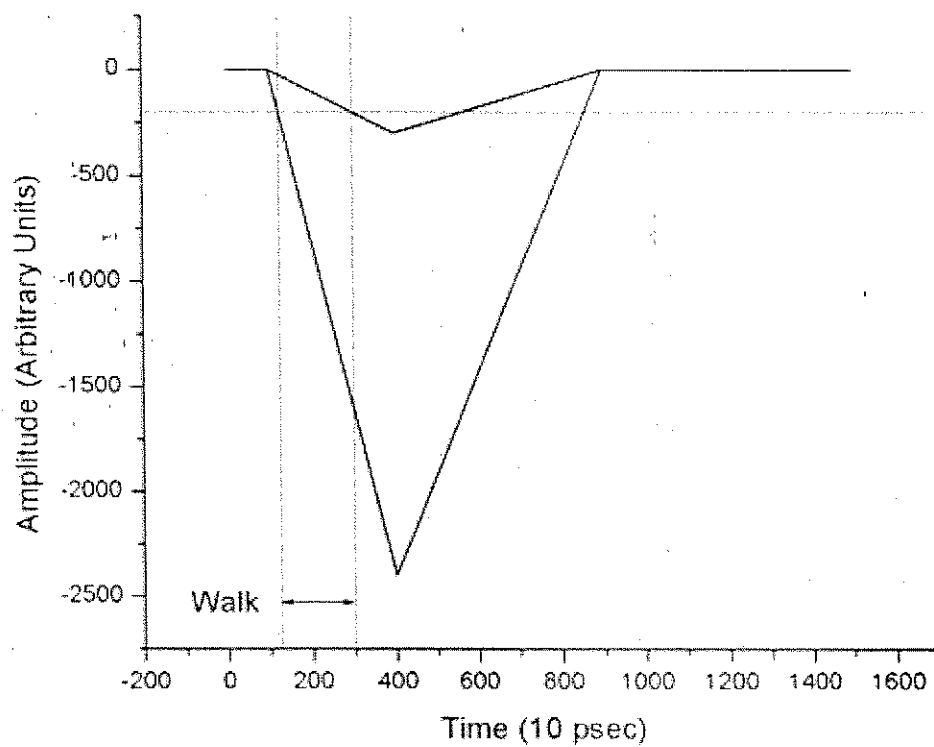| Model Number	Pulse Pair Resolution (in nsec)
Tennelec TC453 single	10
Ortec 934 quad	7-10
Ortec 935 quad	5
CF4000 quad	15-20
CF8000 octal	30

Figures

Figure 1: This illustrates the time "walk" seen for different signal amplitudes when using a leading edge discriminator with a fixed trigger point.
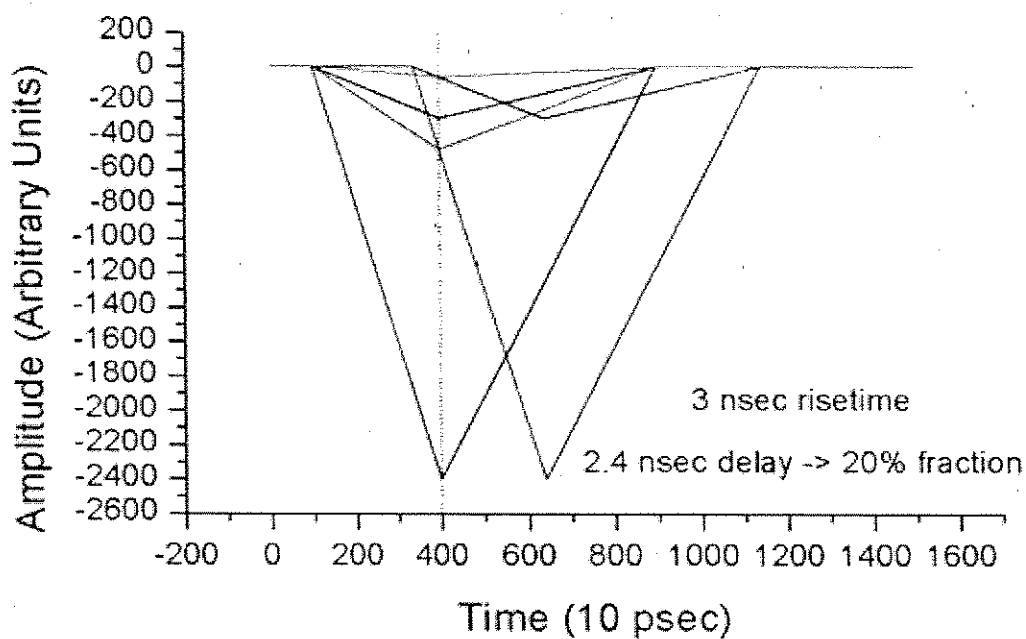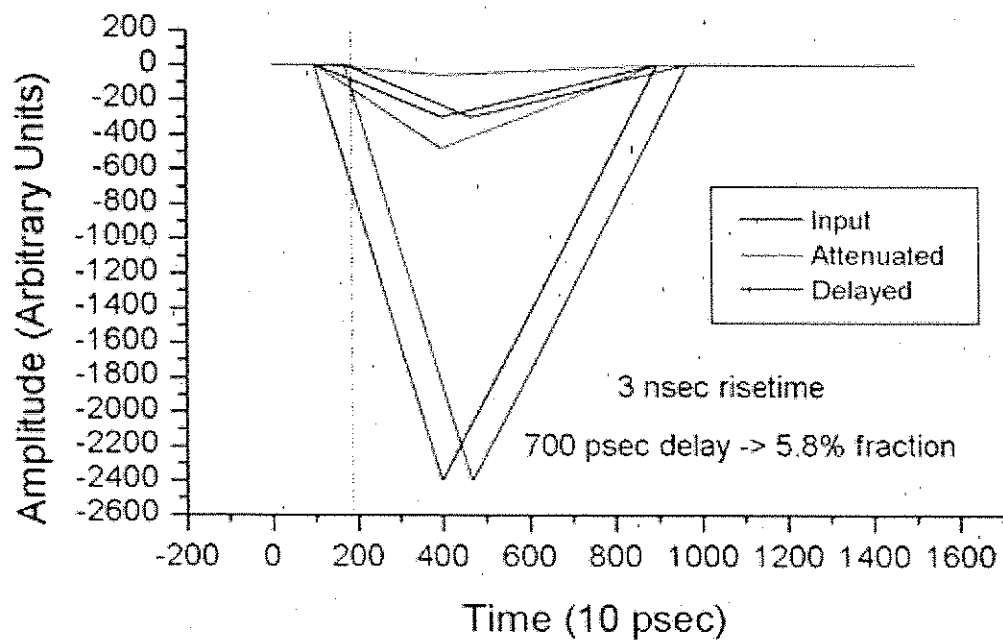
7.56 × 0.4

Figure 2: Two different values for the fraction in a constant fraction discriminator showing how the fraction depends on the delay (delay cable plus internal delay) and how time walk is virtually eliminated for signals of different amplitudes.

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