INSTRUCTION MANUAL
MODEL 73A
SCSI BUS
CAMAC CRATE CONTROLLER

Edition 6.1

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SERIAL NUMBER_____

NOTE To Users who intend to use Fermilab Software:

Fermilab purchases Model 73A controllers that incorporate special microcode for use with their software. This microcode can be identified by the designation M73AxR2.8 on the prom labels, (x is either the letter H or L). Standard 73A controllers use microcode labeled either: M73AxR2.7, M73AxR2.a or 3047-010 and 3048-010.

Jorway will exchange microcode proms with any user who encounters difficulty using Fermilab software.

1.0 Introduction

This manual describes the installation, operation, and programming of the Jorway Model 73A series SCSI Bus CAMAC Crate Controllers. It is assumed that the user is familiar with the CAMAC system, as described in IEEE Standards 583 and 675. Knowledge of the SCSI-2 specification, ANSI Standard X3.131, while not required, will be helpful, especially in writing software using the SCSI message system, and interpreting the controller's replies to various SCSI commands.

2.0 General Description

The Jorway Model 73A Crate Controller is a double-width CAMAC module that interfaces a CAMAC Crate to any computer supporting the ANSI standard Small Computer System Interface (SCSI) Bus. Several CAMAC Crates with Model 73A Controllers can be intermixed with other SCSI devices on a single SCSI port, which can support up to 7 devices. The single-ended SCSI bus is employed, allowing a maximum bus length of six meters. The Controller has two SCSI-2 high density shielded connectors, permitting devices to be daisy-chained.

The Model 73A obeys all mandatory requirements in the SCSI-2 specification. All types of CAMAC operations are permitted, including high-speed Block Transfers under hardware control. Any of three ESONE standard modes can be selected, Address Scan, Q-Stop, or Q-Repeat. During block transfers, only data is transferred on the SCSI Bus. For any transfer, the user can elect to transfer either two or three data bytes for each CAMAC cycle. In the latter case, an additional null byte is inserted in the data stream so that 24 bit data is aligned on 32 bit memory boundaries. The order of byte transmission is user selectable as high order first or low order first. The Model 73A can operate in synchronous as well as asynchronous SCSI mode, and can transfer data at full dataway speed.

Modules asserting LAM's can interrupt the computer using the SCSI Asynchronous Event Notification (AEN) protocol. In the course of this protocol, the complete pattern of asserted LAM's from a single crate is transferred to the host, which can determine the crate ID during the selection process. Note that the host adapter must be capable of operating in Target mode to use this protocol. In other respects, the Model 73A provides the same functionality as the Type A CAMAC controller, including the Station Number Register, and uses the same codes for commands addressed to the controller itself. Therefore, the Read-L command can be used to poll for LAMs. In addition, the Model 73A incorporates a LAM mask register.

The Model 73A functions only as a master controller, but does support the Auxiliary Control Bus in accordance with IEEE Std 675. Therefore, the Model 73A must reside in the rightmost station of a Crate, but other auxiliary controllers may also be present, and can use either the Request/Grant or Auxiliary Controller Lockout (ACL) mode protocol. An additional feature is a 24 bit mailbox register with flags. This may be used for system testing, or to facilitate interprocessor communication via an auxiliary controller.

An optional version, the Model 73A-1, can function as either a master or auxiliary crate controller. Changing from one role to the other is accomplished with switches. An additional option, the Model 73A-2, supports the FASTCAMAC protocol, Level 1. This feature increases the transfer rate to 7.5 mbytes/sec. for CAMAC reads. Options 1 and 2 may be combined.

3.0 Installation

The following sections contains information pertinent to the Models 73A, 73A-1 and 73A-2, except where differences are specifically noted.

3.1 Byte Transmission Order

The order of byte significance is determined by a 2-position strap accessible by removing the top cover. For arithmetic calculations, some computers place the most significant byte of a longword at the highest memory address. For these systems, the least significant byte of each CAMAC word must be transmitted first, sometimes

referred to as the "little endian" byte order. Other systems are "big endian". If the strap spans X1 and X2, the "big endian" byte order results. Otherwise the strap should span X2 and X3. Computers from DEC, and 80x86 based PC's are little-endian. Machines using 680x0 processors, such as Macintosh, are big endian, as are HP, Sun, and IBM RS/6000 workstations. VME processors are also generally big endian. Note that the byte order within SCSI commands is not changed by this strap, nor is the order in replies to INQUIRY or REQUEST SENSE commands.

3.2 Host ID

If (and only if) the asynchronous event notification (AEN) procedure is to be used for LAM notification, the SCSI ID of the host must be determined and straps inside the controller set accordingly. The possible host ID's are 0, 1, 6 or 7. It is set at 6 prior to delivery to the customer. Figure 1 shows the strap locations for the different choices. If a host ID different from the above choices is required, the factory should be contacted. As noted earlier, the AEN procedure requires a host adapter and software capable of operating on target mode, which, unfortunately, is rare.

3.3 Internal Switches, Model 73A

The Model 73A has a 4-position piano switch accessible at the top edge of the module. Switch 1 determines whether the Model 73A maintains continuous control of the CAMAC Dataway during a block transfer. If this switch is ON, the Model 73A releases the Dataway after each CAMAC cycle, and must re-arbitrate with other controllers before starting another cycle. If switch 1 is OFF, the Model 73A does not arbitrate after the first cycle, and therefore runs somewhat faster. However, other controllers are prevented from doing cycles until the block is completed. The switch should be OFF if there are no other controllers in the crate.

Switch 2 activates FASTCAMAC reads using function code F(5) (Model 73A-2 only).

If switch 3 is OFF, the controller will operate in ACL (Auxiliary Controller Lockout) mode. When instructed to perform a Dataway cycle, it will assert the ACL signal on the Auxiliary Control Bus, and proceed to perform a Dataway cycle as soon as it detects that the Dataway is not busy. The ACL signal assures that the bus will be available within 600 nanoseconds, by forcing active controllers to abort their cycles if they are in early stages. There can only be one controller in a crate operating in ACL mode, but it need not be the master controller (i.e. occupy the rightmost position). CAMAC Serial Crate Controllers normally operate in ACL mode.

Request/Grant is the preferred method of operating multiple controllers in a crate. If switch 3 is ON, the Request LEMO connector must be patched to the Grant-In LEMO of the highest priority Controller. This Controller's Grant-Out must be connected to the Grant-In of the next highest priority Controller, and so on. The Request LEMO of all controllers carry the same signal. Only one is used. If there is an ACL mode controller in the crate, it does not participate in the grant chain, as it will preempt all other controllers as noted above. If there is only one controller in a crate (occupying the rightmost position), it can operate in either mode. If it is in the R/G mode, Grant-In must be patched to Request.

Switch 4 enables a 24-bit LAM mask register, that can be overwritten by the CAMAC command F(16)N(30)A(0). If the mask register is enabled, only LAMs from stations corresponding to a set mask bit will be returned by a read-L command or generate an interrupt. If switch 4 is off, all LAMs will be recognized.

3.4 Bus Termination

Multiple SCSI controllers (73A or 73A-1) can be daisy-chained on a single SCSI bus, by interconnecting the SCSI-2 high density connectors on the front panel. The connectors are identical; either can serve as input or output. Up to seven SCSI devices may reside on the bus, but the total bus length is limited to six meters by the SCSI standard. The SCSI bus must be terminated at each end with resistor networks or their equivalents, which require power. A wire in the cable is dedicated to this purpose. The SCSI Standard states that this line must be powered by all SCSI "Initiators". The Host interface normally serves this function, as well as providing back termination of the Bus. In accordance with the Standard, the Model 73A does not provide terminator power at either connector, but does provide continuity between connectors for terminator power from the host.

The SCSI bus is internally terminated within the Model 73A by resistor networks in sockets at locations shown in Figure 1. These resistors are powered by the Crate, and do not use the TERTMPWR line in the SCSI bus. The unit is normally shipped with these networks in place, and they should be removed from all but the last controller in a multi-crate system. Alternatively, all terminators can be removed, and a SCSI terminator plug inserted in the unused bus connector of the last device. If it is required that the Model 73A power the bus terminator line in the cable, the factory should be contacted.

NOTE:

If an internally terminated controller is powered down, the SCSI bus will malfunction. However, a controller that is not terminating the SCSI bus may be powered down. If it is desired to power down the last (or only) controller on the bus, the internal terminators may be removed and a terminator plug placed in the unused connector.

3.5 SCSI ID

The SCSI ID of the controller is set by a front panel thumbwheel switch. An ID between 0 and 7 must be selected that differs from all other devices on the bus (including the host). If LAMs are expected from several different crates, the higher IDs should be assigned to crates with the higher priority LAM sources, since the bus arbitration protocol favors higher device IDs. Note that if the SCSI ID of the controller is changed while the crate is powered, a reset is necessary before the changed ID is recognized.

3.6 Station

The standard Model 73A (master only) must be installed in the rightmost two CAMAC stations. The Model 73A-1 may be installed in any stations, but a master controller or equivalent must reside in the rightmost position.

The Model 73A-1 has three multi-pole piano switches at the rear, between the finger areas of the circuit boards. For master operation, all switches must be ON, and the module must be placed in the rightmost two stations of the crate. For operation as an auxiliary controller, the switches must be "OFF. In this case the controller can reside in any stations except the rightmost (control) station.

3.7 Auxiliary Control Bus

If more than one controller resides in a crate, all must be interconnected by the Auxiliary Control Bus. This is a 40-wire ribbon cable that interconnects the rear connectors found on all controllers above the Dataway fingers. If the model 73A-1 is to be used as an auxiliary in conjunction with a serial crate controller, a modified auxiliary control bus is used. Refer to the appropriate manual for the connections.

4.0 Indicators

There are three indicators on the front panel of either model. The D light will be on if there is any unmasked LAM asserted in the Crate. If the LAM Mask is disabled, the D light will be illuminated if there is a LAM from any station.

The I light will be on if the Dataway Inhibit line is asserted, either by the Model 73A or another controller. The user should be aware that the effect of Inhibit depends only on the specific CAMAC modules in use. No features of the Crate Controller are affected by Inhibit. An off-line controller does not assert Inhibit.

The R/G ON light tells the operator the position of the internal switch selecting the Request/Grant or ACL arbitration mode.

5.0 Operation

Besides the SCSI ID switch, discussed earlier, the only operator controls on either model are the ON/OFF line switch, and a two-position momentary switch that generates the Dataway Initialize (Z) or Clear (C) CAMAC cycles. In the Off-Line state, the controller responds appropriately to SCSI protocol commands, but will not perform CAMAC cycles. Instead, an error status is returned. The Z/C switch is only active in the Off-Line state. Manual C affects only CAMAC modules, and does not change the internal state of the Controller. Manual Z initializes all CAMAC modules as well as the controller. It is equivalent to power-on reset. It sets Dataway Inhibit, disables LAMs, and establishes the SCSI UNIT ATTENTION condition. The controller can be switched off line, and the manual Z switch actuated at any time, without causing SCSI protocol errors, as the action is delayed until the controller is idle. Manual Z should be used if the controller's SCSI ID has been changed while the crate is powered, so that the new ID is recognized. Manual Z does not affect other devices on the SCSI bus.

6.0 Programming

In order to issue a command to the Model 73A, the host interface must perform the following tasks, in the appropriate SCSI Bus phase. Many of these tasks are automatically performed, in a fashion transparent to the user, by the port driver provided by most processor vendors.

1. Bus Arbitration
2. Select the Controller
3. Send the Identify message
4. Send the Command Descriptor Block
5. Send or Receive Data
6. Receive the Status Byte
7. Receive the Command Complete Message

Bus Arbitration is only required if there are devices on the bus, other than the host interface, that might become SCSI Initiators. Note that the Model 73A Controller can become a (temporary) Initiator for the purpose of transmitting a LAM message. Therefore, arbitration by the host is required if LAM's are enabled. The hardware of the host SCSI interface normally performs the Arbitration procedure, but this can be skipped if there are no other potential Initiators.

The Controller is selected by asserting the SCSI Data line corresponding to the Controller ID, together with the SCSI SEL signal. The line associated with the host ID may optionally be included. The selected Controller will respond by asserting the SCSI BSY signal, and enter target mode. The SCSI target determines the type and direction of data transfer on the bus by controlling the signals C/D, I/O, and MSG. These signals determine the bus "Phase", in accordance with the following table:

Phase	C/D	I/O	MSG
Command	1	0	0
Data Out	0	0	0
Data In	0	1	0
Status	1	1	0
Message Out	1	0	1
Message In	1	1	1

The "In" direction indicates a transfer from the target to the Initiator (controller to host). The host interface, acting as Initiator, should monitor the bus phase, and send or receive the type of data requested by the target. Since

the sequence of bus phases is normally known to the host, an anomalous phase is indicative of an error condition. The Message Phases are used for physical path management, and to recover from error conditions.

In accordance with the SCSI-2 specification, the host should select the model 73A with the ATN signal asserted, causing the controller to enter the Message Out phase initially. The Controller then expects the host to send a one byte IDENTIFY message that selects the logical unit within the target. This message is described in section 7. If the host continues to assert ATN, the Controller will remain in Message Out phase, and the host may send another message such as a SYNCHRONOUS DATA TRANSFER REQUEST. When ATN is no longer asserted, the Controller enters Command Phase, and expects the host to send a Command Descriptor Block. The following commands are accepted by the Model 73A:

1. INQUIRY

2. TEST UNIT READY

3. REQUEST SENSE

4. CAMAC Commands

The Command Descriptor Blocks accepted by the Model 73A are either 6 or 10 bytes long, and will be described in the next section. Following the Command Phase, the Controller will enter Data Phase if the command involves a data transfer, is valid, and contains no errors. Following this, the Controller will enter Status Phase, and send one byte of status. If the command is invalid, does not involve a data transfer, or for some reason cannot be performed, the Controller will proceed directly from Command Phase to Status Phase. Only three possible status bytes are generated by the Model 73A:

Value	Status
0	GOOD
2	CHECK CONDITION
4	CONDITION MET

CHECK CONDITION status indicates an error. The REQUEST SENSE command may be used to determine the cause. CONDITION MET status is used to return the value of the CAMAC Q signal during a CAMAC non-data command. A status of 4 indicates Q=1; Status 0 indicates Q=0. Data transfer commands will not return CONDITION MET status. Following the Status Phase, the Controller will enter Message In phase, and send a single null byte as required by the standard. It will then cause the bus to go free. Linked commands are not presently supported by the Model 73A.

6.1 INQUIRY Command

The INQUIRY command may be issued at any time to determine the characteristics of any logical unit on any target. 36 bytes of information are returned indicating the type of device attached, the manufacturer, model number, and revision level. This command is generally issued by an operating system at start-up, but may be issued by a user. The Command Descriptor Block is as follows:

INQUIRY Command

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (12h)							
1	Logical Unit Number			Reserved				EVPD
2	Page Code							
3	Reserved							
4	Allocation Length							
5	Vendor Specific		Reserved				Flag	Link

All reserved fields in all SCSI commands must be zero. In accordance with the Standard, The Model 73A will reject any command violating this rule. The only valid Logical Unit Number for the Model 73A is 0. The EVPD, Page Code, Vendor Specific, Flag, and Link fields must also be 0. The Allocation Length is the number of data bytes that the host expects the Controller to return, and is typically 36 (decimal)/ but may be less (in which case the returned data will be truncated).

The data returned by the Model 73A conforms to Table 7-15 of the SCSI Standard. The Peripheral Device Type will be 03h. The Peripheral Qualifier will be 000b if the Controller is on-line, or 001b if off-line. If a non-zero logical unit is specified (in the preceding IDENTIFY message), the Peripheral Qualifier will be 011b. The INQUIRY command will return GOOD Status unless an improper bit is detected in the Command Descriptor Block.

NOTE:
Controllers prior to SN 354 reported device type lFh which is improperly handled by Windows 95.

6.2 TEST UNIT READY Command

The TEST UNIT READY command is a rapid way to determine if the Controller is ready to accept data transfer commands, since there is no associated data phase. The TEST UNIT READY command returns GOOD status if the Controller is ready. There are two situations in which it may not be ready, and will return CHECK CONDITION status in response to this command: (a) The Controller has been switched off-line, or (b) The UNIT ATTENTION condition exists. The UNIT ATTENTION condition is established at crate power-up, by SCSI Bus Reset, by receipt of a BUS DEVICE RESET message, or by a manual Dataway reset (manual Z). While the UNIT ATTENTION condition exists, CAMAC commands and the TEST UNIT READY command return CHECK CONDITION status, and CAMAC commands cannot execute. After this status is transmitted, a "Contingent Allegiance" is said to exist, and the UNIT ATTENTION is cleared. A REQUEST SENSE command, if issued at this time would return a Sense Key indicating UNIT Attention. Note that the sense data is cleared after a REQUEST SENSE command or if another TEST UNIT READY or CAMAC command is issued.

NOTE:

The Model 73A will be ready to process SCSI commands within 25 microseconds of power-up or reset. It will however be in the Unit Attention condition, which must be removed before CAMAC transfers can take place (including CAMAC non-data commands). This can be done by issuing a single TEST UNIT READY command (which will return Check Condition status). It is not necessary to issue a REQUEST SENSE command but if this is not done an error in the command itself will go undetected. Conservative practice is to issue TEST UNIT READY commands until GOOD status is returned.

The format of the TEST UNIT READY command follows:

TEST UNIT READY Command

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (00h)							
1	Logical Unit Number			Reserved				
2	Reserved							
3	Reserved							
4	Reserved							
5	Vendor Specific		Reserved				Flag	Link

The Logical Unit field, Reserved fields, and all fields of byte 5 should be 0. If any are non-zero, CHECK CONDITION status will be returned and a Sense Key of "illegal request" established for a future REQUEST SENSE command. A similar result will be obtained if the preceding IDENTIFY message specified a non-zero logical unit. The two conditions differ in the "Additional Sense Code", as noted later.

6.3 REQUEST SENSE Command

The REQUEST SENSE command is normally issued after a CHECK CONDITION status is returned by any command, to determine the reason. The format of the Command Descriptor Block follows:

REQUEST SENSE Command

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (03h)							
1	Logical Unit Number			Reserved				
2	Reserved							
3	Reserved							
4	Allocation Length							
5	Vendor Specific		Reserved				Flag	Link

Bytes 1,2,3, and 5 should be 0, or the command itself will return CHECK CONDITION status ("illegal request"). The Allocation Length is the number of bytes the host expects in reply. In accordance with the Standard, the Model 73A can return 18 (decimal) bytes of sense data, using the format and codes specified in the Standard. The reply format follows. It will be noted that the last 5 bytes of the standard reply convey no useful information in the present context, so that an improvement in throughput could be achieved by lowering the allocation length to 13.

Sense Data Format

Bit Byte	7	6	5	4	3	2	1	0
0	Valid	Error Code (70h)						
1	Segment Number (0)							
2	0	0	0	0	Sense Key			
3	FIFO Status							
4 thru 6	(MSB) DMA Byte Count (LSB)							
7	Additional Sense Length (10)							
8 thru 11	0							
12	Additional Sense Code							
13 thru 17	0							

The following Sense Keys may be returned by the Model 73A:

Sense Key	Description
0	NO SENSE- No specific sense key is available. Would be the case if a REQUEST SENSE were issued after a successful command.
2h	NOT READY- Controller was off-line
4h	HARDWARE ERROR- Parity error during data transfer or CAMAC module did not return X signal.
5h	ILLEGAL REQUEST- A non-zero logical unit was selected, or a command was issued that is not implemented or contained an improper bit (possibly in IDENTIFY msg.)
6h	UNIT ATTENTION- The Controller has been reset.
9h	SHORT TRANSFER- A stop-mode block transfer did not transfer the expected number of bytes because a CAMAC cycle failed to return the Q signal.
Bh	ABORTED COMMAND- The Controller aborted the command.

In those cases where the sense key leaves some doubt as to the exact cause of an error, the Additional Sense Code provides more specifics. The following ASC's from the SCSI-2 Standard may be encountered:

00h	No additional sense information.
04h	Controller off-line.
20h	Invalid Command Operation Code.
24h	Invalid field in CDB.
25h	Logical unit not supported.
29h	Power on reset or Bus Device Reset occurred.
3Dh	Invalid bit in IDENTIFY message.
44h	CAMAC Cycle did not return X=1.
47h	SCSI Parity error.
48h	INITIATOR DETECTED ERROR message received
80h	CAMAC cycle did not return Q=1.

Bytes 4 through 6 are the "information" field of the standard sense reply, and pertain to improperly terminated block transfers. They will be described later.

6.4 CAMAC Commands

The SCSI Standard does not provide for a device like a CAMAC crate. Therefore, non-standard Command Descriptor Blocks are used, following the IDENTIFY message of the SCSI-2 specification. Both 6 and 10 byte commands are used, the latter only for block data transfers of 256 or more bytes in length.

6.4.1 CAMAC Non-Data Commands-

A CAMAC non-data command has a function code between 8 and 15, or between 24 and 31 (the F8 bit set). The Command Descriptor Block for a non-data CAMAC command consists of 6 bytes as follows:

CAMAC NON-DATA Command

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (01h)							
1	Logical Unit Number			F16	1	F4	F2	F1
2	0	0	0	N16	N8	N4	N2	N1
3	0	0	0	0	A8	A4	A2	A1
4	0							
5	Control Byte (0)							

After the command is executed, the Controller proceeds to the Status Phase, and returns one of the following status bytes, and then the Command Complete message (which is null):

Status Byte	Description
0	GOOD Status, Q=0
2	CHECK CONDITION (Error)
4	GOOD Status, Q=1

If CHECK CONDITION status is returned, the REQUEST SENSE command may be issued to determine the reason.

6.5 CAMAC Data Transfers

CAMAC data transfers use the same Operation Code (Byte 0) for reads and writes (unlike other SCSI commands). The distinction is conveyed in the CAMAC Function Code within the Command Descriptor Block. A distinction is made, however, between commands with a transfer length less than 256 bytes, and those with 256 or more. Short transfers use a 6 byte Command Descriptor Block, and long transfers 10. Either type of transfer may made in either 16 or 24 bit mode. The former only transfers data on the low order 16 data lines of the CAMAC Dataway, and therefore requires only two bytes to transfer a CAMAC word on the SCSI Bus. In 24 bit mode, all Dataway data lines are used, and three bytes are required for each Dataway cycle. In order to align memory data on fullword boundaries in 24 bit mode, a null byte is inserted in the SCSI data stream as the most significant byte of each CAMAC word transferred. Transfer lengths are always stated in bytes, and therefore will be two or four times the number of CAMAC words involved.

NOTE:

Inexperienced CAMAC users are often disturbed to find non-zero bits appearing on the high order eight Dataway write lines (W17-W24) when using 16-bit mode. This is unavoidable, as the Dataway is "hard-wired" to use 24 bits. If it is desired to use 16-bit mode with modules sensitive to all 24 bits, a single 24 bit write command may be issued with a null high order byte. Following this 16 bit mode may be used, and the high order bits will be 0.

6.5.1 Short CAMAC Transfers

The Command Descriptor Block for transfers of less than 256 bytes consists of the following 6 bytes:

CAMAC Short Data Transfer Command

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code (01h)							
1	Logical Unit Number			F16	0	F4	F2	F1
2	M1	M2	S	N16	N8	N4	N2	N1
3	0	0	0	0	A8	A4	A2	A1
4	Transfer Length							
5	Control Byte (0)							

6.5.2 Long CAMAC Transfers

CAMAC data transfers with a length of 256 or more bytes use a 10 byte Command Descriptor Block as follows:

CAMAC Long Data Transfer Command

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code (21h)							
1	Logical Unit Number			Reserved				
2	Reserved			F16	0	F4	F2	F1
3	M1	M2	S	N16	N8	N4	N2	N1
4	0	0	0	0	A8	A4	A2	A1
5	Reserved							
6 thru 8	(MSB) Transfer Length (LSB)							
9	Control Byte (0)							

6.5.3 Transfer Modes

For either short or long transfers, the M1 M2 and S bits specify the mode of transfer as follows:

M1	M2	S	Transfer Mode
0	0	0	Single Word, 16 bit Mode
0	1	0	Address Scan, 16 bit Mode
1	0	0	Q-Stop, 16 bit Mode
1	1	0	Q-Repeat, 16 bit Mode
0	0	1	Single Word, 24 bit Mode
0	1	1	Address Scan, 24 bit Mode
1	0	1	Q-Stop, 24 bit Mode
1	1	1	Q-Repeat, 24 bit Mode

In Address Scan mode, consecutive Subaddresses are addressed until either Subaddress 15 is finished, or a CAMAC cycle returns Q = 0. The Station number is then incremented, and the process continues until the transfer length is satisfied or N24 is reached. In Q-Stop or Q-Repeat mode, the Station and Subaddress remain fixed at the initial value. If M2 = 0, the transfer terminates if Q = 0. If M2 = 1, data is not transferred if Q = 0, but CAMAC cycles continue as long as X = 1. All transfer modes terminate if the transfer length is satisfied or an error occurs, and the Controller proceeds to the Status Phase.

Single Word mode is included to permit reading the few CAMAC modules that do not return Q = 1 when transferring valid data. Transfers of a single CAMAC word may be made in Q-Stop mode or with M1 = M2 = 0. In the former case, data from a CAMAC read operation will not be transferred to the host if the command returns Q = 0, and CHECK CONDITION status will be returned. If M1 = M2 = 0, data will always be transferred to the host, and GOOD status returned even if Q = 0. The user cannot tell what Q response was returned. The destination between the 2 modes is moot for write operations, since the data is transferred before Q response is returned. Single Word mode can not be used for transfers of longer than one CAMAC word.

NOTE:

Early models of the 73A returned CHECK CONDITION status in response to Single Word mode transfers that detected Q = 0, although data was transferred.

CAMAC data transfer commands return only two possible status bytes, GOOD (0) or CHECK CONDITION (2). CHECK CONDITION status will be returned any time the transfer length is not satisfied, or if the transfer terminates with X or Q equal to 0. The REQUEST SENSE command can be issued to determine the cause of termination, and the number of bytes successfully transferred. Byte 3 of the sense data is the number of bytes remaining in the internal FIFO of the Controller. Bytes 4 through 6 contain a value that is the number of bytes remaining to be transferred on the SCSI bus. In other words, the value in bytes 4-6 is subtracted from the programmed byte count, to yield the number of bytes transferred on the SCSI bus. This value may also be obtained by counting bytes at the host end. In the case of CAMAC reads, this value, plus the number of bytes remaining in the FIFO, yield the number read from CAMAC modules. If the transfer was done in 24 bit mode, this value includes the "filler" bytes, and must be divided by 4 to obtain the number of CAMAC Dataway cycles. In 16 bit mode, it should halved.

In the case of CAMAC writes, the number of bytes remaining in the FIFO must be subtracted from the number of SCSI transfers to determine the number of Dataway cycles completed. Furthermore, if a Q-Stop write transfer terminates due to (lack of) Q response, the above calculation will produce a value one higher than the actual number of successful (Q=1) Dataway transfers, since the cycle resulting in Q=0 is counted. In the case of CAMAC reads, a cycle returning Q=0 does not result in a data transfer, except in single-word mode.

6.5.4 Controller Commands

The Controller itself responds to the following CAMAC commands, resulting in the actions indicated. Except for the last one, these are the same commands used with the standard type A Crate Controller.

ACTION	COMMAND	RESPONSE
Generate Dataway Z	F(26)N(28)A(8)	Q=0
Generate Dataway C	F(26)N(28)A(9)	Q=0
Read LAM Pattern	F(0)N(30)A(0-7)	Q=1
Load Station Number Register	F(16)N(30)A(8)	Q=1
Remove Dataway Inhibit	F(24)N(30)A(9)	Q=0
Set Dataway Inhibit	F(26)N(30)A(9)	Q=0
Disable Demands	F(24)N(30)A(10)	Q=0
Enable Demands	F(26)N(30)A(10)	Q=0
Overwrite LAM Mask	F(16)N(30)A(0)	Q=0

In addition to the above commands, commands addressed to N(24) select all stations stored in the Station Number Register, and N(26) addresses all stations simultaneously.

7.0 Asynchronous Event Notification

If LAMs are enabled (F(26)N(30)A(10)), and a LAM arises in an enabled CAMAC module, the Model 73A will become a temporary Initiator and will inform the host using the SCSI-2 AEN procedure. It will arbitrate for the bus, select the host SCSI adapter, and send the IDENTIFY message followed by the SCSI SEND command. The host adapter must have been programmed to execute the proper Target mode phases. The SEND command instructs the Target (the host adapter) to transfer data from the Initiator (the Crate Controller). The SEND command, described in Table 11-3 of the Standard, will have a transfer length of 4 bytes, and an AEN bit of zero. This informs the host that the data format is vendor-specific. During the ensuing data phase, the Controller sends 4 bytes that convey the pattern of all LAMs asserted in the crate (not merely the one initiating the request). The byte order is the same as for a CAMAC data transfer in 24-bit mode, including the null filler byte. The least significant bit of the fullword corresponds to the LAM from station number 1, and so on up to station 24.

The host interface must be capable of executing the AEN procedure, or else LAMs should not be enabled. The Controller does not check that the host has this capability. However, the Controller does clear the UNIT ATTENTION condition in the host interface, using the TEST UNIT READY command prior to sending its first LAM message. The Target (host) is expected to send the status byte and COMMAND COMPLETE message in response to command, although the contents of these bytes are not checked. It is assumed that the TEST UNIT READY command clears the host UNIT ATTENTION.

8.0 Messages

The Model 73A responds to the following SCSI messages:

IDENTIFY
ABORT
BUS DEVICE RESET
INITIATOR DETECTED ERROR
MESSAGE PARITY ERROR
MESSAGE REJECT
NO OPERATION
SYNCHRONOUS DATA TRANSFER REQUEST

The IDENTIFY message is the SCSI-2 method of selecting the Logical Unit within a target. If a non-zero Logical Unit is specified in the IDENTIFY MESSAGE, the ensuing command will fail. The IDENTIFY message is one byte long as follows:

IDENTIFY MESSAGE

Bit	7	6	5	4	3	2	1	0
	1	0	0	0	0	Logical Unit Number		

NOTE:

It will be noted that there is also a Logical Unit Number field in the Command Descriptor Blocks described earlier. This field has been maintained in the SCSI-2 Specification for compatibility with SCSI-1. If the Logical Unit is conveyed by the IDENTIFY message, this field is not used, and should be set to zero.

The ABORT message interrupts the currently executing command, and the Controller enters the BUS FREE phase. The BUS DEVICE RESET message causes a hardware reset of the Controller. A Dataway Z is generated, and the UNIT ATTENTION condition is set. LAMs are disabled, and Dataway Inhibit asserted. If synchronous transfers were in effect, the Controller reverts to asynchronous mode.

The INITIATOR DETECTED ERROR message causes the Controller to terminate the current command, and return CHECK CONDITION status. A subsequent REQUEST SENSE command will return a sense key of 0Bh, and an ASC of 48h. Note that early versions of the Model 73A responded to this message by retrying the current command.

The MESSAGE PARITY ERROR message causes the Controller to resend the previous message. The MESSAGE REJECT message causes the Controller to perform an "unexpected disconnect". This should not occur, due to the limited and well defined message repertoire of the Model 73A.

The SYNCHRONOUS TRANSFER REQUEST message causes the Model 73A to prepare to use synchronous transfers in future data phases, and to return a similar message confirming the parameters it will use. This message is 5 bytes long as follows:

Byte	Contents
0	1
1	3
2	1
3	Transfer Period
4	REQ/ACK Offset

The Transfer Period is specified in units of 4 nanoseconds. The Model 73A can transfer at a 5 mbyte/sec. rate, and accordingly returns the value 50 (decimal) in byte 3, or a lower value if proposed by the host. A value of 8 is returned in byte 4 unless the host proposed a smaller offset.

The Model 73A generates the following SCSI messages under the appropriate circumstances. The host must be prepared to process them.

COMMAND COMPLETE
SYNCHRONOUS DATA TRANSFER REQUEST

The COMMAND COMPLETE message is one byte transmitted in MESSAGE IN phase at the completion of every command, after the STATUS Phase. Since the Model 73A does not support linked commands, this

message is always NULL. The SYNCHRONOUS DATA TRANSFER REQUEST message is only generated in response to a similar message from the host. The Model 73A will not initiate synchronous transfers. All AEN transfers use asynchronous mode. Since some operating systems are not prepared to accept the MESSAGE REJECT or MESSAGE PARITY ERROR messages, the Model 73A does not generate either. In the event that it receives corrupted or invalid message, it merely disconnects from the bus. This "unexpected disconnect" informs the host that an error has occurred. However, the response to an invalid IDENTIFY message is sent in Status Phase, as noted earlier.

During Asynchronous Event Notification, the Model 73A generates the IDENTIFY message to convey the host's Logical Unit Number, which is expected to be zero. It further expects the host to send the COMMAND COMPLETE message after sending the status byte.

9.0 Mailbox

The Model 73A incorporates a 24 bit "Mail Box" register to facilitate communication between its SCSI host and another processor connected to (or incorporated in) another controller in the same Crate. The mailbox can be overwritten or read either by the SCSI host, or by another controller using the Dataway. The host accesses the mailbox using CAMAC commands addressed to station 28. Another controller addresses it at the station number corresponding to the right hand slot occupied by the Model 73A (station 25 if the Model 73A is in the control station).

Associated with the mail box is a flag that can be used to interlock communication between the controllers using Q response. In addition, a LAM flip-flop is included that can set by Dataway command. As noted in Section 3, the LAM can be detected by either controller. These features utilize the following commands:

F(0)A(0)	Read contents of mail box
F(0)A(1)	Read contents. Return Q=1 if flag set, else Q=0. Clear Flag.
F(16)A(0)	Overwrite mail box
F(16)A(1)	Overwrite if flag clear, set flag and return Q=1. If flag is set, return Q=0 but do not overwrite.
F(8)A(0)	Test LAM
F(10)A(0)	Clear LAM source
F(14)A(0)	Set LAM source
F(24)A(0)	Disable LAM
F(26)A(0)	Enable LAM

NOTE:

Starting with Serial number 454, the model 73A incorporates the mailbox as a standard feature. This feature can be used to test data transfers, Q response, and lam response without the need for special modules. Unlike the Model 73A-1, the mailbox is enabled by default. Since the standard Model 73A incorporates the auxiliary control bus, the mailbox can also be accessed by an auxiliary controller, as noted above.

10.0 FASTCAMAC Option

The Model 73A-2 can perform Level 1 FASTCAMAC read operations in accordance with document DOE/SC-0002, endorsed by the U.S. NIM committee. This feature is enabled by switch #2. In this mode, the CAMAC cycle is expanded to consist of multiple S1 pulses at a nominal interval of 400 nanoseconds, terminated by a single S2 pulse. Used with a CAMAC module that is designed to transfer a CAMAC word on every S1, a transfer rate of 7.5 Mbytes/second is possible. For this to be achieved, the SCSI host adapter must be capable of transferring at least 10 Mbytes/second in synchronous SCSI mode. A FASTCAMAC level 1 read is performed using CAMAC function code F(5), with a transfer length greater than 1 CAMAC word. No modification of existing software is required.

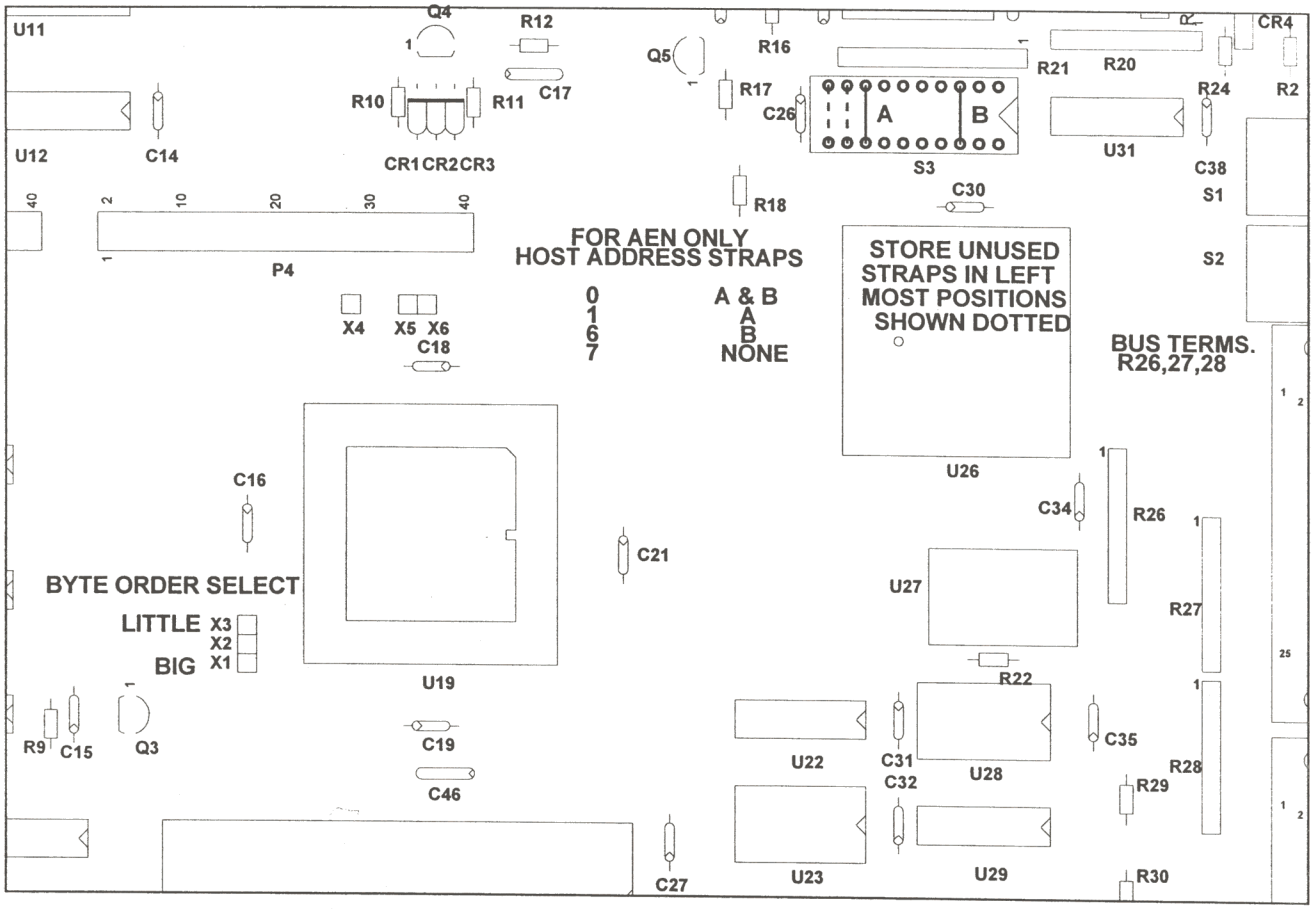
U11
Q4
R12
Q5
R16
R21
R20
CR4
R10
R11
C17
R17
C26
A
B
R24
R2
U12
C14
CR1 CR2 CR3
S3
U31
C38
S1
R18
C30
FOR AEN ONLY
HOST ADDRESS STRAPS
0
1
6
7
A & B
A
B
NONE
STORE UNUSED
STRAPS IN LEFT
MOST POSITIONS
SHOWN DOTTED
S2
BUS TERMS.
R26,27,28
P4
X4
X5 X6
C18
C16
U26
C34
R26
C21
U27
R27
BYTE ORDER SELECT
LITTLE X3
X2
BIG X1
U19
R22
R9
C15
Q3
C19
C46
U22
C31
U28
C35
R28
C32
R29
U23
U29
R30
C27

FIGURE 1