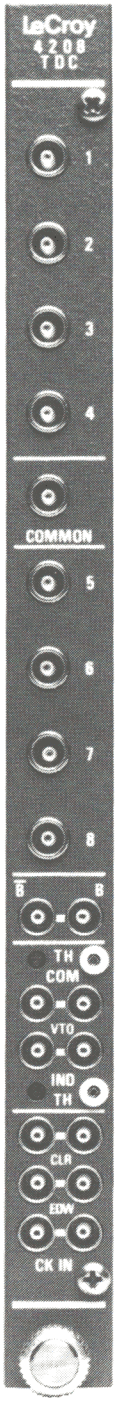
TECHNICAL DATA

LeCroy



CAMAC Model 4208

8 Channel Wide Range Real-Time TDC

- **8 channels in a single width CAMAC module**
- **24-bit dynamic range**
- **High resolution: LSB = 1 nsec**
- **Mixed common START/STOP operations**
- **Common fast clear input**
- **Minimum dead time due to the real-time technique**

The LeCroy Model 4208 Time-to-Digital Converter (TDC) is designed to cover applications where time measurements must be performed in real time, and require wide dynamic ranges with high resolution.

The Model 4208 has eight independent channels, each of which measures the time from the leading edge of a common input pulse to the leading edge of its individual input pulse.

Due to the particular design, common start input mode as well as common stop input mode can be used. The TDC will encode input pulses preceding the common input as negative times and input pulses arriving after the common input as positive times.

The 4208 TDC may also operate as a single channel multi-hit (8) TDC. In this strap selectable mode, all eight channels are cascaded, each channel hit enables the next one. The unit may also be configured as a dual channel TDC with multi-hit (4), a quad TDC with double hit, or almost any combination of mulit-hit.

The 4208 converts the measured time intervals into a 23-bit digital word plus a 24th sign bit which indicates whether or not the common input has preceded the individual input. This corresponds to a dynamic range of ± 8.3 msec (which is expandable with an external clock and appropriate logic circuits).

The module is equipped with a high stability crystal controlled 125 MHz clock. The 1 nsec resolution is realized by digital interpolation between two clock pulses. Dead time after an event has occurred is negligible and data readout can occur immediately after the event.

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Innovators in Instrumentation

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SPECIFICATIONS
CAMAC Model 4208
8 CHANNEL WIDE RANGE REAL-TIME TDC

INPUTS

8 Individual Inputs:	One Lemo-type connector per channel, impedance 50 Ω; protected to ± 3 A for 0.5 μsec, clamping at + 6 and − 6 V; each input is followed by a fast discriminator, minimum input pulse width is 4 nsec; threshold is common to the 8 channels and is adjustable by a front panel potentiometer (IND TH) from − 1.5 V to + 1.5 V; threshold precision ± 20 mV; 10× threshold monitor on the front panel. Multi-hit selectable by internal straps.
Common Input (COMMON):	One Lemo-type connector, high impedance 50 Ω; protected to ± 3 A for 0.5 μsec, clamping at + 6 and − 6 V; the input is followed by a fast discriminator, minimum input pulse width is 4 nsec; threshold adjustable by a front panel potentiometer (TH) from − 1.5 V to + 1.5 V; 10× threshold monitor on the front panel.
Individual Veto Inputs (IND):	Two bridged Lemo-type connectors, high input impedance; accepts NIM levels; the eight individual inputs are inhibited for the duration of the veto; active for the first hit only in multi-hit mode.
Common Veto Inputs (VTO):	Two bridged Lemo-type connectors, high input impedance; accepts NIM levels; the common input is inhibited for the duration of the veto.
End of Time Window (EDW):	Two bridged Lemo-type connectors; high input impedance; accepts NIM level pulses; LAM is generated in response to the leading edge allowing readout of the unit. Internal monostable provided, range adjustable from 0.2 to 8 msec (set at factory to 8 msec); OR'd with the external EDW input; can be disabled via internal strap.
Fast Clear Input (CLR):	Two bridged Lemo-type connectors; high input impedance; accepts NIM levels; the unit is ready to operate approximately 50 nsec after the trailing edge of the Fast Clear Input. Clear input width: > 50 nsec. Does not clear the LAM
External Clock Input (CK IN):	Two bridged Lemo-type connectors; high impedance NIM input active in external clock mode only. Permits: absolute time accuracy improvement, and time range expansion (clock suppression during "no event deadtime"). Note: If the duty cycle of external clock is not 50% ± 5%, time linearity can be affected.

OUTPUTS

BUSY Output ($\overline{B}$ and B):	Two Lemo-type connectors; two NIM levels are started by a nine-input OR of the eight individual inputs and the common input, and are stopped by the clear; allow various input veto logic combinations; complementary outputs are provided.

CAMAC COMMANDS

Z, C:	Initialize module; clears all channels and clears the LAM.
I:	Inhibits all channel inputs during CAMAC inhibit command.
Q:	Conditional response for F(0), F(2), F(8), F(10).
X:	X = 1 response is generated for each valid function.
L:	When enabled (jumper option), LAM is generated by the unit in reponse to either the "End of Time Window" input or the internal monostable pulse, whichever comes first.
F(0)•A(0) to A(7):	Addressed readout; read data on Read Lines (2's complement convention); Q = 0 if an empty channel is read; Q = 1 otherwise.
F(2)•A(0) to A(7):	Addressed readout as for F(0); F(2)•A(7) clears the unit at S2; does not clear the LAM.
F(8)•A(0):	Test Look-at-Me; Q = 1 if LAM is present.
F(9)•A(0):	Clears unit; resets LAM and all channels.
F(10)•A(0):	Test and clear Look-at-Me; Q = 1 if LAM is present.

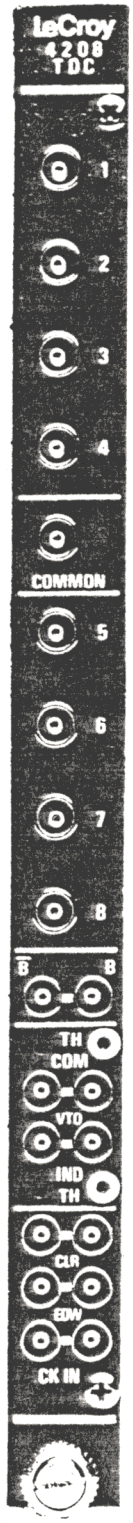
GENERAL

Resolution:	± 1 nsec
Dynamic Range:	23 bits + 1 bit for sign. Expandable via external clock mode.
Integral Non-Linearity:	± 1 count
Encoding Time:	None, the time is encoded in real time.
Multi-hit Dead Time:	Inherent dead time (time reference at front panel Lemo-type connector): 3 nsec typical.
Packaging:	Single width CAMAC standard module.
Power Requirements:	1.5 A at 6 V; 3.3 A at − 6 V; 17 mA at + 24 V; 17 mA at − 24 V.

SPECIFICATIONS SUBJECT TO CHANGE

MODEL 4208

FRONT PANEL



(8) Individual Inputs (Section 1.3)

Common Input (Section 1.3)

Busy Outputs (Section 1.8)

Threshold for Common Input (Section 1.3)

Common Input Veto (Section 1.5)

Individual Input Veto (Section 1.5)

Threshold for Individual Inputs (Section 1.3)

External Clear Input (Section 1.4)

End of Window Input (Section 1.6)

External Clock Input (Section 1.7)

SECTION 1

OPERATING INSTRUCTIONS

1.2 General

The LeCroy Model 4208 8-channel, Real Time TDC (Time-to-Digital Converter or Time Interval Meter) contains 9 independent time encoding channels; one COMMON and 8 INDIVIDUAL channels.

The 4208 TDC converts the time difference between a signal at the COMMON input and any INDIVIDUAL input signal into a 24-bit signed number (2's complement convention). The module may operate in COMMON stop mode, COMMON start mode or mixed START and STOP mode.

An INDIVIDUAL channel hit before the COMMON input will record a negative time, while an INDIVIDUAL channel hit after the COMMON input will indicate a positive time.

The total time range, with the 24-bit signed number and the 1 nsec resolution, is $\pm$ 8.3 msec with respect to the COMMON input occurrence time.

Basically, the 4208 TDC can be in one of two different modes:

a. Ready to Operate
b. Ready for Readout

Upon receipt of a 'CLEAR', the TDC is in the Ready to Operate mode and can accept the input signals. When an 'End of Window' is encountered, it is set to the Ready for Readout mode and can be read out via CAMAC.

1.3 Inputs

The 9 (1 COMMON + 8 INDIVIDUAL) inputs are internally terminated with 50 Ω impedance and detect either negative or positive crossing of the thresholds. The amplitude of the input signal should not exceed 3 Volts (input level: $<$+3V or $>$-3V) for correct operation of the input stage.

There are two threshold levels, one for the COMMON input and the other for the 8 INDIVIDUAL inputs. These threshold levels can be adjusted between $\pm$ 1.5 V by two front panel, 10 turn potentiometers. 10x threshold monitors are provided.

Negative versus positive edge detection is selected by removing the side cover and setting the appropriate STRAPS in the desired position (see 4208 JUMPER OPTIONS, Figure 1.2).

To permit multi-hit mode operation, each of the last seven INDIVIDUAL inputs (CH 2 to CH 8) can be disconnected from its LEMO connector and connected in parallel to the previous input with a strap (see 4208 JUMPER OPTIONS, Figure 1.2). Detailed discription of mode of operations is given in Section 1.9.

WARNING: Multi-Hit Mode is not available for ECO's #1001 and 1002.

All 9 (1 COMMON + 8 INDIVIDUAL) inputs are protected to ± 3 A for 0.5 µsec clamping at ± 6 V.

1.4 External Clear Input (CLR)

The CLR input is high impedance (> 5 kΩ) and accepts NIM level signals. Two bridged LEMO-type connectors permit cascading the clear signal across several units. The last unit in the chain must be terminated with 50 Ω

A CLR pulse (see also NIM specs, Appendix 3.1) of width greater than 50 nsec has the following effects:

- Clears all data values.
- Resets all logic signals inside the TDC except the LAM.
- Disables all 9 inputs for its duration + 50 nsec (50 nsec dead time after CLR pulse trailing edge).
- Sets the TDC into "the Ready to Operate" mode. All 9 channels (1 COMMON + 8 INDIVIDUAL) are 'armed' and will record the time of the next non-vetoed threshold crossing transition (see Section 1.5).

WARNING: CLR pulses of width < 50 nsec can cause incomplete clear action and result in improper TDC operation.

1.5 External Veto Inputs (COM and IND)

Two external veto inputs are provided. One for the COMMON input and one for all 8 INDIVIDUAL inputs.

The COM and IND veto inputs are high impedance (> 5 kΩ) and accept NIM level signals. Two bridged LEMO-type connectors permit the cascading of veto signals across several units. The last unit in the chain must be terminated with 50 Ω

A veto signal (see also NIM specs, Appendix 3.1) applied to the COM VTO will disable the COMMON input for its entire duration.

A veto signal (see also NIM specs, Appendix 3.1) applied to the IND VTO will disable all 8 INDIVIDUAL inputs for its entire duration.

When an input is disabled, any threshold crossing transition on that input is ignored. The trailing edge of the veto cannot trigger the corresponding channel(s) even if it occurs while a pulse is 'present' at the input. See Figure 1.1 for the precise timing relations of the veto actions.

1.6 External End of Window (EDW)

The EDW input is high impedance (> 5 kΩ) and accepts NIM level signals. Two bridged LEMO-type connectors permit the cascading of an EnD of Window signal across several units. The last unit in the chain must be terminated with 50 Ω

A HIGH to LOW NIM transition (see also NIM specs, Appendix 3.1) has the following effects:

- Disables all inputs, stops all real time counters and sets the TDC into the "Ready for Readout" mode.

- Sets LAM if enabled.

Note: The EDW HIGH to LOW transition must occur at least 10 nsec after the last input (any of 9) threshold crossing to be recorded. Input hits in time coincidence with the EDW transition may not be encoded accurately. They can easily be avoided by vetoeing all channels 10 nsec before the EDW transition.

WARNING: CLR action prevails over EDW action.

1.7 External Clock Input

The CK IN input is high impedance (> 5 kΩ) and accepts NIM level signals. Two bridged LEMO-type connectors permit cascading a CK IN signal across several units. The last unit in the chain must be terminated with 50 Ω.

The clock must be a highly stable 125 MHz, 50% duty cycle signal. The CK signal may be interrupted during a wait period of data acquisition in order to extend the time range beyond 8.3 msec. In doing so, remember that the real time counters are incremented by the positive edge of the CK IN input. Factory strap settings disable this input, (see 4208 JUMPER OPTIONS, Figure 1.2, to enable the CK IN input).

Note: a poor duty cycle CK IN signal can result in loss of the time monotonicity of the TDC (missing codes); extreme care must be taken if this input is to be used.

1.8 Busy Outputs

Two complementary NIM level output signals (see also Appendix 3.1) are provided for various veto or control applications. The BUSY output, reset by the CLR is set when the first pulse hits any INDIVIDUAL input or the COMMON input.

1.9 Single/Multi-Hit Mode

The option of operating in single or multi-hit mode can be chosen independently for each channel.

Internal strapping options (see 4208 JUMPER OPTIONS, Figure 1.2) permit the selection for each channel 2,3,...8 of first the source of the timing signal at the input of the TDC, and the source of the enable signal.

A channel is in single-hit mode when its input comparator is connected to the corresponding LEMO input connector, and its enable signal to the internal INDIVIDUAL VETO line. In this mode, a particular channel will operate independently from the other channels.

A channel is in multi-hit mode when its input comparator and its enable signal are connected in parallel to the input and the Q output of its adjacent channel respectively. A channel set in this way, remains in the disabled state until its adjacent channel has been hit. If many channels are cascaded, the first one will time the first occurring pulse of a burst, the second one will time the second pulse of the burst, and so on.

WARNING: Multi-Hit Mode is not available for ECO's #1001 and 1002.

The dead time between two pulses (DPR) is typically 3 nsec.

Note: The INDIVIDUAL VETO has no effect for each channel set to multi-hit mode.

1.10 CAMAC Control Functions

The CAMAC functions F(9)·A(0)·S2, Z·S2, C·S2 are "ORed" with the front panel CLR input and have the same effect as an external CLR pulse. In addition, the CAMAC functions reset the internal LAM flip-flop. When present, the CAMAC INHIBIT line (I) disables the COMMON input and all 8 INDIVIDUAL inputs (I is "ORed" with the common COM and with the individual VTO vetoes).

1.11 Internal EDW Monostable

An internal timer is provided for low data rate situations or applications where the EnD-of-Window can not be generated. The output of the internal timer is "ORed" with the external EDW input (see Section 1.6).

The timer is started by the BUSY signal (i.e., the first input pulse) and approximately 8 msec later (factory setting) an internal EDW signal sets the 4208 TDC into the Ready for Readout mode.

This timer can be disabled via internal strap setting (see 4208 JUMPER OPTIONS, Figure 1.2), and can be adjusted over a range from 200 μsec to 9 msec via an internal potentiometer.

See also note of Section 1.6.

1.12 LAM Handling

The 4208 TDC generates a LAM signal (CAMAC L line) each time it receives or internally generates (see Section 1.11) an EDW input signal (see Section 1.6).

An internal strap can be set to disable the LAM signal (L=0 always). See 4208 JUMPER OPTIONS, Figure 1.2.

LAM CAMAC commands:

F(8)·A(0) will give Q=1 if LAM present.

F(10)·A(0) will give Q=1 if LAM present and clear it at S2.

C·S2, Z·S2, F(9)·A(0)·S2 will clear the LAM flip-flop.

Note: The F(8) and F(10) functions are operational even if the strap has been set to suppress the L line activity.

1.13 Data and Readout

The LeCroy Model 4208 is a 24-bit, 1 nsec resolution real time TDC. The full scale range goes from -2^{23} to $2^{23}-1$ nsec (approximately $\pm$ 8.39 msec). Data is read out via the "R" lines in the "two's complement convention". The time in nsec can be computed from the R line values with the formula:

$$\text{Time} = -2^{23}\cdot R_{24} + 2^{22}\cdot R_{23} + 2^{21}\cdot R_{22} + \ldots + 2^{1}\cdot R_{2} + 2^{0}\cdot R_{1} \text{ nsec.}$$

All INDIVIDUAL channels hit after the COMMON channel will give a positive time. Those hit before the COMMON will give a negative time.

Three conditions must be met in order to read a valid value for a particular channel:

1. The 4208 TDC must be in the Ready for Readout mode (EDW received, Sections 1.6 and 1.11).

2. The COMMON input must have been hit (threshold crossing while COMMON input is enabled).

3. The selected (subaddress) INDIVIDUAL input must have been hit (threshold crossing while INDIVIDUAL inputs are enabled).

If anyone of these three conditions is not met, the Q response to the CAMAC readout function will be 0 and all R lines will be left in the 0 state.

CAMAC Readout functions:

F(0)·A(i) reads channel (i + 1)

F(2)·A(i) reads channel (i + 1), F(2)·A(7)·S2 clears all data and logic; the LAM is not cleared.

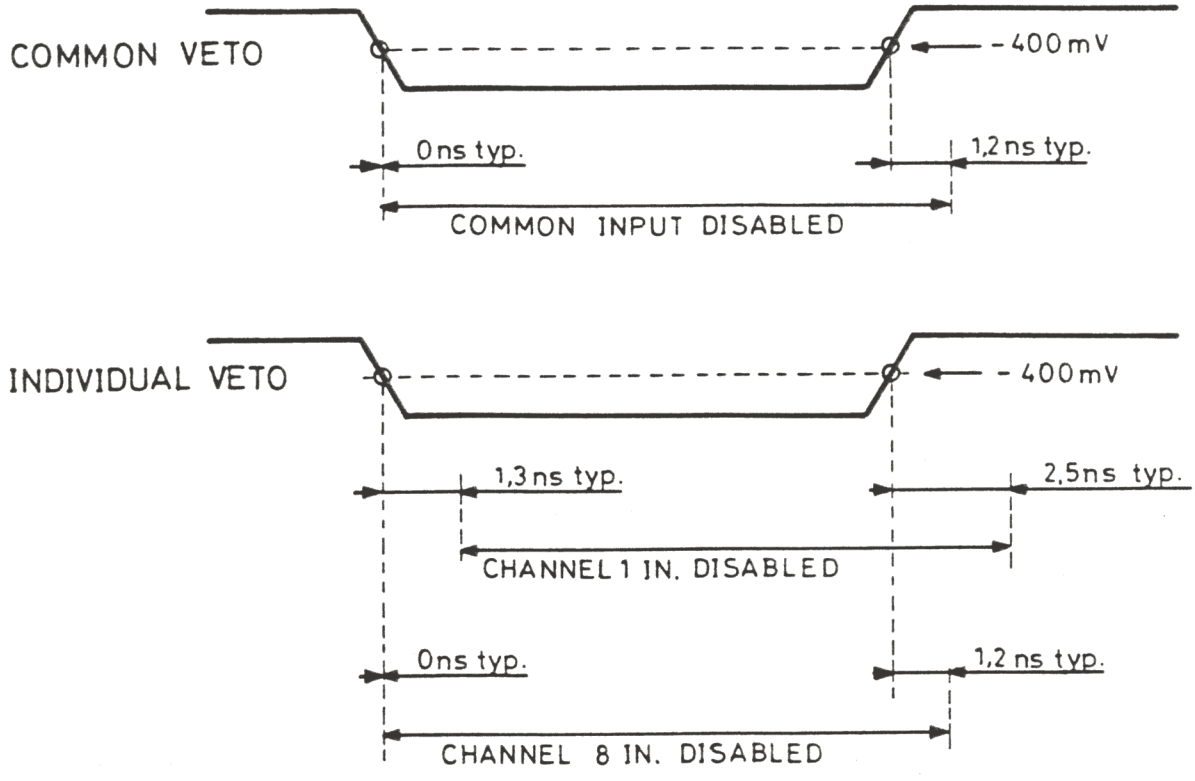
The F(0) function must be used for non-destructive readout of the 4208 TDC.

WARNING: As already mentioned above, CLR has an irreversible destructive effect on the data contained in the 4208 TDC.

1.14 Packaging and Power Requirements

The 4208 TDC is packaged in a standard #1 width CAMAC module. It dissipates a total of 29.6 Watts of power with the following current distribution:

1.5 A at +6 V; 3.3 A at -6 V;
17 mA at +24 V; 17 mA at -24 V.



Note: Time shifts between CH 8 and CH 1 is due to VETO signal propagation delays across the board. The Time shifts for channels 7 to 2 are linearly distributed between the values of channels 8 and 1.

VETO TIMINGS

Figure 1.1

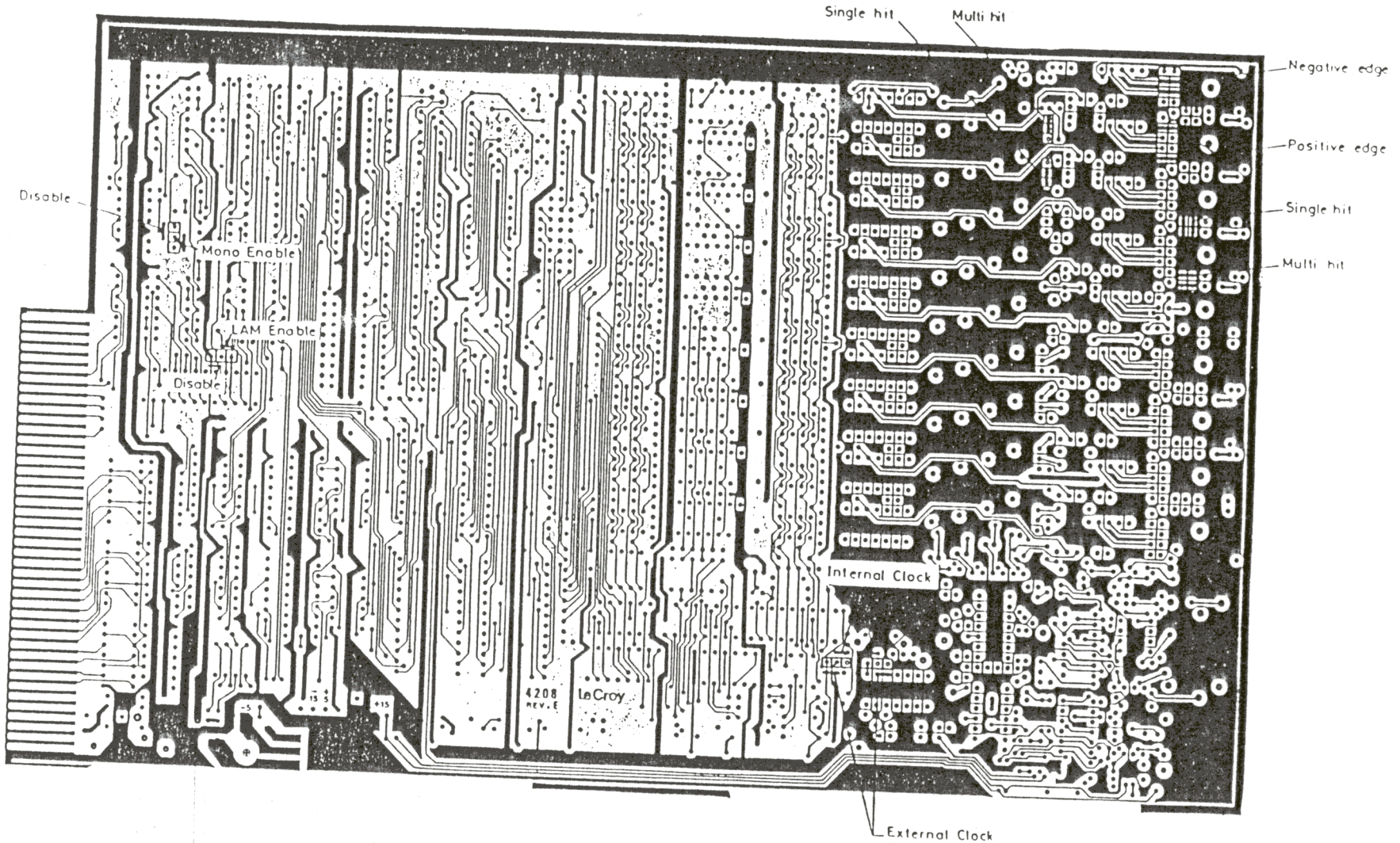


FIG 1-2 4208 JUMPER OPTIONS

ECO : 1006

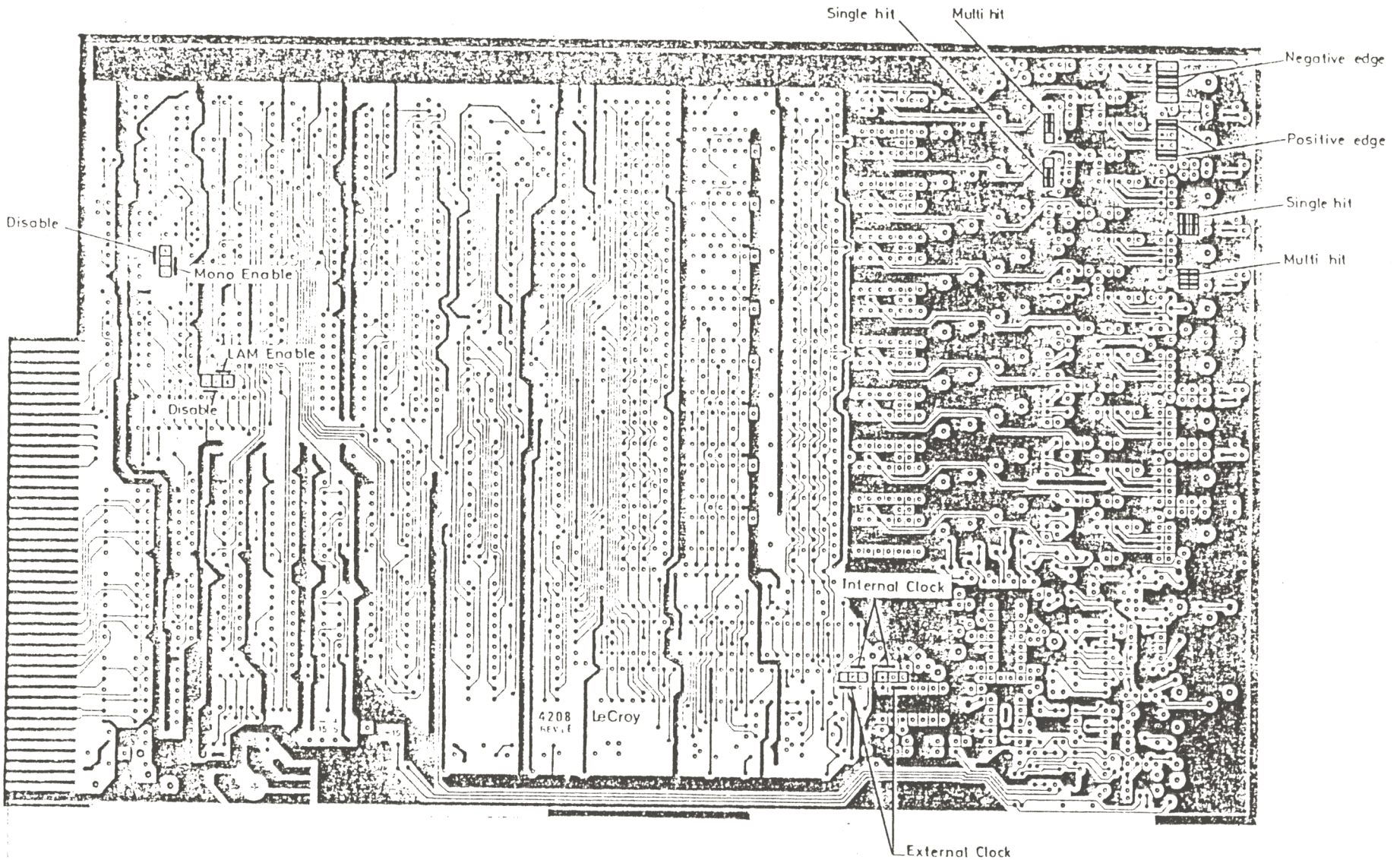


FIG 1-2 4208 JUMPER OPTIONS

ECO : 1006

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 General

The Model 4208 TDC consists of 9 independent, synchronously started, (stopped) time digitizers and associated circuitry. Referring to the 4208 block diagram (Figure 2.1), the circuitry is divided into 8 basic sections:

a. Input discriminators and hit registers
b. Digital interpolators
c. Real time counters
d. Time interval calculator
e. Clock and interpolator driver
f. Clear, Veto and BUSY circuits
g. Readout validation circuit
h. CAMAC control circuit

2.2 Input Discriminators and Hit Registers

Each of the 9 inputs (1 COMMON + 8 INDIVIDUAL) consists of an LD 601 hybrid discriminator circuit containing a fast input comparator C and a D flip-flop hit register HR.

Selection of negative versus positive edge sensing is accomplished by inverting the connections of the two inputs of the comparator (see Figure 1.2).

Selection of single versus multi-hit operation is accomplished by setting the s/m straps in the correct position (see Figure 2.1).

Each hit register HR, reset by CLEAR, is ready to be "set" by a clock pulse from the input comparator C, provided its D input is enabled. When HR is set to the "1" state, its Q output disables its clock input, and nothing but the CLR can reset it.

WARNING: Multi-Hit Mode is not available for ECO's #1001 and 1002.

2.3 Digital Interpolators

The 8 nsec clock period is divided into 8 steps to get the final 1 nsec resolution by feeding the digital interpolators (DI) with 4 clock signals delayed from each other by 1 nsec.

Looking at the different consecutive states of these 4 clock signals, one can see that the time function of the 4 signals follow a gray code rule, i.e., only one of the 4 signal changes its state at a time.

Each digital interpolator DI "latches" the state of the gray code when it receives a high to low transition from the hit register HR. The latched values are then converted to binary by the code converters CC to get the final 1 nsec resolution. This last operation is done at readout time.

2.4 Real Time Counters

The output of the digital interpolator feeds the input of the 4-bit ECL counter C_1 with a 125 MHz clock frequency. The MSB output of C_1 is converted to TTL, and feeds the input of the TTL 16 bit counter C_2. The counters C_2 of the 8 INDIVIDUAL channels consist of 4 LS 408 hybrids.

All 9 (1 COMMON + 8 INDIVIDUAL) real time counters start counting synchronously after the CLEAR and count the number of 8 nsec clock pulses until the occurrence of a hit on a given channel.

At the end of the conversion, the real time counter content represents the number of clock periods between the CLR and the hit on each channel, minus $N \cdot 2^{20}$, N being the number of overflows counted when the counter reaches full scale.

2.5 Time Interval Calculator

For each channel read, this circuit (A-B) computes the time difference between the INDIVIDUAL channel and the COMMON channel. This circuit consists of a 24-bit full adder (A-B) and an overflow discriminator (OVF CTR). The OVF CTR adds 0, 2^{23} or substracts 2^{23} whether there is 0, +1 or -1 overflow count difference between the COMMON and the INDIVIDUAL channel.

2.6 Clock and Interpolator Driver

A precision quartz crystal is used in conjunction with a fast ECL circuit (10216) to build a highly stable 125 MHz oscillator (see Appendix 3.2 for quartz crystal specifications).

The interpolator driver receives the 125 MHz signal and a set of $4 \cdot 50\ \Omega$ coaxial cables accurately delays signals to feed the DI bus. Symmetry and delay fine adjustment are implemented to improve the differential linearity of the digital interpolation. These adjustments are factory set and must not be modified without the appropriate differential linearity test equipment.

2.7 Clear, Veto, Busy Circuits

The clear flip-flop CS synchronizes the external or CAMAC clear pulses to the internal oscillator to insure that all real time counters start synchronously.

The external vetoes are "ORed" with an internal VETO signal which goes true when:

- CAMAC INHIBIT goes true
- or - Internal synchronous clear goes true
- or - EDW flip-flop output goes true (see Section 2.8).

Note that the IND signal has no effect on the INDIVIDUAL inputs when set to multi-hit mode (m). Therefore, the veto is active only for the first pulse of an input burst. Once the first pulse has occured (in multi-hit mode) subsequent pulses can set the HR register at any time. If this is undesirable, an external gate must be implemented between the source of the pulses and the input of the 4208 TDC.

The BUSY/$\overline{\text{BUSY}}$ output state is equal to the logical "OR" of all 9 hit registers HR. The BUSY goes true at the time of the first hit and is reset by the next clear.

2.8 Readout Validation Circuit

When a readout function is performed, F(0) or F(2) for any subaddress, the circuit VAL.CTR checks that the following three conditions are met:

a. The EF flip-flop must be ON (must have received an EDW signal or an end signal from the internal timer).
b. The COMMON HR register must be ON (COMMON stopped).
c. The addressed HR register must be ON (addressed channel stopped).

If one or more of the 3 above conditions is not met, the valid signal VD stays low thus vetoeing the output driver RD DRV and the Q response for the readout function. This results in Q = 0 and R data = 0 for the readout function.

2.9 CAMAC Control Circuit

The CAMAC control circuits consist of a CAMAC function decoder (CAM.FNC.DEC) and address selector. The former is a programmable logic array (MMI PAL) that fully decodes the N, A, F CAMAC functions and generates all appropriate internal signals. The X and Q responses are also issued by this device.

The READ ENABLE signal enables the address selector which, in turn, decodes the subaddress and selects the appropriate channel of the 4208 TDC.

See data sheet for additional information.

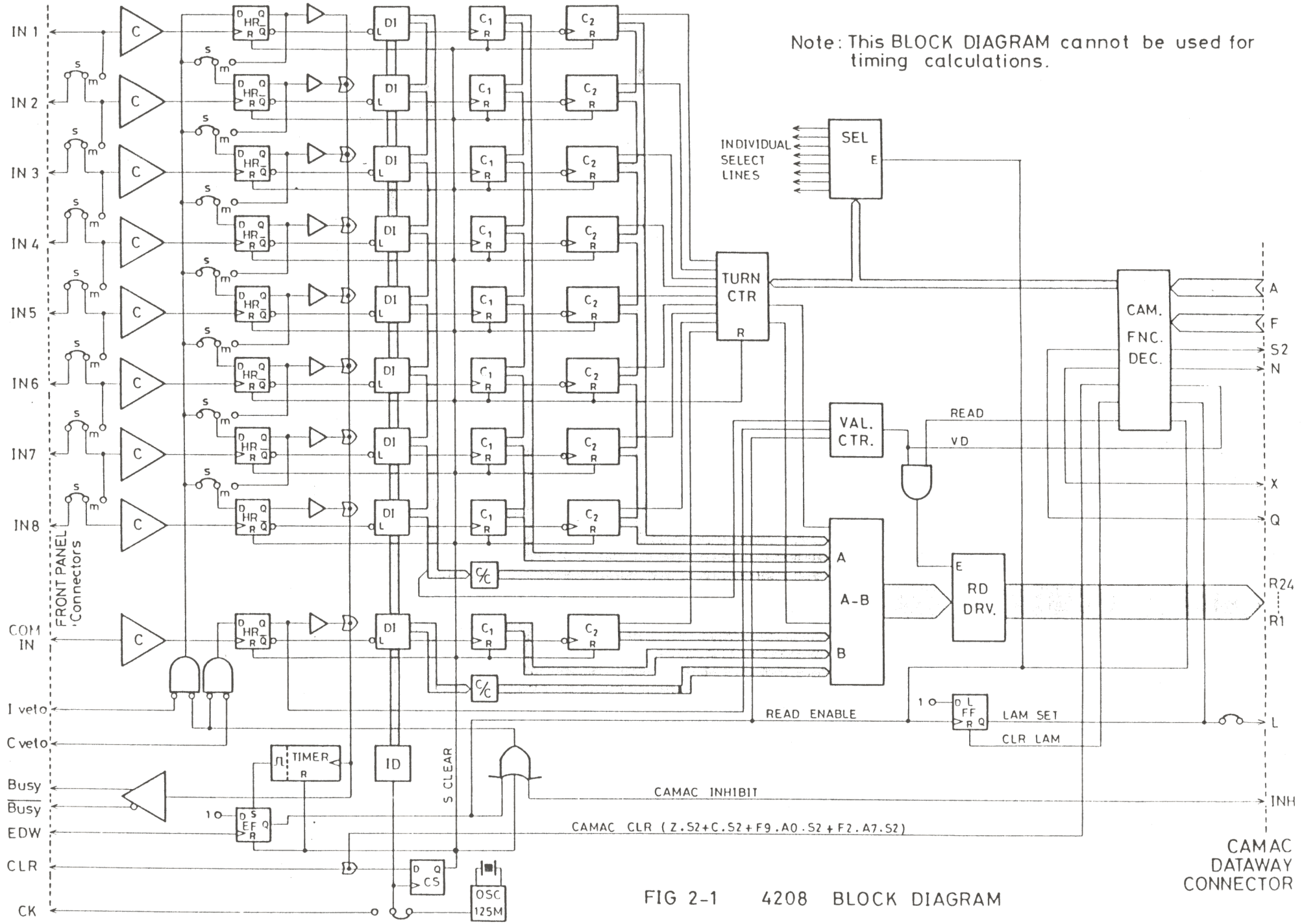


FIG 2-1 4208 BLOCK DIAGRAM