MODEL 3420
CONSTANT FRACTION
DISCRIMINATOR

LeCroy

Innovators in Instrumentation

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CAUTION

COOLING

The high power dissipation of the 3420 requires that it be well cooled. Be sure the fans move sufficient air to maintain the exhaust air temperature at less than 50° C.

6 V POWER REQUIREMENT

The 3420 uses significant power from the -6 V and +6 V CAMAC power bus. Be sure that your crate can supply enough current to this and other modules, especially if multiple 3420s are being used.

INSTALLATION

CAMAC crate power should be turned off during insertion or removal of modules to avoid possible damage due to momentary misalignment of contacts.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

TABLE OF CONTENTS

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the LeCroy Model 3420 Fraction Discriminator. In addition, it describes the interface's theory of operation and presents information regarding its function and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier and filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only. In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide an extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for details.

**DOCUMENTATION
DISCREPANCIES**

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

**SOFTWARE LICENSING
AGREEMENT**

Software products are licensed for a single machine. Under this license you may:

■ Copy the software for backup or modification purposes in support of your use of the software on a single machine.

■ Modify the software and/or merge it into another program for your use on a single machine.

■ Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

SERVICE PROCEDURE

Products requiring maintenance should be returned to the Customer Service Department. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department.

PRODUCT DESCRIPTION

OVERVIEW

The LeCroy Model 3420* is a 16-input Constant Fraction Discriminator in a single-width CAMAC module. Constant Fraction Discriminators (CFDs) use a constant fraction (or percentage) of the input pulse to precisely determine the timing of the output pulse leading edge relative to the input signal. This technique is not subject to jitter ("time walk") caused by varying amplitudes of the inputs, such as in leading edge discriminators. This method of discrimination is indispensable in critical sub-nanosecond timing or trigger systems.

This module is part of the LeCroy family of ECLine programmable logic modules. Each channel has its own programmable threshold. Common to all channels is a programmable output width and a dead time control. A programmable mask and test pulse allow computerized system testing and simulation.

The Model 3420 has the unique feature of also providing charge outputs along with the differential ECL logic outputs. The charge outputs become a flexible time-to-digital converter when used with a charge sensitive ADC such as the LeCroy Model 4300B.

SPECIFICATIONS

Input Characteristics

Signal Inputs: 16 inputs via a front-panel 34-pin connector, 100 Ω $\pm5\%$ (50 Ω optional), AC-coupled (750 nsec time constant). Protected to 1 A for 1 μsec; clamping at +1 V and -6 V.

Threshold: Individually adjustable, -20 mV to -1.4 V set by an 8-bit DAC (5.5 mV steps) programmed via CAMAC. Stability better than ±100 ppm/$°$C to 70$°$C operating temperature.

Test Input: One front panel Lemo connector terminated in 50 Ω; drives all channels with a > 800 mV, 20 nsec with a minimum duration of 100 nsec. Requires NIM level signal (-600 mV minimum). Minimum width, 100 nsec. Maximum rate, 1 MHz.

Veto Input: One front panel Lemo connector terminated in 50 Ω. Common to all channels. Allows fast inhibiting of outputs (inhibits only the overlap of the veto and output). Used in the time-to-charge mode.

Output Characteristics

Discriminator Outputs: 16 outputs on one 34-pin, front panel connector; ECL differential level (-0.8, -1.6 V) into 100 Ω twisted pair. Duration: 25 nsec to 250 nsec programmable in 16 nsec steps via CAMAC, common to all channels.

Charge Outputs: 16 outputs on one 34-pin, front panel connector (ground, signal). Negative, current sink outputs suitable for use with charge sensitive ADCs. Duration same as discriminator outputs. Programmable from 1 - 10 mA.

Current Sum Output: One, front panel Lemo connector; 1 mA per triggered channel for duration of discriminator outputs.

Designed by Michigan State University.

OR Output: One front panel output provided both as a NIM signal via a Lemo connector and as an ECL differential level (-0.8, -1.6 V) via a 2-pin connector. Duration equal to discriminator output.

Timing Characteristics

Walk: < ±200 psec from 100 mV to 5 V (with a pulse of 20 nsec width, rise and fall times of 5 nsec, constant fraction delay of 10 nsec and constant fraction set to 30%).

GENERAL

Output Width and Dead Time Adjustments: Both the output width and dead time are programmable via CAMAC in the 3420. The preset ranges are 25 nsec to 250 nsec. The output width adjustment determines the width of both the discriminator output and the time-to-charge output. The output width has not been trimmed and can vary ±50%. It must be re-standardized with another logic module if it is to be used as a gate or for overlap coincidence. The dead time adjustment sets a time interval (starting at the same time as the discriminator output) which inhibits the discriminator from triggering again. The dead time MUST always be set as long or longer than the discriminator output. This protects against multiple pulsing.

Maximum Rate: 40 MHz at lowest settings for dead time and output pulse width.

Double Pulse Resolution (DPR): 25 nsec minimum. Depends on dead time setting.

Input to Output Delay: 15 nsec + constant fraction delay. Delay matched to better than 2 nsec.

Test to Output Delay: 30 nsec.

Multiple Pulsing: None; one and only one output pulse is produced regardless of input pulse amplitude so long as the dead time setting is greater than the programmed pulse width.

Cross Talk: <5% with proper cabling and termination.

Built-in Time-to-Charge Converter (TQC): A common 8-bit DAC sets the TQC outputs from 0 to 10 mA. An internal jumper allows switching to a NIM signal (-16 mA). The output is a current sink output, clamped at -1 V, that can only drive a properly terminated cable. It is meant to be used by charge integrating ADCs such as the LeCroy Model 4300B (FERA). Maximum timing resolution is 25 psec with an internal jitter of approximately 10 psec. When used in this mode, the ADC gate must encompass the leading edge of the TQC pulse and terminate before the trailing edge of the TQC pulse. If this is not convenient, the veto input can be used to terminate the TQC pulse before it terminates because of the width setting. The ADC gate can then be set arbitrarily wide to encompass the whole pulse.

TQC Linearity: < 200 psec deviation from a straight line fit.

Constant Fraction and Delay Alteration: Can be altered on a channel-to-channel basis by changing the resistors mounted on an internal DIP adapter and by changing the delay via a 5 tap internal delay line.

Factory set fraction = 30%; delay = 10 nsec max., five 2 nsec taps.

Packaging: RF-shielded, CAMAC #1 module.

Power Requirements: +6 V at 1.00 A; -6 V at 1.75 A; +24 V at .05 A and -24 V at .25 A.

Weight: 1.6 lbs (0.7 kg).

CAMAC COMMANDS

The commands for the 3420 conform to the CAMAC Standard-IEEE Std 583-1975. If the user is unfamiliar with the CAMAC standard, a good reference is *"CAMAC Instrumentation and Interface Standards"*, published by The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017.

Further information is available from LeCroy Research Systems in the form of Application Notes. In particular, AN-33, *"Introduction to CAMAC"*, is very useful.

F(0)•A(0-15):   Reads channel Threshold on CAMAC R1 - R8.

F(1)•A(0):   Reads Mask register on CAMAC R1 - R16.

F(1)•A(1):   Reads Dead Time register on CAMAC R1 - R4 and Width register on CAMAC R5 - R8.

F(1)•A(2):   Reads Time-to-Charge register on CAMAC R1 - R8.

F(16)•A(0-15):   Writes channel Threshold on CAMAC W1 - W8 (-20 mV to -1.4 V, 5.5 mV increments).

F(17)•A(0):   Writes to Mask register on CAMAC W1 - W16.

F(17)•A(1):   Writes to Dead Time register on CAMAC W1 - W4 and Width register on CAMAC W5 - W8 (25 - 250 nsec, 16 nsec increments; 0000=25 nsec, 1111=250 nsec).

F(17)•A(2):   Writes to Time-to-Charge register on CAMAC W1 - W8 (0 to 10 mA, 40 μA increments).

F(25)•A(0):   Triggers Test function.

CAMAC Responses

X: An X response is generated for every valid F, N, A.

Q: A Q response is generated for every valid F, N, A.

Z: Clears mask register at S2 time.

INSTALLATION

The 3420 is a CAMAC module and as such must be installed in a CAMAC crate. Care must be taken to ensure the crate power is off before the module is installed. It can be installed in any slot except in the crate controller position (slots 24 and 25).

The 3420 does not draw an excessive amount of power. A 1000 Watt crate such as the LeCroy Model 8025, easily powers a full crate of 3420 modules. However, the user should always check the power capacity of his crate against the power required by the installed modules.

It is best, although not necessary, to adjust the Constant Fraction and Delay setting before installing the module. If the discriminator outputs are not used, jumper J2 must be moved toward the rear of the module to provide a load on the ECL outputs. Unloaded ECL outputs have a subtle effect on the TQC. The TQC output can be changed to a NIM signal by moving jumper J1 toward the top of the module. See Operating Instructions for more details.

The 3420 comes with 50 Ω input impedance and AC coupling. This can be modified to 100 Ω input impedance. See Additional Information for more details.

CAUTION: Once the unit is installed in the crate and powered up, it must be programed because the internal registers can power up loaded with random values. For test purposes, it is best to set all Thresholds to 40 mV, Mask to all zeros, Dead Time and Width to 250 nsec and TQC to 10 mA.

To complete the installation, cables need to be connected to the inputs and outputs. The discriminator outputs are ECL so that standard flat, twisted pair cable can be used. The inputs and TQC outputs are analog and consideration should be given to using miniature shielded cable rather than unshielded cable if maximum performance is desired.

OPERATING INSTRUCTIONS

GENERAL

Setup of the Model 3420 can be split into three different categories. The first is to select the hardware configuration for the constant fraction and delay, and position the jumpers for the desired type of operation. This is done with the side cover off. The second is to load the internal registers with the necessary values to obtain the desired performance. The last is to setup up the TQC timing and use the test input.

Selecting the Fraction

The fraction (f) is selected by changing resistors in the Fraction DIP Adapter (see Figure 1). The value can be set from f=0 to f=1 and normally comes from the factory with f=0.3. The fraction selected depends on the application and typically f=0.3 for plastic scintillators and surface barrier silicon detectors while f=0.1 for slower inorganic scintillators such as Na(T).

Implementing the Fraction

Each channel has a 6-pin DIP adapter containing 2 resistors that determine the fraction and one resistor for the delay line termination. Please refer to the accompanying diagram. The relationship of the resistors is as follows:
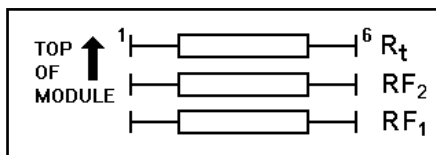

$Rf_1 + Rf_2 = 300 \ \Omega$
$Rf_2 = (1 - f) \cdot 300 \ \Omega$
$Rf_1 = f \cdot 300 \ \Omega$
$f = \text{fraction} = Rf_1/(Rf_1 + Rf_2)$
Termination resistor $Rt = 100 \ \Omega$

Figure 1: Fraction DIP adapter.

Selecting the Delay

A socket mounted tapped delay line is available on each discriminator channel for selecting the appropriate delay to determining the constant fraction. There are 5 equal taps on each delay line with a jumper for selecting the desired tap. The "n" in the model number "3420/n" gives the total delay of the factory supplied delay line. Figure 2 shows the arrangement of the taps on the circuit board along with the formula for selecting the correct delay.
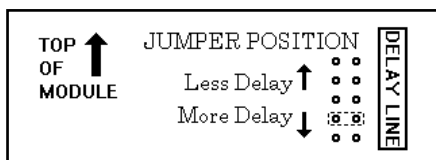
Assuming the following:
t_{rise} = rise time of pulse
f = fraction
t_d = desired delay
Then: $t_d = (1 - f) \ t_{rise}$

Figure 2: Delay Line Tap Layout.

A complete description of how the constant fraction works is discussed in Theory of Operation.

Other Jumper Configurations

There are two other jumpers on the printed circuit board, J1 and J2. J1, located ≈ 2" back from the front panel in the center of the board, determines whether the TQC outputs will be a standard NIM output or an output whose current is controlled by the Time-to-Charge register. Positioning J1 toward the top of the module makes the TQC outputs NIM. J2, located between the two top front panel connectors, creates a load for the discriminator outputs if they are NOT being used. This is necessary for proper operation of the TQC outputs. Position J2 toward the rear

of the module when the discriminator outputs are NOT connected to another module.

Threshold

The internal threshold registers of the 3420 MUST be programmed upon powering up the module. This is accomplished with a CAMAC F(16)•A(i) where i = channel number. The thresholds are programmable from 0 V to -1.4 V in 5.5 mV increments. If the thresholds are set too sensitive, the outputs will oscillate and cause problems. Under ideal conditions, the thresholds can be set to -22 mV and operate satisfactorily. However, input noise, shielding and signal rise time will effect this, so great care should be taken to minimize these effects for best results. The user is encouraged to read the Theory of Operation section of this manual, so that he can fully appreciate the way the threshold works.

Dead Time and Width

The Dead Time & Width register MUST be programmed upon power up. A CAMAC F(17)•A(1) will accomplish this with the bottom 4 bits setting the Dead Time and the upper 4 bits setting the width. All bits = off gives a 25 nsec setting and all bits = on gives a 250 nsec setting with incremental settings of 16 nsec. Satisfactory operation will not occur unless the Dead Time is made ≥ the Width. The Width setting is determined either by the width required by the down stream modules using the discriminator outputs or by the TQC (see following description of Charge Outputs). It is best to re-standardize any outputs (with another logic module) that will be used as a gate or in overlap coincidence because they are not meant for that purpose.

TQC Setup

The TQC (Charge-to-Time Converter) uses the Charge outputs, digitized by a charge ADC such as a FERA, to generate a digital number proportional to the time between when the constant fraction crossing occurred and a reference signal that occurs AFTER the crossing. This reference signal can either be the leading edge of the veto input to the 3420 or the trailing edge of the gate to the charge ADC. The leading edge of the ADC gate MUST encompass the constant fraction crossing under all conditions. It is important that the Width be LARGER than the maximum time that can occur between the constant fraction crossing and the reference signal and if the veto is used, the veto be wide enough to exclude any portion of the Charge output that might be included in the ADC gate, or this approach will not work. Refer to the following timing diagram for more detail:
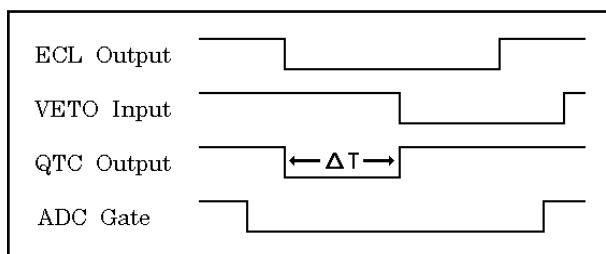

Figure 3: Charge-to-Time Converter Timing Diagram.

Once the correct timing relationships have been established, the current available on the Charge outputs can be adjusted with a CAMAC F(16)•A(2). The output range is 0 to 10 mA in 40 μA increments (8 bit). This allows the user to finely adjust the charge to the ADC as can be seen in the following relationship.

Given: Δt from Figure 3.
          I_{TQC} = current at charge outputs
          Q_{out} = charge converted by ADC

Then: $Q_{out} = I_{TQC} \cdot \Delta t$

Note: By adding an appropriate amount of delay (20 nsec or more depending on the ADC used) to the QTC output, the OR output and/or the Multiplicity output can be used to gate the ADC.

Test Input

A NIM pulse directed to the Test Input will generate an internal input pulse of > 800 mV amplitude and $\approx$ 125 nsec duration (equal to the test input width when >125 nsec wide). A CAMAC F(25)•A(0) will also generate the same internal test pulse. This allows the user to test all the channels and by setting the Mask (see following description), send test patterns to down stream modules such as the ECLine family produced by LeCroy.

Mask

The Mask register will be loaded with an arbitrary value on powering up the 3420. This is corrected with a CAMAC F(17)•A(0) which writes a 16 bit word, one bit for each channel (LSB = channel 0), with a "1" masking the channel and a "0" unmasking it. The Mask is retained until changed by user.

Figure 4 shows a simplified block diagram illustrating the input section of one 3420 channel. The incoming signal is split three ways after passing through a limiting circuit and an AC-coupling capacitor. (The test input is ORed into the circuit at this point.) One path is to a comparator that drives the D input of the flip-flop in the AD891 that provides the output of the channel. The other side of this comparator is the Threshold DAC. The other two paths consist of the fraction input which is attenuated by the combination of R1 and R2 and the delayed input that is selected from a tap on the delay line. Both these inputs to the clocking comparator are quiescently at 0 V. The attenuated input goes negative first followed by the delayed input. At their crossing, which comprises the Constant Fraction, the D input (threshold comparison) must be true for an output to occur. It is important that the delay and fraction be matched for proper operation of the circuit, for example:

$$t_{delay} = (1 - fraction) \cdot t_{rise}$$

Too short a delay will require an excessively high threshold.

Figure 5 illustrates the waveforms presented to and generated by the AD891.

Note that the internally generated Dead Time signal (set by the Dead Time DAC) disables the operation of the flip-flops, thus preventing more than one output occurring during its duration. This is a desirable feature
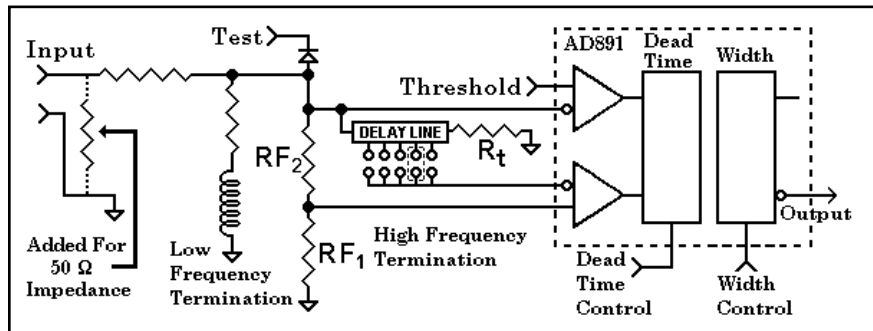

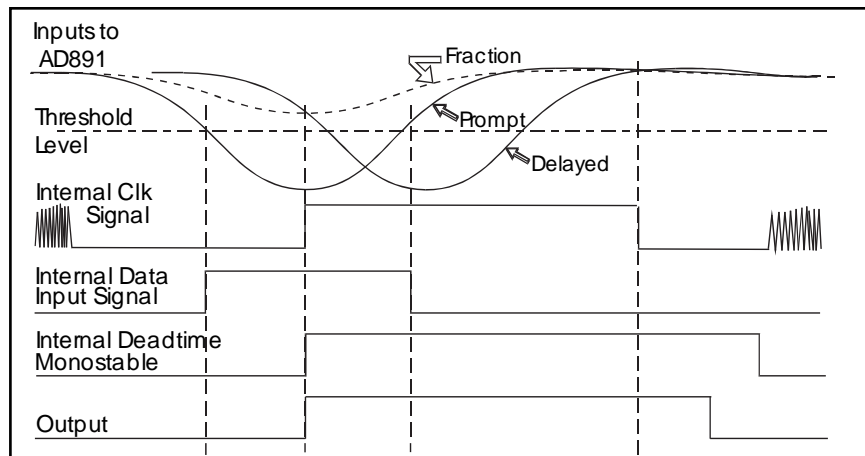Figure 4: Constant Fraction Input Section, One Channel

Figure 5: AD 891 Waveforms

when dealing with slow, noisy signals such as encountered from NaI(Tl) scintillators. This also means that the Dead Time MUST be set $\geq$ the Output Width (set by the Width DAC) or unpredictable outputs can occur.

AD891 Waveforms

Figure 6 shows a simplified block diagram of the output section of one 3420 channel. The output of the AD891, which now determines the width of the output pulse, goes through a three input NAND gate. The other two inputs to this gate, Veto and Mask, are used to control the channel output. The output of the NAND gate drives the module output OR circuit, the ECL output drivers and the TQC circuit. The NOR gate driving the TQC circuit also provides a drive to the summing circuit which generates 1 mA per channel at the Multiplicity summation output. The waveforms in Figure 7 illustrate the operation of this output.
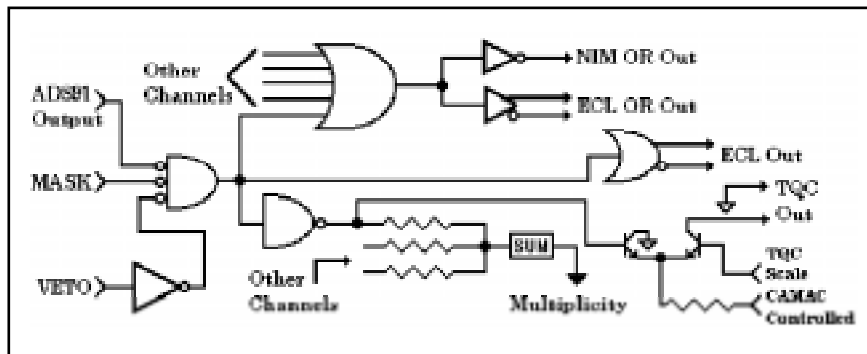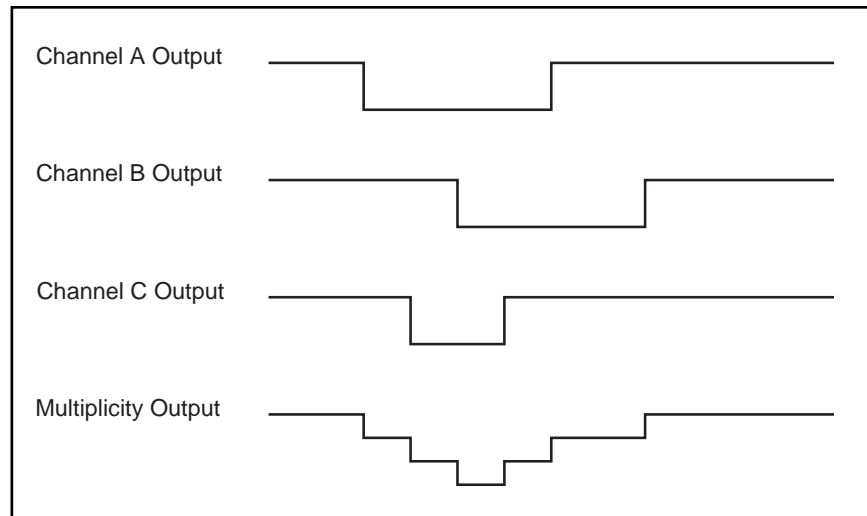

Figure 6: Constant Fraction Output Section One Channel

Figure 7: Multiplicity Waveforms

USER MODIFICATIONS

Depending on the application, the user may find it necessary to modify the Model 3420. There are four simple modifications available; changing the input impedance to 100 Ω, replacing the fraction DIP adapters, replacing the delay elements and providing NIM outputs.

INPUT IMPEDANCE

The 3420 comes from the factory with 50 Ω input impedance for the greatest noise immunity. However, the user may elect to use twisted-pair cable which has 100 Ω impedance, is low cost and easily assembled. The user must then remove two 10 pin, SIP, 100 Ω bussed resistor networks at R13 and R21 to change the input impedance to 100 Ω thereby matching the cable. The SIPS are in sockets located in the upper right hand corner of the circuit board when viewed from the component side with the front panel toward the right.

FRACTION

Each channel has its own 6 pin socketed DIP adapter which carries the terminating resistor for the delay element and the two resistors that determine the fraction. Figure 8 shows the relationship of these resistors and a diagram of the adapter.
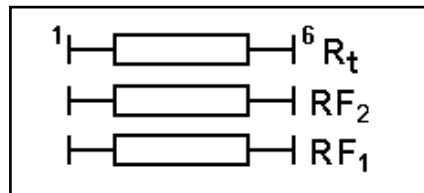
$Rf_1 + Rf_2 = 300 \ \Omega$
$Rf_2 = (1 - f) \cdot 300 \ \Omega$
$Rf_1 = f \cdot 300 \ \Omega$
$f = $ fraction
Termination resistor $Rt = 100 \ \Omega$

Figure 8: Resistor Adapter

These adapters are easily located on the PC board because their part identification printed on the board begins with P. When viewed from the component side with the front panel to the right, the resistor arrangement on the adapter corresponds to the diagram above. The standard configuration shipped from the factory is $Rf_2 = 200 \ \Omega$, $Rf_1 = 100 \ \Omega$ and $Rt = 100 \ \Omega$ which makes $f = 1/3$.

DELAY ELEMENT

The delay element is a socket mounted 7 pin SIP with 5 equally spaced delay taps which is available with a total delay of 5, 10, 20, 30, 40, 50, 60, 75 or 100 nsec. It is available from LeCroy Research Systems or Data Delay Devices, Inc., 3 Mt. Prospect Ave., Clifton, NJ 07013, (201) 773-2299, Fax (201) 773-9672. When ordering from Data Delay Devices, specify their part number 1505-xB where x equals the total delay in nsec as stated previously. The necessary delay is easily calculated by using the following relationship:

$$t_{delay} = (1 - fraction) \cdot t_{rise}$$

NIM OUTPUTS

The TQC outputs can be easily configured to provide standard NIM outputs. Jumper J1, which is located ≈ 2" back from the front panel in the center of the board, provides this function. When position toward the top of the module, the outputs are NIM. When positioned toward the bottom of the module, the outputs are TQC. Note: if the ECL outputs are not used, J2, which is located between the two top front panel connectors, must be positioned toward the rear of the module creating a load for the ECL outputs. If the ECL outputs are to connect to another module, then J2 must be positioned toward the front of the module. Unloaded ECL outputs have a subtle effect on the TQC outputs.

INDEX