3420 CONSTANT FRACTION DISCRIMINATOR *Designed by Michigan State University.

(http://www.lecroy.com/lrs/dsheets/3420.htm)

- Works as a Constant Fraction or Zero Crossing Discriminator
- 16 Inputs Per Module
- Low Time Walk: 200 psec (at 100:1 Dynamic Range)
- Individually Programmable Thresholds
- Programmable Dead Time and Output Widths
- ECLine Compatible
- CAMAC Packaging
- Built-in Time-to-Charge Converter

GENERATION OF PRECISE LOGIC PULSES FOR CRITICAL TIMING APPLICATIONS

Discriminators generate precise logic pulses in response to input signals exceeding a given threshold. Constant Fraction Discriminators (CFDs) use a constant fraction (or percentage) of the input pulse to precisely determine the timing of the output pulse relative to the input signal. This technique is not subject to jitter ("time walk") caused by varying amplitudes or rise times of the inputs, such as in leading edge discriminators. Output pulses are of standard amplitude and of preset duration. CFDs are the units of choice for use with critical subnanosecond timing or trigger systems.

The Model 3420* is part of the LeCroy family of ECLine programmable logic modules. It has two modes of operation. The first and foremost mode is as a Constant Fraction Discriminator, which results in best timing precision. The other mode is as a zero crossing discriminator. The unit offers many benefits including external control of the output pulse width, the 16 individual thresholds, as well as having built-in test features.

The module features a time-to-charge converter that allows the user to perform precise time measurements in conjunction with a charge sensitive ADC such as the LeCroy 4300B or similar ADC.

FUNCTIONAL DESCRIPTION

General

The LeCroy Model 3420, Constant Fraction Discriminator, is the next step in CAMAC-ECL discriminators. It offers excellent timing accuracy, adjustable analog delay, adjustable fraction, adjustable dead time, adjustable output pulse width, and a wide range of programmable thresholds for each channel. It was designed to be a versatile yet flexible module for applications where precise timing is critical.

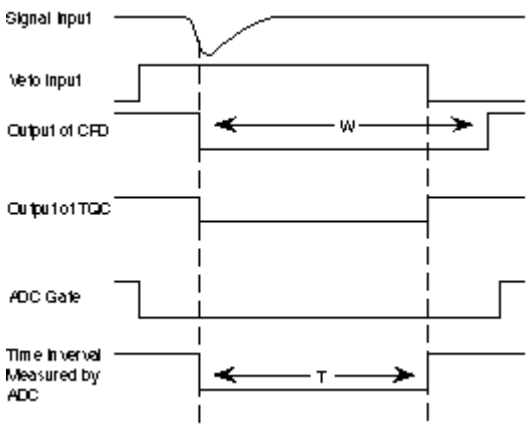
The 3420 offers 2 modes of operation, constant fraction discrimination and zero crossing. In addition, it offers simultaneous time-to-charge conversion.

Threshold and Width

In the constant fraction mode, the 3420 offers a programmable threshold range from -20 mV to -1.4 V for each of its 16 inputs via CAMAC. All outputs have a width which is programmable from 25 nsec to 250nsec in 16 nsec steps via CAMAC. Thresholds on each channel and the global dead time and output width values can be read back from CAMAC. Timing jitter on the output is less than 200 psec over a dynamic input signal range of 100:1. This unit has differential ECL logic outputs (which offer noise immunity) and is compatible with LeCroy's ECLine family of CAMAC modules.

Model 3420 timing diagram when used as a time digitizer together with an ADC. The time digitized by the ADC is "T". For correct operation as a time digitizer, the output pulse width "W" must be set to

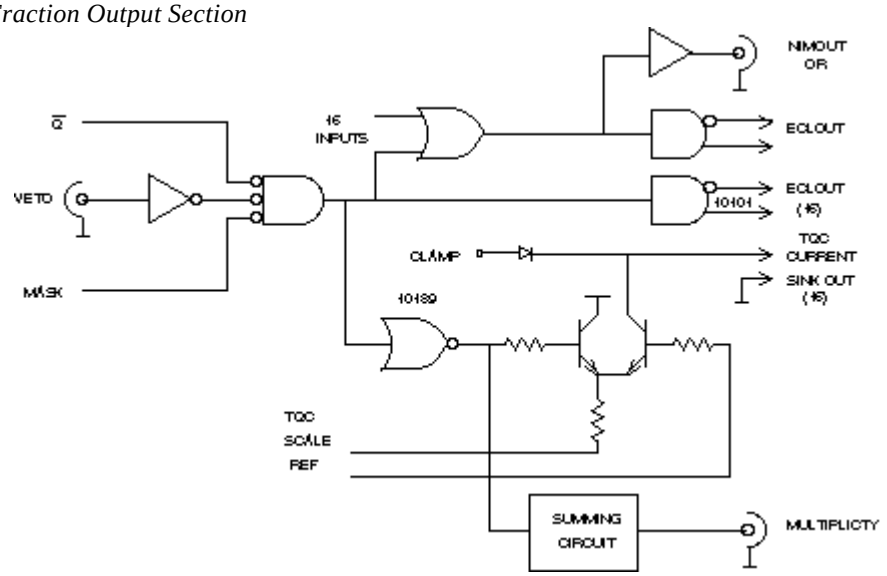
exceed the duration of the Veto signal; also, the Veto signal must be applied prior to the arrival of the input signal.



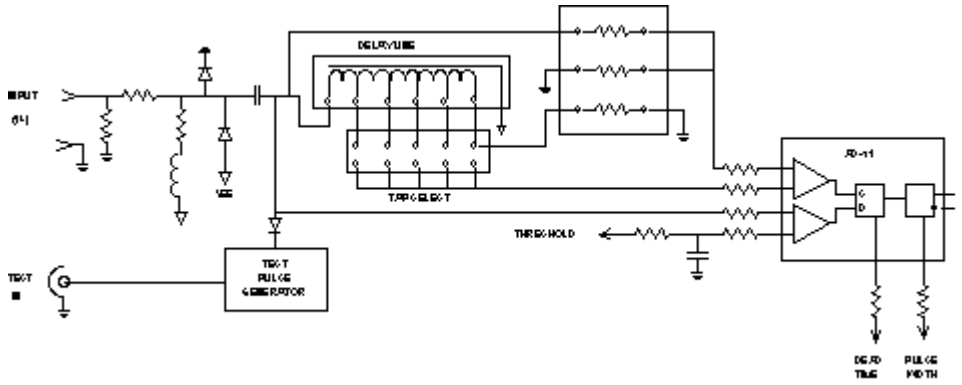
Delay and Fraction

The module uses plug-in headers to determine the fraction of the input pulse used for best timing. By changing the headers, the 3420 fraction can be altered or it can be converted into a leading edge or zero-crossing discrimi nator.

Constant Fraction Output Section



Constant Fraction Input Section, One Channel



Masking

For additional system flexibility, input masking is made possible by simultaneously inhibiting any combination of the 16 inputs via CAMAC command. This feature allows the user to generate or simulate any desired trigger configuration. It also allows complete point-to-point checks of the system electronics without requiring removal of wires or disassembly of the data acquisition system.

Test Feature

A built-in test feature simulates an input signal for each channel upon receipt of either an F(25) command or a NIM level signal applied to the test input connector. This permits rapid, simultaneous testing of all enabled dis criminator channels.

Current Sum

A current sum is also provided which generates -1 mA per enabled input channel to a front-panel Lemo connector output. This output can be used to conveniently monitor discriminator activity or to act as a source for prompt trigger information.

Digitizing Time Intervals

The built-in time-to-charge converter (TQC) converts a time interval into a charge. This feature is used with integrating ADCs such as the LeCroy 4300B FERA ADC to provide time measurements with 25 psec resolution with a < 200 psec integral linearity. The time interval measured is the time from the leading edge of the signal input to either the leading edge of the 3420 VETO, acting as a Common Stop (as shown in the timing diagram) or the trailing edge of the 4300B GATE input. Thus, the combination of the TQC with an ADC acts like a Common Stop TDC. By incorporating the TQC into the discriminator module, the Model 3420 can replace both, a discrimi nator and a separate time-to-charge converter (such as the LeCroy 4303) in most applications, saving cost and CAMAC slots.

SPECIFICATIONS

INPUT

Signal Inputs: Sixteen inputs via 2-pin front-panel connectors, 100 ohm, ±2%, 50 ohm optional. Protected to 1 A for 1 µsec; clamping at +1 V and -6 V. Reflections < 5% for input pulses of 5 nsec rise time; input offset voltage typically ±1 mV.

Test Input: One Lemo connector on front panel, 50 ohm; triggers all enabled channels. Requires NIM level signal (-600 mV minimum). Minimum width, 100 nsec. Maximum rate, 1 MHz.

Veto-Input: One Lemo front-panel connector, 50 ohm. Permits simultaneous fast inhibiting of all channels. Requires NIM level signals. Minimum duration, 20 nsec. This input is used to work the module in the time-to -charge mode only. Signal must overlap output pulse.

OUTPUT

Discriminator Outputs: 16 outputs, ECL level (-0.8 V to -1.7 V) into 100 ohm twisted-pair. Duration for all channels, approximately from 25 nsec to 250 nsec ±50% programmable in 16 steps via CAMAC; 0.2%/°C maxi mum.

Current Sum Output: One, front-panel Lemo connector; 1 mA per fired channel.

OR: One front-panel lemo for NIM level output and one ECL level output on front panel 2-pin header. The output is an OR of 16 input channels which exceed the set threshold.

Time-to-Charge: 16 outputs, 0 -10 µA programmable in 40 µA steps. Suitable for use with LeCroy Model 4300B FERA.

GENERAL

Output Width and Dead Time Adjustments: The unit has an internally generated programmable dead time followed by an output pulse width. Each one of these times must be set via CAMAC. The preset ranges are 20 nsec to 250 nsec. Different choices are possible by user modification (10 nsec to 100 nsec and 50 nsec to 500 nsec).

Operating Modes: Constant fraction discriminator or zero-crossing discriminator, both followed by built-in time -to-charge converter (TQC).

Maximum Rate: 50 MHz at lowest settings for dead time and output pulse width.

Double Pulse Resolution (DPR): 20 nsec, typical.

Input-Output Delay: 15 nsec + constant fraction delay. Delay matching better than 2 nsec.

Test-Output Delay: 30 nsec + constant fraction delay.

Multiple Pulsing: None; one and only one output pulse is produced for each input pulse regardless of input pulse amplitude or duration.

Threshold: -20 mV to -1.4 V ±5% through 8-bit DAC via CAMAC. Stability better than ±100 ppm/°C to 70°C operating temperature. Individually programmable per channel in 5.5 mV steps.

Cross Talk: < 5% with proper cabling & termination.

Walk: < ±200 psec from 100 mV to 5 V (with a pulse of 20 nsec width, rise and fall times of 5 nsec, constant fraction delay of 10 nsec and constant fraction set to 30%).

Built-in Time-to-Charge Converter (TQC): 0 to 10 mA output, programmable in 40 µA steps. Output is a current sink output. It will therefore, drive only properly terminated cable. The output is clamped at -1 V. It can be switched to provide fast NIM signals (-16 mA) by moving an internal jumper. Maximum timing resolution is 25 psec with an internal jitter of approximately 10 psec. When using this mode, the output pulse width must be set to a time greater than the width of the ADC gate pulse. To ensure accurate results a veto pulse should be used to inhibit inputs to the CFD when the ADC is not gated (armed).

TQC Linearity: < 200 psec deviation from a straight line fit.

Constant Fraction and Delay Alteration: Can be altered on a channel-to-channel basis by changing the internal plug-in header and by changing the delay via a 5 tap internal delay line. Factory set fraction = 0.3; delay = 10 nsec, five 2 nsec taps.

Packaging: RF-shielded, CAMAC #1 module.

Power Requirements: +6 V at 1.00 A; -6 V at 1.75 A; +24 V at .05 A; and -24 V at .25 A.

Weight: 1.6 lbs (0.7 kg).

CAMAC COMMANDS

CAMAC COMMANDS

X: An X response is generated when a valid N, A, F command is recognized.

Q: A Q response is generated only if the requested function can be executed.

Z: Clears mask register at S2 time.

CAMAC FUNCTION CODES

F(0)·A(0-15): 8 bits - Read THRESHOLD; channel = 0 - 15.

F(1)·A(0): 16 bits - Read MASK Register on R1 - R16; 0 = Mask Off; 1 = Mask On.

F(1)·A(1): 8 bits - Read DEAD TIME (bits 0 - 3) & WIDTH (bits 4 - 7).

F(1)·A(2): 8 bits - Read TIME-TO-CHARGE-SCALE.

F(16)·A(0-15): 8 bits - Write THRESHOLD; channel 0 -15; 0 = 0 V, FF = -1.4 V.

F(17)·A(0): 16 bits - Write MASK Register on W1 - W16; 0 = Mask Off; 1 = Mask On.

F(17)·A(1): 8 bits - Write DEAD TIME (bits 0 - 3) & WIDTH (bits 4 - 7) 16 steps; (0000 = minimum; 1111 = maximum).

F(17)·A(2): 8 bits - Write TIME-TO-CHARGE-SCALE; (0 to - 10 mA).

F(25)·A(0): n/a - Generate a TEST PULSE.