OPERATOR'S MANUAL

CAMAC MODEL 2323A
DUAL GATE AND DELAY
GENERATOR

May 1987

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2 PRODUCT DESCRIPTION

GENERAL DESCRIPTION

The CAMAC Model 2323A is a fully programmable dual gate and delay generator. The gate pulse output width is programmable via CAMAC or manual control over the range of 100 nsec (50 nsec at reduced accuracy) to 10 seconds.

The delay signal starts at the trailing edge of the Gate pulse. Its width also is programmable via CAMAC or manual control to values of 10 nsec, 30 nsec, 100 nsec, or 300 nsec. Settings of both gate and delay signals are overwritten under CAMAC control, whereas they are incremented under manual control. Values may be read back via CAMAC.

The Model 2323A is triggerable by either an external START pulse or by a CAMAC command. In the Latched mode, the output pulse width is determined by the time between the START and STOP inputs or CAMAC commands.

The Model 2323A provides NIM outputs of the Gate and Delay and a complementary NIM output of the gate signal. Also, jumper options allow selection of either an ECL gate or delay output and selection of either a TTL gate or delay output of either positive or negative polarity.

FRONT-PANEL DESCRIPTION

Displays

LED's are used to indicate:

1. The channel currently or last selected (A or B)
2. The Gate duration setting (3-1/2 Digit Display)
3. The Gate range setting (μsec, msec, sec, L (latched mode))
4. The Delay width (10, 30, 100, 300 nsec)
5. Channels currently triggered (CHAN A or CHAN B)

Controls

The 3-position (A-OFF-B) CHAN switch is used to select either CHAN A or CHAN B. Settings can be changed manually only while the CHAN switch is depressed.

The pushbutton UP (DOWN) switch is used to increment (decrement) the display setting. The display increments (decrements) at about 2 Hz for the first eight counts and then changes to a faster rate.

The pushbutton RANGE switch selects the order of magnitude of the gate setting and advances the decimal point and the range setting indicators accordingly. The indicator advances from μsec to sec and then the display goes blank for two increments as the L indicator comes on. This is the Latched mode.

The pushbutton DELAY WIDTH switch selects the width of the Delay pulse and advances the Delay width indicators accordingly.

The 2–position, locking TRIGGER switches (one for each channel) select either the positive–going (+) or the negative–going (–) edge of the START pulse as the trigger.

The front–panel multi–turn potentiometers and test points (one for each channel) are used to set the threshold above which the START pulse will trigger the unit. The range of adjustment is –3 V to +3 V and is operated in conjunction with the polarity selecting trigger control described above.

The 2–position, locking CAMAC switch selects either manual control (OFF) or CAMAC control (ON) as long as they are not overwritten by a CAMAC write command.

Inputs

START is a bridged, high impedance pair of inputs via two Lemo–type connectors, allowing for the possibility of daisy chaining START signals. The input threshold level is factory adjusted to –400 ± 50 mV to accept NIM inputs and is adjustable over a range of ±3 V via the front–panel potentiometer. The positive or negative–going edge (selected by the TRIGGER switch) of the START signal initiates the timing cycle. A 50 Ω terminator should be employed in the unused START input. Alternatively, there is space available on the board for an optional 1/8 W, 50 Ω terminating resistor.

STOP is a standard NIM input via a Lemo connector, with an impedance of 50 Ω. In the latched or the preset mode, the STOP signals terminates the timing cycle.

OR is a standard NIM input via a Lemo connector, with an impedance of 50 Ω. The OR signal produces a gate output for as long as it is asserted.

BLANK is a standard NIM input via a Lemo connector with an impedance of 50 Ω. The BLANK signal cancels the Gate outputs (including an OR signal) for as long as it is asserted.

Outputs

NIM is a NIM–standard output via a Lemo connector. This signal goes low (–16 mA) for the Gate duration. The risetime is ≤2.5 nsec and falltime is ≤2.5 nsec.

Complementary NIM is a NIM–standard output via a Lemo connector. This signal goes high (0 mA) for the Gate duration. The risetime is ≤2 nsec and falltime is ≤2.5 nsec.

DLY is a NIM–standard output via a Lemo connector. This signal goes low (–16 mA) at the trailing edge of the gate signal

for the delay duration (10, 30, 100, or 300 nsec). It will be reset high if the leading edge of a new gate occurs during the delay pulse. The risetime is $\leq$2 nsec and the falltime is $\leq$2.5 nsec.

TTL is an open-drain FET output connected to the front-panel Lemo connector. This signal has the option of being normally off (+ polarity) and going high for the gate or delay duration, or normally on (-polarity) and going low for the gate or delay duration. Polarity and gate or delay options are selectable with shorting plugs*. Factory set for negative polarity. There is a factory installed 51 Ω 1/2 W pullup resistor to +5 V. If parallel operation of several 2323A's is desired, this resistor should be removed from all but one output to prevent excessive current. *Note: The 51 Ω pullup (to match 50 Ω cable) will enable operation with output pulse durations greater than 30 nsec. For 10 nsec operation use the NIM output discussed above.*

+E- is an ECL differential pair output via a 2-pin connector. The + (-) signal goes high (low) (-0.8 V (-1.7 V)) for either the gate or delay duration. These options are selectable with shorting plugs*, factory set for Gate output.

OPTIONS

The following options are made available to the user (see Figure 1). They are located at the front-panel end of the main pc board. Note that there are two identical sections, each taking up half of the board space. Channel A(B) is located at the top (bottom).

* Connections made at factory (see Figure 1).

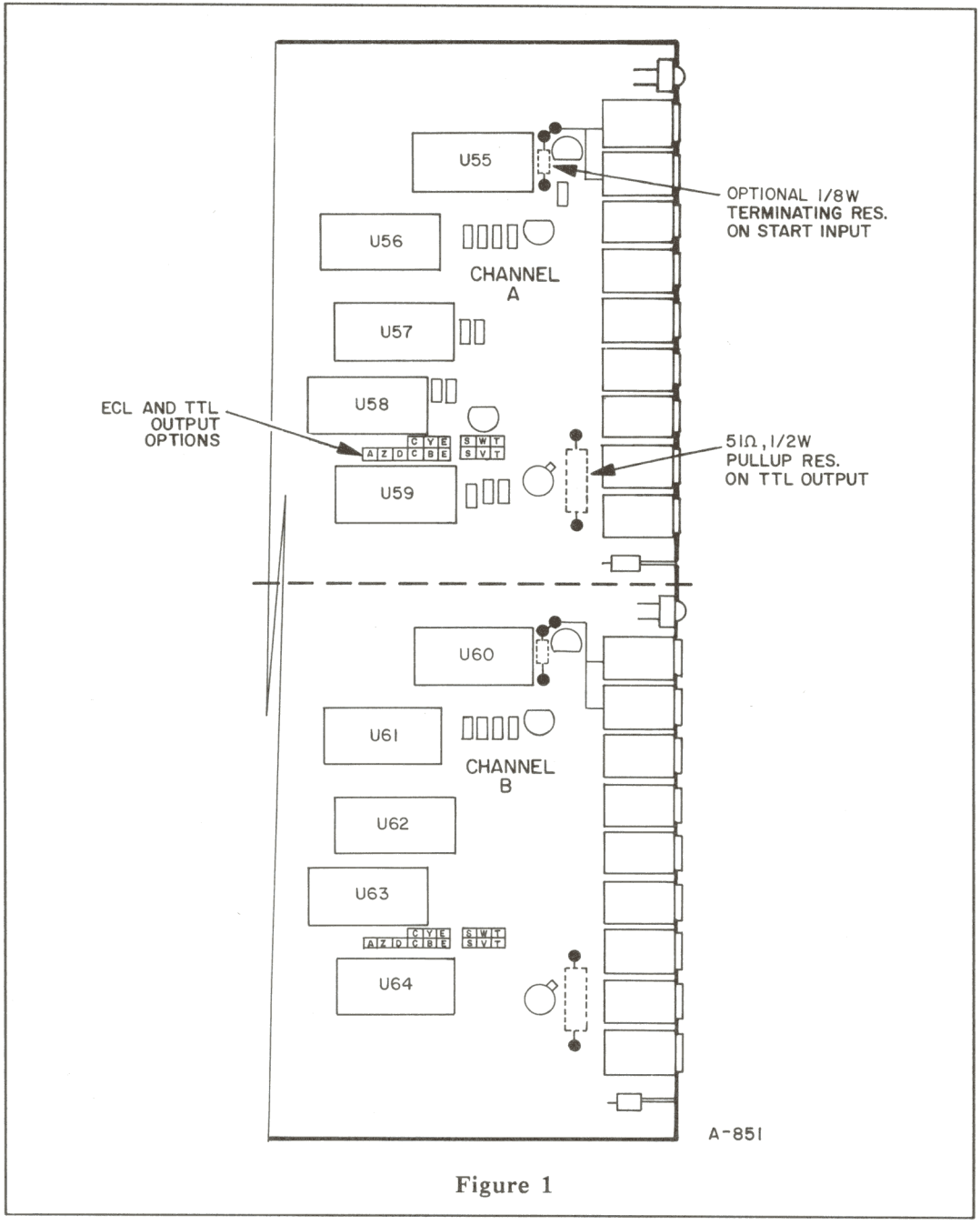

U55
U56
U57
U58
U59
U60
U61
U62
U63
U64
CHANNEL A
CHANNEL B
OPTIONAL 1/8W TERMINATING RES. ON START INPUT
ECL AND TTL OUTPUT OPTIONS
51Ω, 1/2W PULLUP RES. ON TTL OUTPUT
A-851

Figure 1

Should the user wish to terminate the START input with a resistor to ground (typically 50 Ω), space is available at the front-panel side of U55 (U60), the AM865's, for an 1/8 W resistor.

The TTL and ECL outputs are factory set for the Gate output and the TTL polarity is negative (normally on). However, should the user wish to set either or both of these outputs for the delay output or change the TTL polarity, it can be done by moving the shorting plugs according to the table below. The wire wrap pins and shorting plugs are located between and in the vicinity of U58 (U63) and U59 (U64).

LOGIC	OUTPUT	CONNECTIONS
ECL	GATE	B-C *
ECL	DELAY	B-E
-TTL	GATE	Z-A, Y-C, S-W, T-V *
-TTL	DELAY	Z-D, Y-E, S-W, T-V
+TTL	GATE	Z-A, Y-C, S-V, T-W
+TTL	DELAY	Z-D, Y-E, S-V, T-W

* Connections made at factory (see Figure 1).

4 OPERATING INSTRUCTIONS

MANUAL OPERATION

With the CAMAC switch off, the 2323A responds only to the front-panel switches and inputs. Any Gate duration and Delay width can be programmed manually into the 2323A and can be manually changed only.

After setting all values, set the trigger threshold for the START signal, select the positive and negative-going edge with the TRIGGER switch, and apply the START signal to generate an output. Since the factory presets the trigger threshold to -400 ±50 mV, a NIM pulse makes a convenient START signal. In this case, one of the two START inputs should be terminated in 50 Ω unless daisy chaining is desired.

It is possible to generate one output pulse (or a train of output pulses) without a START signal by flipping the TRIGGER switch.

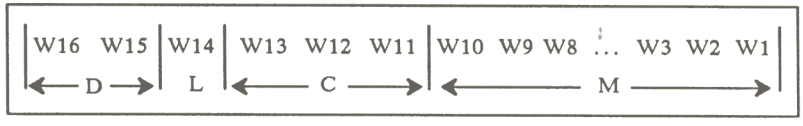
CAMAC OPERATION

With the CAMAC switch on, the 2323A responds to the CAMAC commands listed below. The unit responds to the front-panel switches, but anything programmed in manually will be overwritten immediately should a CAMAC WRITE command be executed. The unit also will respond to the front-panel inputs in this mode.

CAMAC COMMANDS

F(1)•A(0) - READ CHANNEL A PROGRAMMING WORD
F(1)•A(1) - READ CHANNEL B PROGRAMMING WORD
F(9)•A(0) - STOP CHANNEL A OUTPUT
F(9)•A(1) - STOP CHANNEL B OUTPUT
F(17)•A(0) - WRITE CHANNEL A PROGRAMMING WORD
F(17)•A(1) - WRITE CHANNEL B PROGRAMMING WORD
F(25)•A(0) - START CHANNEL A OUTPUT
F(25)•A(1) - START CHANNEL B OUTPUT
C or Z - STOP CHANNELS A AND B OUTPUTS

The CAMAC programming word is 16 bits wide and is divided up into four segments.



The first 10 bits, W1 - W10, are the mantissa (M). This number, seen in the 3-12/3 digit display, ranges from 0 to 1023.

The next 3 bits, W11 - W13, are the characteristic (C). It sets the order of magnitude of the gate duration.

The next bit, W14, is the latch bit (L). When L=0, the gate duration equals $M \cdot 10^C$ nsec. Settings of M below 100 will result in somewhat reduced accuracy and stability. When L=1, the gate duration equals the time between STOP and START.

The next 2 bits, W15 – W16, determine the delay width (D).

D	WIDTH
00	10 nsec
01	30 nsec
10	100 nsec
11	300 nsec

The CAMAC START and STOP commands perform the same function as the external START and STOP inputs.

The CAMAC C or Z commands shut down both outputs simultaneously.

NOTE: In the CAMAC mode, the TRIGGER switches and the threshold pots have no effect.

BATTERY BACK-UP

The Model 2323A has a battery backed up circuit which stores the settings of the mode, gate duration and delay width for the two channels in case of power down. The retention time is in excess of one year.

It is possible that the display will be blank after power up. In order to read the settings, you must first address the channel manually or via CAMAC.

The battery back-up is provided only for the Model 2323A, not for the earlier version 2323.

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