LeCroy

CAMAC ECLine Model 2365
Octal Logic Matrix; 16 × 8

- **CAMAC logic**
- **≥ 100 MHz throughput**
- **16 inputs per #1 CAMAC**
- **Logic fan-in**
- **Coincidence**

- **Complementing input and output**
- **Fast veto**
- **Continuous memory − battery backup**
- **Analog multiplicity output**

The Model 2365 Octal Logic Matrix is a versatile programmable 100 MHz logic unit designed for trigger applications involving high speed logic arrays. It allows complete programmability of all of the logic functions which it provides. The unit is ideal for specifying triggers based upon roadways through hodoscope arrays. An analog multiplicity output via a front panel Lemo Connector is provided for triggering on multi track events.

The Model 2365 accepts 16 differential ECL inputs. These signals are applied to each of the eight independent logic channels. The outputs are differential ECL levels on a standard ECLine header. Two outputs are provided per channel. The 16-bit input size is most useful for large counter arrays. Wide 16-bit input width minimizes the need for cascading of logic units. This results in lower cost and shorter overall trigger propagation delay.

The logic matrix for the Model 2365 is shown in figure 1. Each channel is comprised of a series of programmable select gates which allow a wide variety of boolean logic combinations to be assigned. These functions include:

> **Input selection** — switchyard
> **Complementing** — input and output
> **OR** — logic fan-in
> **AND** — coincidence
> **Veto** — via complementing function

A CAMAC-loadable Test Register, CTR, in the Model 2365 adds to the versatility of the unit. This register may be used as one of the diagnostics for complete CAMAC checkout of the trigger logic. The 16-bit pattern, loaded into the Test Register, may be applied to the inputs of the logic matrix by a CAMAC command, thereby deselecting 16 front panel logic inputs. This operation simulates logic inputs for testing purposes. The eight outputs of the logic matrix may also be read via CAMAC.

The CTR also allows for a sophisticated veto. A consequence of the versatility of the Logic Matrix is that the quiescent states of its outputs are defined by the application. For this reason, the Test Register is used in the veto circuit. Application of a fast front panel ECL Veto Enable signal sets the inputs to the pattern stored in the Test Register for the duration of the Veto Enable pulse (≥ 10 nsec). If the quiescent input levels are loaded in the Test Register, proper veto operation is achieved.

The Model 2365 provides many logic functions never before feasible in such a compact format. Together with the other members of the ECLine logic family, it allows an economical and versatile prompt trigger to be configured under computer control.

March 1983

Innovators in Instrumentation

SPECIFICATIONS
ECLine Model 2365
OCTAL LOGIC MATRIX; 16 × 8

INPUT CHARACTERISTICS

Number of Inputs: 16, direct coupled; 100 Ω, high Z by user option; reflections < 10% for signals of ≥ 2 nsec risetime.

Input Width: ≥ 5 nsec fwhm

Maximum Rate: ≥ 100 MHz

Input Connector: 17-pair front-panel header

Veto Enable: Differential ECL input via two pin header. Input impedance 100 Ω, high Z by simple user modification. When asserted, the contents of the 16-bit CAMAC-programmable test register (CTR) are applied to the logic matrix overriding the front panel inputs. Minimum width 5 nsec. Must precede the Input by ≥ 5 nsec.

OUTPUT CHARACTERISTICS

Logic Outputs: Two per channel, sixteen total; ECL levels via a 34-pin header with pinouts to match the ECLine standard. Output width equals duration of logic condition.

Output Rate: ≥ 100 MHz

Propagation Delay: < 10 nsec

Analog Multiplicity: Front panel Lemo output provides 1 mA for each logic matrix output in the logical 1 state. Rise and falltime < 4 nsec.

MEMORY PROTECTION

Continuous Memory: Memory battery back up. This feature preserves contents of memory and CTR during CAMAC power down. Life of the battery is two years of operation.

MODE CONTROL

Front Panel: The sixteen ECL input levels are applied to the octal logic matrix (8LM). Selected by the CAMAC Mode Selector bit.

Test: The contents of the 16-bit CTR are applied to the 8LM. Selected by the Mode Selector bit.

Veto: The contents of the CTR are applied to the 8LM. Selected via front panel Veto Enable input.

SOFTWARE SELECTED LOGIC COEFFICIENTS (See Figure 1)

$A_{i,j}$ — AND Selector. When set to logical 1, routes the compliment of the ith input to the jth logic matrix OR. When $A_{ij} = 0$, compliment unused.

$B_{i,j}$ — OR Selector. When set to logical 1, routes the ith input to the jth logic matrix OR. When $B_{ij} = 0$ normal signal unused.

C_j — Output Complimentor. When set to logical 1, ≤ routes the compliment of the jth logic matrix OR to the ith output. When $C_j = 0$, the normal OR is used.
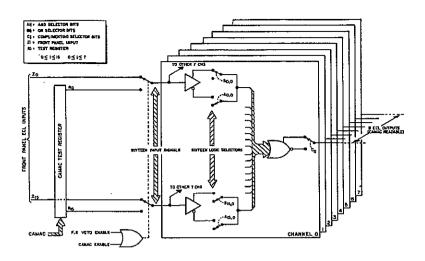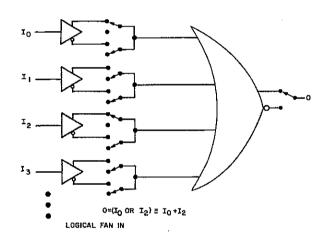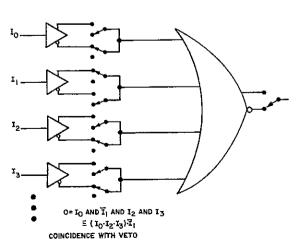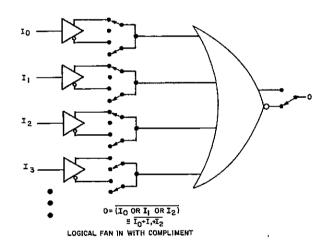
Figure 1

APPLICATION EXAMPLES

$O = (I_0 \text{ OR } I_2) \equiv I_0 + I_2$

LOGICAL FAN IN

$O = \overline{(I_0 \text{ OR } I_1 \text{ OR } I_2)}$
$\equiv \overline{I_0 + I_1 + I_2}$

LOGICAL FAN IN WITH COMPLIMENT

$O = I_0 \text{ AND } \overline{I_1} \text{ AND } I_2 \text{ AND } I_3$
$\equiv (I_0 \cdot I_2 \cdot I_3) \cdot \overline{I_1}$

COINCIDENCE WITH VETO

$O = \overline{I_0} + \overline{I_1} + I_2$
$\equiv \overline{(I_0 \cdot I_1 \cdot \overline{I_2})}$

COINCIDENCE WITH COMPLIMENTARY OUTPUT

BIT MAP

Logical Designation	Logic Coefficient Word (16 bits)			Programming Designation
$B_{i,0}$	$B_{15,0}$	• • •	$B_{0,0}$	PW0
$A_{i,0}$	$A_{15,0}$	• • •	$A_{0,0}$	PW1
$B_{i,1}$	$B_{15,1}$	• • •	$B_{0,1}$	PW2
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
$A_{1,7}$	$A_{15,7}$	• • •	$A_{0,7}$	PW15
C_j	X • • • X	C_7 • • •	C_0	PW16
T_i	T_{15}	• • •	T_0	PW17

CAMAC COMMANDS

$F(0) \cdot A(0)$: Read 18 sixteen-bit programming words. Eighteen successive read commands must be done to complete read operation and reinitialize the 2365 for logical operation.

$F(0) \cdot A(1)$: Read 16-bit input pattern. The ECL logic levels at the input must be static during the read cycle.

$F(0) \cdot A(2)$: Read 8-bit output word. Outputs must be static during the read cycle.

$F(0) \cdot A(3)$: Read Mode Selector bit (0 indicates Front Panel mode, 1 indicates Test mode).

$F(9) \cdot A(0)$: Initialize the 2365. This operation is required on power up.

$F(16) \cdot A(0)$: Write eighteen 16-bit programming words. Requires 18 successive write commands.

$F(16) \cdot A(3)$: Write Mode Selector bit (0 indicates Front Panel mode, 1 indicates Test mode).

X: An $X = 1$ response is generated for any valid $N \cdot F \cdot A$.

Q: A $Q = 1$ response is generated for $F(0) \cdot A(0)$ and $F(16) \cdot A(0)$. A $Q = 0$ response is generated at the 18th successive command (terminal count). This Q response is valid only if a $F(9) \cdot A(0)$ has been performed at power up.

GENERAL

Packaging: In comfomance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100 or IEEE Report 583. RF-shielded CAMAC #1 module.

Current Requirements:
< 400 mA at $+6$V
< 2.5 A at -6V

SPECIFICATIONS SUBJECT TO CHANGE

SECTION I

SPECIFICATIONS

1.2   Introduction

The Model 2365 Octal Logic Matrix (8LM) is a high speed (100 MHz), programmable logic unit.   Each of the 8 independent ECL output channels is a programmed, logical function of the 16 ECL inputs.   Simple functions such as input selection, input complementing, ANDs, ORs, and output complementing as well as more complex mixed logic functions are possible with the 8LM.

Programming of the 8LM involves creating a matrix of logic coefficients 16 bits wide (1 word) and 18 words deep.   These coefficients determine the logical function the output channels and the test pattern in the CAMAC programmable Test Register (CTR).

The inputs to the 8LM can be switched from the front panel to the test pattern in the CTR by either selecting the Test Mode via CAMAC or applying a veto signal at the front panel.   In addition to the digital outputs, the 8LM provides an analog current output of -2 mA for each digital output in the high state.

1.3   Front Panel Connectors

INPUTS:

1.   The "IN" port consists of 16 ECL differential inputs via a 17-pair header, with pin out matching the LeCroy ECLine standard.   The input impedance is $100\ \Omega \pm 5\%$ and can be made high impedance by simply removing the four, 8-pin, 100 Ω resistor networks in the strip sockets located directly behind the connector.   The high impedance feature allows more than one ECLine input to be driven from a single source by cascading, see LeCroy's ECLine Application Note. In the Front Panel Mode, these 16 inputs are applied to the logic matrix.   The minimum pulse width is 5 nsec.

2.   The "VETO" input is an ECL differential input via a bridged 2-pair header.   Input impedance is $100\ \Omega \pm 5\%$ and can be made high impedance by simply removing the 8-pin, 100 Ω resistor in the strip sockets located directly behind the connector.   The contents of the 16-bit CAMAC programmable Test Register (CTR) are applied to the logic matrix for the duration of the veto signal.   The front panel inputs are overridden for this time.   The minimum veto pulse width is 10 nsec and this signal must preceed the inputs by at least 2 nsec.

OUTPUTS:

1. "OUT A" and "OUT B" are two identical ports, each consisiting of 8 ECL differential outputs via the same 17-pair header. Each of the 8 outputs is an independent channel whose logic is a function of the 16 inputs and the CAMAC programmable logic coefficients for that channel. The output signals last for the duration of the logic condition after a < 10 nsec delay through the unit. At frequencies approaching 100 MHz, these signals should not be observed directly, but only at the output of a line receiver.

2. "ANALOG OUT" is a current output via a LEMO-type connector. Each of the logic matrix outputs in its high state contributes -2 mA to this output. Thus, with all 8 logic outputs in their high state, -16 mA is generated. Driving a 50 Ω cable amounts to a total of -800 mV, in -100 mV steps. The current output lasts for the duration of the logic condition, after < 10 nsec delay. Its transition time is < 4 nsec.

1.4 Continuous Memory

Semiconductor memory including that contained with the Model 2365 loses its information when the power is shut off. Continuous memory is a special feature added to the circuit to protect against such losses. It employs a battery which maintains (backs up) the Model 2365 memory when power is off.

The use of low power CMOS registers has made battery back-up of the logic matrix, as well as the Mode Selector bit, possible. The battery can power the unit for up to 5 years and is not used when the crate power is on. The battery shelf life is 5 years.

SECTION 2

OPERATING INSTRUCTIONS

2.1   CAMAC Commands

The Model 2365 generates an X=1 response of each of the following commands:

F(0)•A(0)   Read eighteen 16-bit programming words. Eighteen successive read commands must be done to complete the read operation and re-initialize the 2365 for logical operation.

F(0)•A(1)   Read the 16-bit input pattern from the front panel or the CTR depending upon the selected mode. Front panel inputs must be static during this operation.

F(0)•A(2)   Read the 8-bit output word. Front panel inputs must be static during this operation.

F(0)•A(3)   Read the Mode Selector bit.

F(9)•A(0)   Initialize the 2365. This operation is required on power-up.

F(16)•A(0)   Write eighteen 16-bit programming words. Eighteen successive write commands must be performed to complete the write operation and re-initialize the 2365 for logical operation.

F(16)•A(3)   Write the Mode Selector bit.

Q   A Q=1 response is generated for each F(0)•A(0) and F(16)•A(0) until the 18th successive command (terminal count) at which point Q=0. This is the Stop on Word mode Q-response for block transfers as described in the CAMAC Instrumentation and Interface Standards (IEEE Standard 583-1975). This Q response is valid only if the 2365 has been initialized by (F(9)•A(0)) after power-up.

2.2   Mode Control

The Mode Selector bit is used to direct either the front panel inputs or the contents of the CTR to the logic matrix.

When this bit is 0, the 16 front panel inputs are applied to the logic matrix. The 2365 is normally run in this front panel mode.

When this bit is 1, the contents of the 16-bit CTR are applied to the logic matrix. This test mode is used to examine the 2365 for proper logical functioning. This is a static test, i.e., the outputs will remain in their test state for as long as the Mode Selector bit remains a 1.

2-1

When the Mode Selector bit is 0 and a front panel Veto level is applied, the contents of the CTR are applied to the logic matrix for the duration of the veto pulse. In this Veto mode, the CTR should be loaded with the quiescent input levels. Applying the Veto then forces the outputs to their quiescent states. If the CTR is loaded with a test pattern, pulsing the Veto input results in an active test of the 2365. The outputs will remain in their test state for the duration of the Veto.

2.3 Software Selected Logic Coefficients

Logical functioning of the Model 2365 depends upon the logic coefficient that are programmed into the logic matrix. The logic coefficients themselves are selector bits which determine whether an input is to be ANDed, ORed, or complemented, if an output is complemented and what the test pattern in the CTR is. These coefficients are arranged into a 16 bit (1 word) by 18 word matrix which is then loaded into the 2365. The coefficients are defined as follows:

$A_{i,j}$ AND selector. When set to a logical 1, the complement of the ith input is enabled and used to produce the jth output. When $A_{i,j} = 0$, the complement of the ith input is disabled and unused in producing the jth output.

$B_{i,j}$ OR selector. When set to a logical 1, the ith input is enabled and ued to produce the jth output. When $B_{i,j} = 0$, the ith input is disabled and unused in producing the jth output.

C_j Output complementor. When set to logical 1, the jth output is complemented. When $C_j = 0$, the jth output is uncomplemented.

T_i Test input. When set to a logical 1, the ith bit of the CTR is set to a logical 1. When $T_i = 0$, the ith bit of the CTR is a logical 0.

The matrix of logic coefficients is arranged according to the following bit map.

Logical Designation	Logic Coefficient Word (16 bits)			Programming Designation
$B_{i,0}$	$B_{15,0}$	$\cdots$	$B_{0,0}$	PW0
$A_{i,0}$	$A_{15,0}$	$\cdots$	$A_{0,0}$	PW1
$B_{i,1}$	$B_{15,1}$	$\cdots$	$B_{0,1}$	PW2
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
$A_{i,7}$	$A_{15,7}$	$\cdots$	$A_{0,7}$	PW15
C_j	X $\cdots$ X $\quad C_7 \cdots$		C_0	PW16
T_i	T_{15}	$\cdots$	T_0	PW17

The OR selectors for a given output channel are programmed first, followed by the AND selectors for that channel. This amounts to two words per channel. The output channels are programmed in sequence, 0 through 7.

The output complementor bits come next followed by the test input pattern. The $F(16) \cdot A(0)$ command writes this matrix into the unit beginning with PW0. All eighteen words must be loaded for proper operation because the words are shifted in serially. The $F(0) \cdot A(0)$ command reads this matrix beginning with PW0.

2.4   Determining the Logical Function

The 2365 operates according to the following logical function table.

INPUT(I_i) TRUTH	$B_{i,j}$(OR)	$A_{i,j}$(AND)	C_j(COMP)	T_i(Veto)	OUTPUT Q_j TRUTH	LOGIC
+	1	0	0	0	+	OR
+	1	0	1	0	−	OR
−	1	0	1	1	+	AND
−	1	0	0	1	−	AND
+	0	1	1	0	+	AND
+	0	1	0	0	−	AND
−	0	1	0	1	+	OR
−	0	1	1	1	−	OR

When $A_{i,j} = B_{i,j} = 0$, input I_i is disabled and unused in producing output Q_j. $B_{i,j} = A_{i,j} = 1$ is an undefined state.

If the inputs have positive polarity (high true) then,
an OR output requires that the $B_{i,j} = 1$,

a NOR output requires that the $B_{i,j} = 1$ and $C_j = 1$,

an AND output requires that the $A_{i,j} = 1$ and $C_j = 1$,

a NAND output requires that the $A_{i,j} = 1$.

If the inputs have negative polarity (low true) then,
an OR output requires that the $A_{i,j} = 1$,

a NOR output requires that the $A_{i,j} = 1$ and $C_j = 1$,

an AND output requires that the $B_{i,j} = 1$ and $C_j = 1$,

a NAND output requires that the $B_{i,j} = 1$.

Thus either polarity input can be handled quite easily and either polarity output can be produced. The T_i for the veto are simply set to the input quiescent state.

2.5   Application Example

The following examples are helpful in explaining the operation of the 2365.

1.   Output channel 0 is to be a logical fan in (OR) of inputs I_0, I_2, and I_4.

$$Q_0 = I_0 + I_2 + I_4.$$

$$B_{0,0} = B_{2,0} = B_{4,0} = 1. \quad \text{All other } B_{i,0} = 0.$$

$$A_{i,0} = 0. \quad C_0 = 0.$$

2.   Output channel 1 is to be a logical fan in with complement (NOR) of inputs I_7 and I_{15}.

$$Q_1 = I_7 + I_{15}.$$

$$B_{7,1} = B_{15,1} = 1. \quad \text{All other } B_{i,1} = 0.$$

$$A_{i,1} = 0, \quad C_1 = 1$$

3.   Output channel 2 is to be a logical coincidence (AND) of inputs I_9, I_{11}, and I_{13}.

$$Q_2 = I_9 \cdot I_{11} \cdot I_{13}.$$

$$B_{i,2} = 0. \quad A_{9,2} = A_{11,2} = A_{13,2} = 1. \quad \text{All other } A_{i,2} = 0$$

$$C_2 = 1.$$

4.   Output channel 3 is to be a logical coincidence with complement (NAND) of inputs I_6 and I_{14}.

$$Q_3 = \overline{I_6 \cdot I_{14}}$$

$B_{j,3} = 0.$ $A_{6,3} = A_{14,3} = 1.$ All other $A_{j,3} = 0.$

$C_3 = 0.$

5.   Output channel 4 is to be a logical fan in (OR) of inputs I_1 and I_3.   These inputs are low true.

$$Q_4 = I_1 + I_3.$$

$B_{j,4} = 0.$ $A_{1,4} = A_{3,4} = 1.$ All other $A_{j,4} = 0.$ $C_4 = 0.$

6.   Output channel 5 is to be a logical coincidence (AND) of inputs I_{10} and I_{12}.   These inputs are low true.

$$Q_5 = I_{10} \cdot I_{12}.$$

$B_{10,5} = B_{12,5} = 1.$ All other $B_{j,5} = 0.$

$A_{j,5} = 0,$ $C_5 = 1.$

7.   Output channel 6 is to be a logical fan in with complement (NOR) of inputs I_9, I_{10}, I_{11}, and I_{12}. I_{10} and I_{12} are low true.

$$Q_6 = \overline{I_9 + I_{10} + I_{11} + I_{12}}$$

$B_{9,6} = B_{11,6} = 1.$ All other $B_{j,6} = 0.$

$A_{10,6} = A_{12,6} = 1.$ All other $A_{j,6} = 0.$

$C_6 = 1.$

8.   Output channel 7 is to be a logical coincidence (AND) of inputs I_0, I_1, I_2, and I_3. I_1 and I_3 are low true.

$$Q_7 = I_0 \cdot I_1 \cdot I_2 \cdot I_3$$

$B_{1,7} = B_{3,7} = 1.$ All other $B_{j,7} = 0.$

$A_{0,7} = A_{2,7} = 1.$ All other $A_{j,7} = 0.$

$C_7 = 1.$

The veto pattern in the CTR requires $T_1 = T_3 = T_{10} = T_{12} = 1.$ All other $T_j = 0.$ Note that in their quiescent state, outputs Q_1, Q_3 and Q_6 are in the high state.

The bit map now takes the following form:

Logical Designation	Logic Coefficient	Programming Designation
$B_{i,0}$	0000 0000 0001 0101	PW0
$A_{i,0}$	0000 0000 0000 0000	PW1
$B_{i,1}$	1000 0000 1000 0000	PW2
$A_{i,1}$	0000 0000 0000 0000	PW3
$B_{i,2}$	0000 0000 0000 0000	PW4
$A_{i,2}$	0010 1010 0000 0000	PW5
$B_{i,3}$	0000 0000 0000 0000	PW6
$A_{i,3}$	0100 0000 0100 0000	PW7
$B_{i,4}$	0000 0000 0000 0000	PW8
$A_{i,4}$	0000 0000 0000 1010	PW9
$B_{i,5}$	0001 0100 0000 0000	PW10
$A_{i,5}$	0000 0000 0000 0000	PW11
$B_{i,6}$	0000 1010 0000 0000	PW12
$A_{i,6}$	0001 0100 0000 0000	PW13
$B_{i,7}$	0000 0000 0000 1010	PW14
$A_{i,7}$	0000 0000 0000 0101	PW15
C_j	0000 0000 1110 0110	PW16
T_i	0001 0100 0000 1010	PW17

Eighteen successive $F(16) \cdot A(0)$ write commands load this map into the 2365. Verifying that what has been written is correct requires eighteen successive $F(0) \cdot A(0)$ read commands. Once the desired logic coefficients are loaded into the logic matrix, one should set the Mode Selector bit to the proper state. The battery insures that the data are safe and the Model 2365 can even be removed from the crate without data loss.

As another example, the following list of logic coefficient words can be loaded.

Logical Designation	Logic Coefficient	Programming Designation
$B_{i,0}$	1010 1010 1010 1010	PW0
$A_{i,0}$	0000 0000 0000 0000	PW1
$B_{i,1}$	1100 1100 1100 1100	PW2
$A_{i,1}$	0000 0000 0000 0000	PW3
$B_{i,2}$	1111 0000 1111 0000	PW4
$A_{i,2}$	0000 0000 0000 0000	PW5
$B_{i,3}$	1111 1111 0000 0000	PW6
$A_{i,3}$	0000 0000 0000 0000	PW7
$B_{i,4}$	1111 1111 1111 1111	PW8
$A_{i,4}$	0000 0000 0000 0000	PW9
$B_{i,5}$	0000 0000 0000 0000	PW10
.	.	.
.	.	.
$A_{i,7}$	0000 0000 0000 0000	PW15
C_j	0000 0000 0000 0000	PW16
T_i	0000 0000 0000 0000	PW17

The action of this functional assignment is to cause binary encoding of the input word as a 4-bit output. If only one of the 16 inputs is true, outputs 0-3 indicate which one. Output 4, the OR of all inputs, differentiates between no data and channel zero.

2.6   Cable Requirements

The ECL inputs and outputs are carried by a 17 twisted pair cable with 34-pin flat cable connectors. The veto signal is carried by an individual twisted pair cable with 2-pin connectors. The analog output signal is carried by standard 50 Ω coaxial cable with Lemo cable ends.

SECTION 3

TECHNICAL DESCRIPTION

3.1 Introduction

The circuitry of the Model 2365 can be divided into three sections. The first section is the high speed circuitry, consisting of the front panel inputs and outputs, the input line receivers, input multiplexers, logic matrix hybrids, line drivers, the analog output and the Veto input. The second section is the CAMAC control, consisting of the reading buffers and multiplexers, write buffers, level shifters, and command decoding. The third section is the continuous memory circuitry, consisting of the battery, and the power sensing circuit.

3.2 High Speed Circuitry.

3.2.1 Input to Output

The differential ECL input signals comprising the input, arriving at the front panel via the ECLine standard 17 twisted pair cable, are each terminated in 100 Ω (or high impedance if the 100 Ω SIPS are removed). They are then received by the 10114 line receivers (U5, U6, U8, U10, U12, U13). The outputs of these receivers (I0-I15) are pulled-down with 330 Ω to -5 V and are multiplexed with the outputs of the CAMAC Test Register, CTR, (V0-V15) by the 10H158 quad two input multiplexers (U19-U22). The outputs of these multiplexers (M0-M15) are pulled down with 56 Ω to -2 V and are then input to the Logic Matrix hybrids (HLM440 U36-U43). M0-M15 are also buffered with 1 kΩ series resistors (N0-N15) and input to level shifters for CAMAC reading.

The HLM440 matrices form the heart of the Model 2365. Each HLM440 consists of four fast inputs, outputs, and four logic coefficient inputs and outputs. The logic coefficient inputs are ECL compatible CMOS signals (power supplies V_{dd} = -0.8 V, V_{ss} = -5.2 V) and are stored in latches (74C374) in the hybrid. The outputs of these latches become the inputs of the multiplexers (10H158) where the logic function is determined. Figure 3.1 is a simplified schematic of the logic.

This figure shows how inputs M_i and M_j contribute to each of the outputs O0-O3. This is one half of an HLM440. Each input is buffered and converted to differential signals. The high-true signal is ANDed with the B coefficients and the low true signal is ANDed with the A coefficients. When $B_{i,0} = A_{i,0} = B_{j,0} = A_{j,0} = 0$, inputs M_i and M_j do not contribute to Output O0, (Points $j,1$ and $j,2$ are wire-ORed to each other and to the other four points that contribute to O0. While 1 and 2 are themselves low other points can pull O0 high).

If $B_{i,0} = B_{j,0} = 1$ and if M_j goes high, the O0 goes high. If M_i goes low and Mj goes high, O0 goes high again. This is the OR configuration. O0 is an OR of any combination of inputs that are selected by the B coefficients.

If $A_{i,0} = A_{j,0} = 1$ ($B_{i,0} = B_{j,0} = 0$) and both M_i and M_j are 0 (assume all other inputs are not selected) then O0 is high. If M_i goes high, O0 remains high. If, however, both M_i and M_j go high together, O0 is forced low. This is the AND configuration (actually a NAND configuration), O0 can be subsequently inverted at the output drivers by the complement bit C0). O0 is an AND of any combination of inputs that are selected by the A coefficients.

If $A_{i,0} = B_{i,0} = 1$, O0 is forced on all the time. This condition is not defined.

The logic coefficients are shifted in, in a word serial format, one output at a time. There are 16 OR and AND coefficients referring to a specific input. Hence the first word shifted in consists of the $B_{i,0}$ coefficients, the OR coefficients selecting inputs i for Output O0. Next comes the $A_{i,0}$ coefficients and so on through Output O7.

The eight hybrids are combined to form the eight outputs O0–O7. There are two groups of four hybrids, one group making O4–O7 and the other making O0–O3 (see schematic). These outputs are pulled down with 56 Ω to -2 V and are input to the 10H107 EXOR output drivers (U51, U53, U55, U130, U131, U132). The logic coefficient word D0–D15 is shifted through the first group of hybrids, then through the second group (SD0–SD15) and are then input to level shifters for CAMAC reading.

The other inputs to the 10H107s are the D0–D7 lines which are actually the complement bits C0–C7. The EXOR gates are utilized for their complementing ability. If a logic matrix output is in the AND condition it is low true. Setting the corresponding complement bit high then inverts this output at these gates. The outputs of the gates of U51, U53, and U55 are pulled-down with 220 Ω to -5 V are drive the output connector of the unit. These outputs are bridged. One gate drives two differential outputs simultaneously.

3.2.2 Analog Output and Veto Input

The gates of U130, U131, and U132 actually reproduce the front panel outputs but their outputs are used for CAMAC reading and for (PN2369) driving the analog output circuitry. The high true outputs are pulled down with 1 kΩ to -5 V and buffered with 1 kΩ series resistors (Q0–Q7) and input to level shifters for CAMAC reading. The low time outputs are pulled down with 220 Ω to -5 V and input to the bases of the transistors driving the analog output. When an output goes low, its corresponding transistor turns off and the other half of the differential pair turns on, contributing -2 mA to the analog output.

The bridged pair of Veto inputs is terminated in 100 Ω (or high impedance if the 100 Ω SIP is removed). It is received by a 10114 line receiver (U5). The output is pulled down with 330 Ω to -5 V and ORed with the Mode Selector bit A from CAMAC at the 10H102 (U2). The output of this gate is pulled down with 330 Ω to -5 V and is used as the select input to the input multiplexers (U19-U22). When this input is low, the front panel inputs (I0-I15) are selected and routed to the logic matrix hybrids. When high, the CTR outputs (V0-V15) are selected.

3.3   CAMAC Circuitry

3.3.1   Writing and Reading

The CAMAC write lines W1-W16 are received by 74LS240 inverter buffers (U70-U71). The tristate outputs of these write buffers are tied together with tri-state outputs of the various read buffers to form the bus R0-R15. This bus is level-shifted to ECL-CMOS with LM339 comparators (U74-U77) and 1 kΩ pull-ups to V_{dd} (-0.8 V).

During a write cycle (F(16)·A(0)), the write buffers are enabled, and the information in W1-W16 is level-shifted and input to the CTR (74C374 U104,U105) where it is clocked in at S2 time by a level-shifted S2. During the next cycle, the CTR is loaded with new information and the information previously at the CTR is shifted to the complement bit register (74C374 U109,U110). The next cycle results in this information again being shifted, now into the first of 16 locations in the logic matrices (U36-U39). At the end of 18 write cycles the logic matrices as well as complement bit register and the CTR are fully loaded, data having been shifted in during each cycle. Thus in order to get the logic coefficients and the complement and CTR bits in their proper loation, 18 write cycles must be performed each time something is changed.

The buffered signals from the high speed circuitry that are read via CAMAC are first level shifted from ECL-CMOS to TTL and then buffered with tri-state devices. The buffered logic matrix fast inputs N0-N15 are input to LM339s (U94-U97). The outputs have series 1 kΩ resistors and 2.7 KΩ pull-ups to +5 V and are input to tri-state devices 74LS258s and 74LS240 (U107, U108, U111). The buffered outputs Q0-Q7 are level shifted by LM339s (U82-U83) and their outputs are input to 74LS258s (U107-U108). The logic coefficients from the hybrids SD0-SD15 are also level shifted by LM339s (U60-U63) and their outputs are input to 74LS240 (U72-U73).

Reading the logic coefficients involves the same procedure as does writing. Eighteen successive reads are required in order to obtain all the coefficients and well as write then back into the logic matrix. During a read cycle (F(0)·A(0)) the read buffers (U72-U73) are enabled as well as the CAMAC read buffers (7403 U118-U121). The information is read by CAMAC and it is also level-shifted by U74-U77 and at S2 time rewritten into the matrix. Thus after a complete read cycle (18 reads) the coefficients in the matrix are again intact.

The tri-state devices U107-U108 and U111 are enabled during an $F(0) \cdot A(1)$ cycle allowing the buffered inputs to the logic matrix to be read. U107 and U108 are enabled also during an $F(0) \cdot A(2)$ cycle, this time selecting the buffered outputs for reading.

The Mode Selector bit is written during an $F(16) \cdot A(3)$ cycle. Level shifted R0 is input to a latch (74C173 U113) and clocked in at S1 time by a level shifted S1. The output of the latch is the A line used for selecting front panel inputs or CTR outputs to the logic matrix. This A line is also level shifted (U45) and buffered (74LS365 U115) and available for reading by an $F(0) \cdot A(3)$.

3.3.2   CAMAC Command Decoding

The CAMAC command decoding is done with the 74LS138 decoders (U87-U88) and the gates of U81, U106, U126 and U92. U87 decodes the F codes and U88 decodes the A signals. The gates produce the $F \cdot A$ signals. S1 is gated with $F(16) \cdot A(3)$ and level shifted (U128) to clock U113. It is also gated with $F(9) \cdot A(0)$ to reset the internal counter (see below). S2 is gated with $F(0) \cdot A(0)$ and $F(16) \cdot A(0)$, level shifted (U128), gated with OFF (see below) and buffered (Q2) to produce the clock which shifts the logic coefficients through the matrix.

All decoded commands are ORed together to produce an X response (U122). Two four-bit counters (74LS169 U124,U125) count the number of times the $F(0) \cdot A(0)$ and $F(16) \cdot A(0)$ commands are executed. During a reset command ($F(9) \cdot A(0)$), these counters are loaded with the number 17. They count down by one during each cycle. Upon reaching terminal count (0), they disable the Q response (U122) which was valid for these commands. Thus, when Q=0 during an $F(0) \cdot A(0)$ or $F(16) \cdot A(0)$ command the reading from or writing to the logic matrix is complete.

3.4   Continuous Memory

3.4.1   The Battery

The battery, a 3.6 V, 1 Ah, lithium cell, EI3B50, backs up the 74C374 latches in the logic matrix hybrid, the 74C374 latches which store the CTR and the complement bits, the 74C173 latch which stores the Mode Selector bit, and A 74C02 (U44) when the CAMAC power is turned off. The battery is isolated by a 1N4448 diode (CR1) during CAMAC power. The power line for the backed up IC's, V_{ss}, is thus either -5 V when the crate is on or -3.2 V when the crate is off. The typical current during the back-up phase is < 1 μA. The battery may be disconnected from the circuit by removing the jumper plug located near the battery.

3.4.2   Power Sensing Circuitry

In order to preserve the integrity of the logic coefficients, the CTR, the Complement Bits, and the Mode Selector bit during power up and power down, it is necessary to deselect these devices at these critical times. The sensing circuitry consists of the 2N5771 (Q1), the TIL209A LED's (CR4, CR5) and the other associated components.

When the power is on, Q1 is on and its collector is near -0.8 V. The OFF line (U44 pin 1) is low and the various CMOS devices are thus enabled.

When power is turned off, the circuitry senses when -6 V drops to about -5 V and then turns off Q1, its collector dropping to V_{ss}. OFF goes high very quickly and thus disables all the CMOS devices. The CLK, in particular, is disabled thus preventing any extraneous spikes which could cause the coefficients to be shifted.

On power up, Q1 does not turn on until the supply voltage is sufficiently close to its nominal value thereby avoiding undefined conditions in the circuitry which may be caused by supply voltage transients.

PART NUMBER	DESCRIPTION	QUANTITY PER
103327103	CAP CERA MONO 50V .01 UF	91
103427104	CAP CERA MONO 100V .1 UF	9
146424106	CAP MINI ALUM 20% 10 UF	4
147214221	CAP ALUM METAL CAN 220 UF	2
161225101	RES CARBON FILM 100 OHMS	1
161225102	RES CARBON FILM 1 K	4
161225103	RES CARBON FILM 10 K	3
161225121	RES CARBON FILM 120 OHMS	2
161225153	RES CARBON FILM 15 K	1
161225161	RES CARBON FILM 160 OHMS	1
161225201	RES CARBON FILM 200 OHMS	1
161225272	RES CARBON FILM 2.7 K	1
161225331	RES CARBON FILM 330 OHMS	1
161225332	RES COMP 1/8W 5% 3.3 K	1
161225432	RES CARBON FILM 4.3 K	2
161225621	RES CARBON FILM 620 OHMS	1
161225750	RES CARBON FILM 75 OHMS	2
190042102	RESISTOR NETWORK 1 K	3
190042221	RESISTOR NETWORK 220 OHMS	3
190042272	RESISTOR NETWORK 2.7 K	5
190042331	RESISTOR NETWORK 330 OHMS	2
190042560	RESISTOR NETWORK 56 OHMS	1
190642152	RESISTOR NETWORK 1.5 K	2
190832101	RESISTOR NETWORK 100 OHMS	5
190832102	RES NETWORK 1 K	16
190842560	RESISTOR NETWORK 56 OHMS	4
200031033	IC 2-INPUT NAND SN7403N	5
200031046	IC HEX INVERTER SN74LS04N	1
200031051	IC 2-INPUT NOR SN74LS02N	1
200031073	IC 2-IN POS OR SN74LS32N	2
200031086	IC 2-INPUT AND SN74LS08N	2
200041058	IC BUS DRIVER SN74LS365N	1
200041062	IC DEC/DEMULTP SN74LS138N	2
200041065	IC UP/DN CNTR SN74LS169AN	2
200041258	IC DATA SEL/MPX SN74LS258	2
200071001	IC 8 X BUFFER SN74LS240	5
200330000	IC 2-INPUT NAND 74F00	1
200344102	IC QUAD 2-IN NOR 10H102	1
200344107	IC 3X 2-IN OR/NOR 10H107	6
204042015	IC LINE RECEIVER MC10114P	6
206023374	IC 8-BIT LATCH MM74C374	4
206033002	IC 2-IN NOR GATE MM74C02N	1
206043173	IC D-TYPE FL-FL MM74C173N	1
207344158	IC QUAD 2-IN MPLX 10H158	4
208031009	IC VOLT COMPARATOR LM319N	1
208031010	IC QUAD DIFF COMP LM339N	15
208122337	IC ADJ -VOLT REG LM337T	2
229020055	TRANS VOLT SUPPR P6KE6.8	2
230110005	DIODE SWITCHING 1N4448	3
235010005	DIODE RECTIFIER 1N4005	2
235050001	DIODE RECTIFIER 1N4139	2
253010835	DIODE HOT CARRIER HP2835	1
256233209	DIODE LED RED MV5075C	2
270110001	TRANSISTOR NPN PN2369A	16

FIS/NCA V4.3A
ZZBPSS.NCA;
ZZIPMS.NCA;

LECROY CORPORATION
2365 PARTS LIST

PAGE   2
13-FEB-87
MANUALBOM.FCF;

PART NUMBER	DESCRIPTION	QUANTITY PER
270170001	TRANSISTOR NPN 2N5770	1
275170002	TRANSISTOR PNP 2N5771	1
300010001	BEAD SHIELDING FERRITE	1
300050001	CHOKE FERRITE SINGLE LEAD	2
312060050	BATTERY PC MTG 3.9V	1
385020180	INSULATING FILM KAPTON	0
400020014	SOCKET IC ST DIP-14	29
400030016	SOCKET IC ST DIP-16	25
400040024	SOCKET IC ST DIP-24	8
400170020	SOCKET IC ST DIP-20	9
402112001	CONN PC MTG LEMO NICKEL	1
403119234	HEADER RT ANGLE 34-PIN	2
405812002	SOCKET STRIP SOLDR 20 POS	2
408063005	W-W PIN, ONE SIDE, 1 WRAP	2
433220002	FUSE PICO II 125V 3 AMP	1
433225001	FUSE PICO II 125V 5 AMP	1
454370002	SHUNT 2 POS	1
454713004	HDR DIP SOLDER TO MALE 4	1
505070003	HEAT SINK FOR TO-220	2
521000004	SPACER HEX 2-56X.417	4
540203001	SIDE COVER CAMAC STD(LIP)	1
540206078	RAIL CAMAC STD TOP W/LIP	1
540206178	RAIL CAMAC STD BOT W/LIP	1
540209101	REAR PANEL CAMAC SIZE 1	1
555430003	CAPTIVE SCREW ASSEMBLY	1
560256005	SCREW PHILIPS 2-56X5/16	4
560440002	SCREW PHILIPS 4-40X1/8	2
560440003	SCREW PHILIPS 4-40X3/16	4
560440004	SCREW PHILIPS 4-40X1/4	2
567440006	SCREW FLAT PHIL 4-40X3/8	2
568256002	SCREW FLAT PHIL 2-56X1/8	4
591101022	WIRE BUS TIN-COPP AWG 22	1
595901022	SLEEVING TEFLON AWG 22	1
599060162	SEALANT RTV162-3T	0
712365003	PC BD PREASS'Y 2365	1
722365003	FRONT PNL PREASS'Y 2365	1
732365002	SIDE CAMAC LEFT 2365	1
HLM440	IC 4X4 LOGIC MATRX HLM440	8

End of report. 92 Details encountered.