LeCroy

CALIFORNIA

CAMAC MODEL 8212

DATA LOGGER

instrumentation
for the study of
transient phenomena

PALO ALTO, CA.

technical information manual

CAMAC MODEL 8212

DATA LOGGER

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

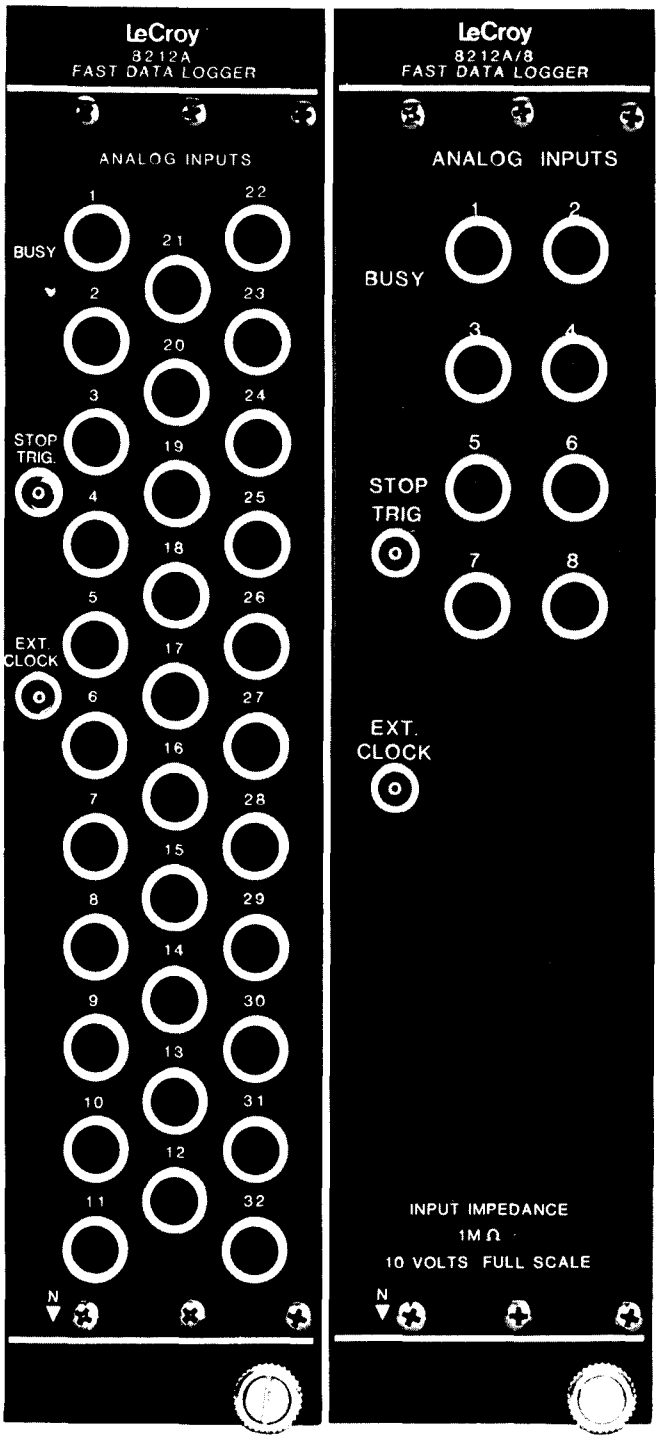
ENGINEERING DEPARTMENT
LeCroy/CALIFORNIA
PALO ALTO, CALIFORNIA

TABLE OF CONTENTS

TABLE OF CONTENTS

(Continued)

LeCroy



CAMAC Models 8212A and 8212A/8

High Accuracy Simultaneous Sampling Data Loggers

- **High density:** up to 32 inputs
- **Independent measurements:** Operates as if there were a separate ADC for each input
- **High sensitivity:** 12 bits, or 0.025% resolution
- **50 KHz bandwidth**
- **Full-scale range of either ±5 V or 0 to 10 V**
- **Differential inputs:** Eliminate 50-60 cycle and other common mode noise
- **Up to 5 kHz simultaneous sampling:** 32 channels
- **100 kHz maximum sampling rate:** One active channel
- **Expandable memory:** Utilize 32K word Model 8800A Memory modules

The LeCroy Models 8212A and 8212A/8 are multi-input 12-bit ADC's intended for use with the LeCroy Model 8800A 32K word Memory module in low frequency transient monitoring applications. The Model 8212A contains 32 independent channels with simultaneous sampling speeds from 40 kHz to 0.2 kHz depending upon the number of active channels. The 8212A/8 contains 8 channels and supports sampling from 100 kHz to 0.5 kHz.

With both versions, the number of active inputs is programmable. As fewer inputs are used, available memory storage per channel and maximum achievable sampling rate are increased. This allows flexible reorganization of sampling and storage parameters for unique experimental situations.

Both digitizers offer full differential inputs which accept ±5 V signals (or by factory modification, 10 V signals of

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

either polarity). Common Mode rejection, better than 40 dB at 4 kHz and 66 dB under 500 Hz, eliminates noise which would otherwise disturb the 12-bit resolution.

Each input to the digitizers has a separate track-and-hold driven by a common clock, ensuring that all inputs are sampled simultaneously, minimizing aperture uncertainty and channel-to-channel phase shifts in the digitized waveforms.

The 8212A can be used in one of two modes. In a "Sweep-and-Log" mode the data logger continually samples all channels simultaneously. The analog signal level from each channel's independent track-and-hold is converted sequentially, each measurement requiring less than 6 μsec dwell time. A complete scan of 32 inputs takes less than 200 μsec. Digitizing is governed either by the internal clock or by clock cycles applied to an external clock input. The data is sequentially stored in up to four Model 8800A 32K word Memory modules. Equal memory segments are automatically assigned to the programmed number of active channels. In this Sweep-and-Log mode, memory is continually overwritten retaining only the most recent conversions. An externally applied Stop Trigger or a CAMAC F(19) or F(25) will stop the digitizer and memory, either instantly or after a pre-programmed number of post-trigger conversions, thus capturing a digitized window of interest. A "Single Scan" mode allows one sample on each active input to be acquired under direct computer supervision for real-time control applications.

The Model 8212A is ideal for logging fast response thermocouple and strain gauge readings on tokamaks, mirror machines and other fusion devices, biomedical transducers, superconducting magnet currents, or other measurments where a computer-compatible high-resolution measurement of millisecond type transients is required.

SPECIFICATIONS
CAMAC Models 8212A and 8212A/8
SIMULTANEOUS SAMPLING DATA LOGGERS

INPUT CHARACTERISTICS

Analog Inputs:	32 differential, Lemo connectors, direct coupled 1MΩ input impedance.
Active Inputs:	The number of active inputs is programmable in binary steps. The number of active inputs can be programmed as either 4, 8, 16 or 32 for the 8212A, and 1, 2, 4 or 8 for the 8212A/8.
Bandwidth:	3 dB—50 kHz.
CMRR:	Comon Mode Rejection Ratio: 66 dB (DC—500 Hz), greater than 40 dB at 5 kHz.
Cross Talk:	66 dB isolation or better between any two channels, from DC to 500 Hz, greater than 40 dB at 5 kHz.
Overvoltage Protection:	± 140 V DC or 115 V rms at 60 Hz across: input pins, or either pin with respect to ground.

ADC CHARACTERISTICS

Full-Scale Range:	± 5 V full-scale. 0 to + 10 V or 0 to − 10 V full-scale is available as a factory installed option.
Resolution:	ADC resolution is 12 bits (0.025% of full scale with ± ½ LSB relative accuracy).
Gain Accuracy:	Maximum channel-to-channel variation is ± 0.1% and stable within ± 0.2% over a 10°C to 40°C range.
Non-Linearity:	Integral non-linearity ± ½ LSB.
Conversion Time:	The output of the front end track-and-holds are converted sequentially. Total conversion time is approximately the number of active channels times 5.5 μsec. During conversion, the data is presented to the memory port for transfer to LeCroy Model 8800A Memory modules.

FRONT-PANEL CONTROLS

Busy:	LED lit indicates conversion is in progress.
Stop Trig:	Lemo connector, 510 Ω, TTL compatible, edge sensitive.
Ext. Clock:	Lemo connector, 510 Ω, TTL compatible, edge sensitive.

SAMPLING RATE

Sampling is governed either by a fixed set of seven sampling frequencies available from internal clocking circuitry, an external clock input, or individual commands from the CAMAC dataway (see F(27)). The sampling frequencies in the table below are available under program control (see F(17) under CAMAC commands). Alternatively, an external clock can be supplied via a front-panel connector. Note that in certain instances higher sampling rates are achievable in the 8218A/8 by using an external clocking source, such as the LeCroy Model 8501.

Number of Active Inputs	8212A Internal Clock	8212A/8 Internal Clock	8212A or 8212A/8 External Clock
1	—	100 kHz	DC to 100 kHz
2	—	50 kHz	DC to 80 kHz
4	40 kHz	25 kHz	DC to 40 kHz
8	20 kHz	12.5, 5.0, 2.5, 0.5 kHz	DC to 20 kHz
16	10 kHz	—	DC to 10 kHz
32	5, 2, 1, 0.2 kHz	—	DC to 5 kHz

READOUT

Internal memory: Before or during any scan, the 8212A may be switched to the Single Scan mode with a CAMAC F(19), which causes a LAM to be generated when conversion is complete. The internal memory may then be read at the maximum CAMAC rate.

External Memory: After the stop-trigger and post-trigger samples, the 8212A automatically enters the data output mode. A single channel may be selected (see F(16) of CAMAC commands) where the time between reads is approximately 0.6 usec times the number of active channels. Q = 1 indicates a valid read, Q = 0 indicates data is being read too quickly. Alternatively, the Data Streaming mode may be used in which successive locations in memory are read at the maximum CAMAC rate with the data from all active channels interlaced.

OUTPUT PORT

TTL data levels; one 40-conductor cable (Model DC 8800); consists of 12 data lines, 12 ground, 7 control lines, and 7 grounds. Output is compatible with LeCroy Model 8800A 32K Memory module. Up to four Memory modules may be used with one 8212A.

CAMAC COMMANDS

L: A LAM is generated at the end of the next conversion following the F(19) Single Scan command. A LAM is generated 7 μsec following the final conversion after a stop-trigger and post-trigger scans. A LAM is also generated following the reading of external memory.

Z or C: Resets into the Sweep-and-Log mode.

Q: A Q = 1 response is generated for valid F(0), F(1), and F(2) reads and also for a test LAM, F(8), if the LAM is set. When F(2) readout is used, Q = 1 will be generated until the last word from the selected channel is read. The next read will generate a Q = 0 response, facilitating DMA transfers. The size of the available memory must be programmed by a switch, having been determined by the number of memory modules attached.

X: An X = 1 (command accepted) response is generated when a valid F, N, and A command is applied.

F(0): Read data from inputs 1-16; requires "A"; A(0) through A(15) are used for channel addresses.

F(1): Read data from inputs 17-32; requires "A"; A(0) through A(15)are used for channel addresses.

F(2): Read successive values from each channel onto the dataway; requires F(16). If input 33 is selected with F(16), initiating the Data Streaming mode, subsequent F(2)'s will read successive memory words (interlaced data) at up to the maximum CAMAC rate.

F(3): Read function data back to computer. Same data written with F(17).

BIT PATTERN

CAMAC	Post-trigger Scans			Clock Frequency			Number of Channels	
	2^2	2^1	2^0	2^2	2^1	2^0	2^1	2^0
F(17)	W8	W7	W6	W5	W4	W3	W2	W1
F(3)	R8	R7	R6	R5	R4	R3	R2	R1

F(8): Test LAM, Q response if a LAM is being generated, even if the CAMAC L line is disabled.

F(9): Resets into the Sweep-and-Log mode.

F(10): Reset LAM.

F(11): Re-enable the Sweep-and-Log mode. Used only after the LAM generated by the F(19) Single Scan command. The data in external memory remains valid unlike the result of C, Z, and F(9) resets.

F(16): Load data from write lines into channel select memory. Used to select a single channel and have the data read from it in chronological order. Values of n-1 select channel number n.

F(17): Writes function data into module (see F(3)).

F(19): Enables the Single-Scan mode, causing a LAM at the end of the next scan. F(0) and F(1) reads are then valid.

F(24): Disable the CAMAC L line. LAM's can still be detected using F(8).

F(25): Generates a Stop Trigger.

F(26): Enable LAM.

F(27): When the external clock is enabled, instead of using an external clock, a single clock pulse can be generated using F(27) and S2.

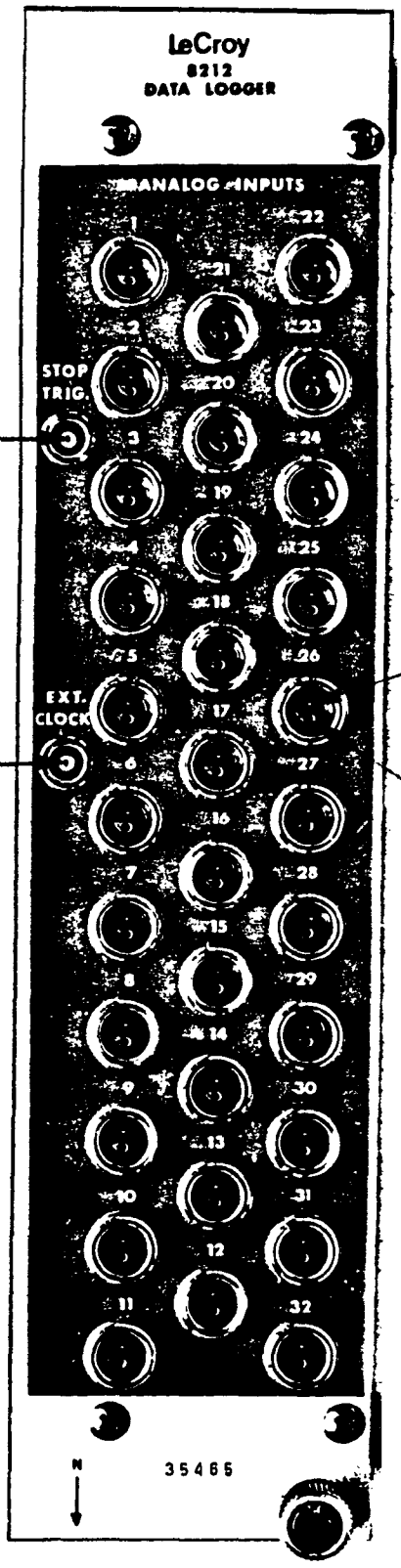
GENERAL

Packaging: In conformance with CAMAC standard for nuclear modules European ESONE Committee Report EUR4100e or IEEE standard #583). RF-shielded CAMAC #3 module.

Power Requirements:

1 A at + 6 V	325 mA at − 6 V
310 mA at + 24 V	240 mA at − 24 V

FRONT PANEL PHOTOGRAPH AND DESCRIPTION



Stop Trigger Input:
Normal Voltage = Ground

Stop Trig. Voltage = +5V
Lemo Connector

External Clock Input:
Clocks on the Rising
Edge of a TTL Pulse

Non-inverting (+) input

Differential Lemo
Connectors

Inverting (-) input

Front Panel Inputs

8212 TECHNICAL INFORMATION

OPERATIONAL DESCRIPTION

a. General

The LeCroy Model 8212 analog to digital converter can simultaneously sample up to 32 voltages at the 32 differential inputs; convert these voltages to 12 bit binary numbers and then store the data in internal memory, and the external LeCroy 8800/12 memory modules. Using just the internal memory, the 8212 can store one sample from each channel.

There is a trade-off between the Number of Samples (NOS) stored, the Number of Channels (NOC) converted and the maximum sampling frequency (CLK). The NOC is CAMAC settable to 4, 8, 16, or 32 active inputs. The maximum sampling frequency is 40, 20, 10, or 5 KHz for 4, 8, 16, or 32 channels respectively. The Number of Samples (NOS) per channel is given by:

$$NOS/CH=(32768/NOC)\cdot NOM$$

where NOM = the number of 8800/12 memory modules (0-3). (Each memory module has a capacity of 32768 words).

b. Front Panel

The front panel contains 32 differential LEMO connectors and 2 single conductor LEMOS; control and data are written and read over CAMAC.

Stop Trigger

The memory modules are organized as a circular shift register. After the memory is filled, further readings are written over initial readings (see Fig. 1).

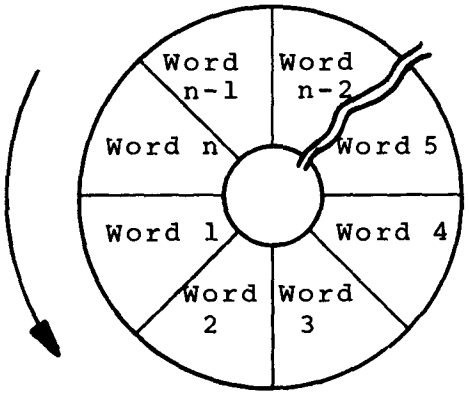


Fig. 1

A stop trigger can be generated by a TTL high level through the front panel STOP TRIG. LEMO connector or by executing a CAMAC F(25). After the stop trigger, the 8212 counts the CAMAC settable number of Post-Trigger Samples (PTS) and then prepares for data readout by executing the LAM mode that has been CAMAC selected. In order to make sure the memory has completely filled up, the following time must be waited after a Reset before giving a Stop Trigger:

$$T_{cycle} = 32768 \cdot NOM/(NOC \cdot CLK)$$

where CLK = sample clock frequency,
NOM = number of memory modules, and
NOC = number of channels.

External Sample Clock

Each sample clock causes the data to be measured and stored in both internal and external (8800/12) memory. The memory internal to the 8212 stores only one sample (up to 32 words).

A number of CAMAC settable clock frequencies (CLK) 0.2, 1, 2, 5, 10, 20, and 40 kHz are available to control the sampling rate. If these frequencies are insufficient or importance sampling is desired, a TTL CLOCK (Positive edge triggered) may be applied to the EXT. CLOCK LEMO on the front panel with the internal clock set by CAMAC to external. When the external clock is selected, samples can be clocked on F(27) at the first edge of CAMAC strobe S2 provided that the EXT. CLOCK LEMO is not left pulled to TTL high. With importance sampling, the time between samples must always exceed or equal the period of the maximum allowable sampling frequency.

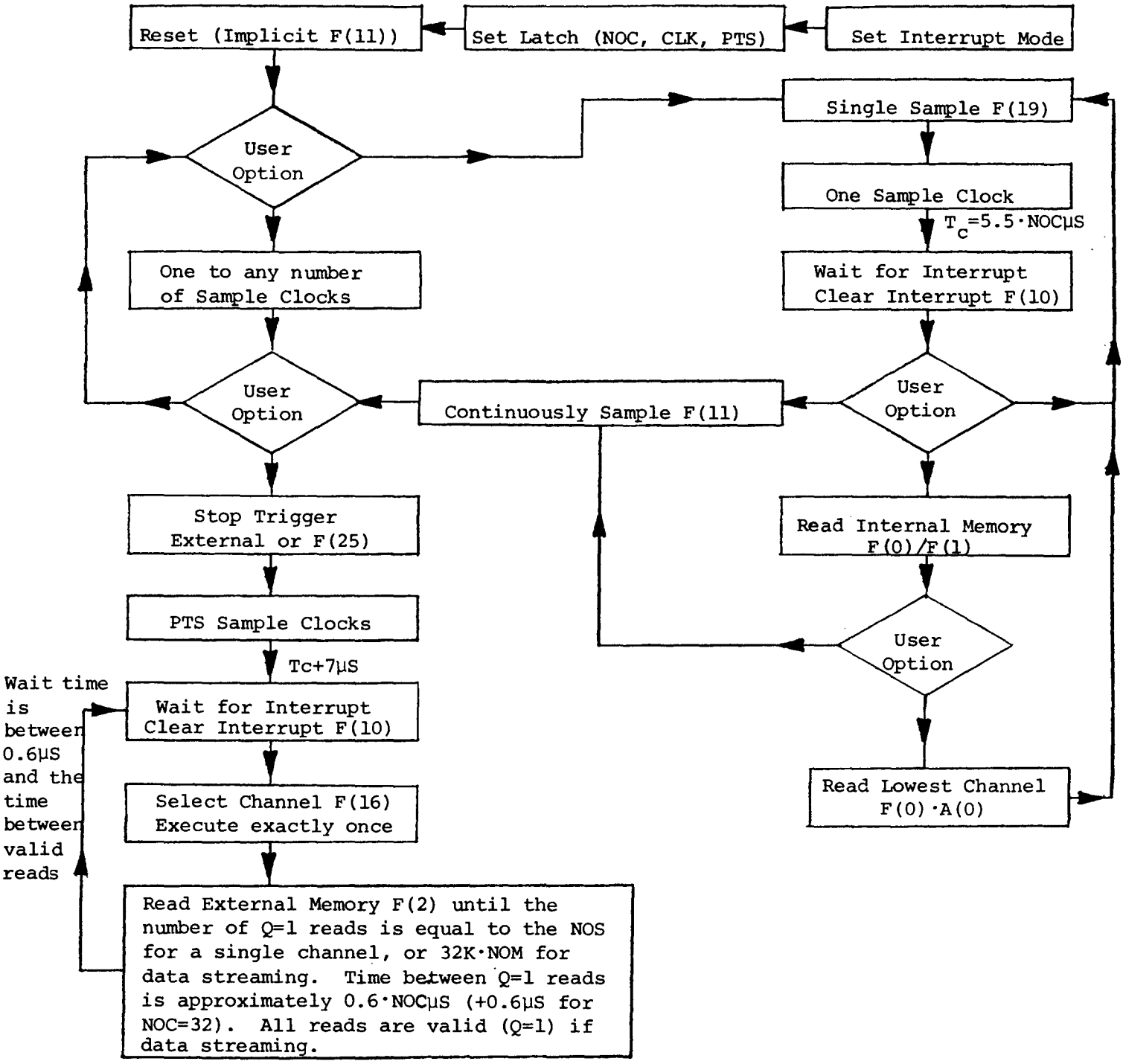
Analog Inputs

The front panel contains a differential LEMO input for each of the 32 channels. The + inputs and the - inputs are marked in Section 1. The unipolar model measures the difference between the + and - inputs in the range of 0-10 volts while the bipolar model measures differences in the range of -5 to +5 volts. In both cases the voltage is converted to a number that increases linearly with voltage from 0 for the lowest voltage to 4095 for the highest voltage, i.e., binary conversion in the unipolar model and offset binary conversion in the bipolar model. Thus a one count increase in data represents a voltage increase of 2.442 millivolts. The absolute maximum input voltages are ±100 volts. To guarantee the accuracy of the measurements, the inputs must be kept in the range of ±20V.

ENGINEERING DEPARTMENT
LeCroy / CALIFORNIA
PALO ALTO, CALIFORNIA

8212 GENERALIZED FLOW DIAGRAM

(Commands are described in the section following)



The top three boxes max be returned to at any time at user option. The source of the Sample Clocks may be internal, external, or the CAMAC Clock. Conversion time (T_C) is given by 5.5·NOCμS. The times given are approximate and vary by several microseconds from cycle to cycle. Data streaming is the sequential reading of every word in external memory.

Figure 3

8212A PROGRAMMING SEQUENCE

The following example shows how to program the 8212A for 32 channel, 5KHz operation. The sequence records 32 simultaneous transients in the external 8800/12 memory and then reads the data into the computer.

NOTE: (N, F, A, W) denotes a CAMAC command where:

N= station number

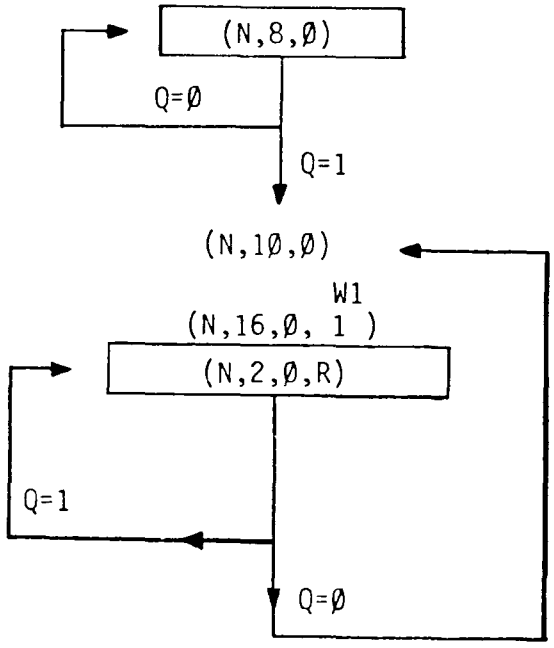
F= CAMAC F code

A= CAMAC A code

W= Data on the CAMAC write lines if a write op. is performed. -(N,F,A,R) denotes same as above except R is the data on the CAMAC read lines if a read op. is performed.

Sequence:

(N,17, Ø	W5 1 0 0 1 W1 1) R5 R1	Program unit for 32 channel, 5KHz and PTSL = Ø.
(N,3,Ø	1 0 0 1 1)	Verify the above step,
(N,9,Ø)		Start digitizing.



Test for the end of conversion due to a stop trigger.

Reset the LAM.

Select channel two to be read.

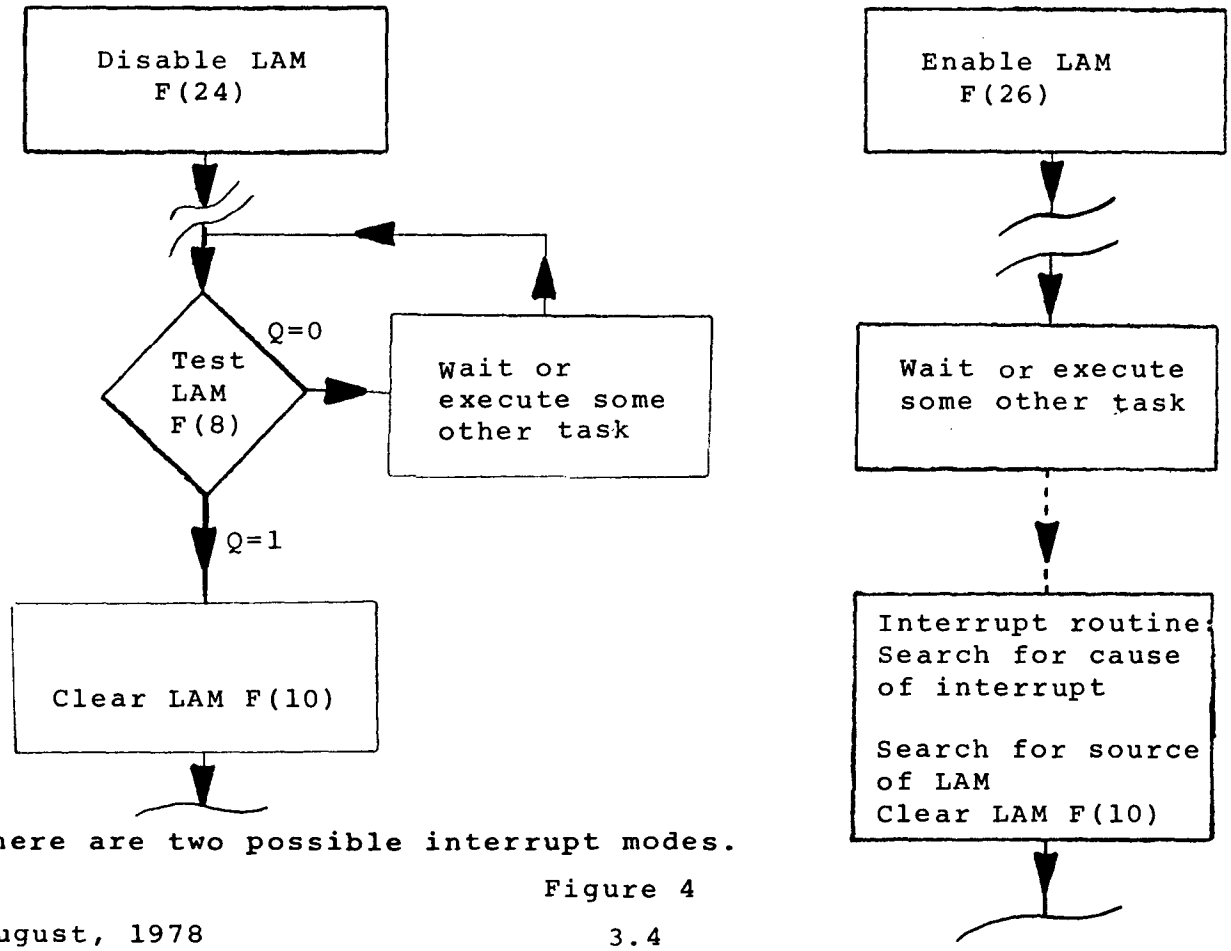
Read data 1024 times (same as reading until Q=Ø).

c. CAMAC Control

All CAMAC functions require N and a X=1 response is returned for valid commands. A more complete description of the CAMAC system standard is given later in this manual.

Interrupt-Look At Me (LAM)

The 8212 has two methods of indicating that conversion is complete. The LAM can be enabled, F(26), causing the CAMAC L line to fire when N is deselected for the 8212. If the LAM is disabled, F(24), completed conversion can be detected by a Test LAM F(8) which returns a Q=1 response if the interrupt circuitry has been activated whether or not the LAM is Enabled or Disabled. If the Test LAM returns a Q=1 response with the LAM Disabled, and the LAM is then Enabled, the CAMAC L line will fire. Always clear the LAM after detection. The LAM is cleared by a CLEAR LAM, F(10), or by one of the resets (see Reset section). The LAM Enable/Disable is not affected by a Reset.



There are two possible interrupt modes.

Figure 4

Set Latch (NOC, CLK, PTS)

The Number of Channels (NOC), Clock Frequency (CLK), and number of Post-Trigger Samples (PTS) are all set by an eight bit word written on the CAMAC write lines with a Set Latch F(17) command. The data written into the latch can be read with the Read Latch F(3) command. The bit patterns are shown in the following diagram.

F(17	W8	W7	W6	W5	W4	W3	W2	W1
F(3)	R8	R7	R6	R5	R4	R3	R2	R1
	PTS			CLK			NOC	

The binary number representing the NOC is given by 0, 1, 2, 3 for 4, 8, 16, 32 channels respectively. The CLK representation is 0, 1, 2, 3, 4, 5, 6, 7 for External Sample Clock, 0.2, 1, 2, 5, 10, 20, 40 kHz respectively.

If the external clock is selected, not only can samples be clocked using the front panel connector, but also samples can be clocked on the first edge of CAMAC strobe S2 during execution of F(27) only if the front panel EXT. CLOCK connection is not pulled to TTL high voltage by some external source.

The maximum recommended Sample Clock Frequency (CLK) is given by:

$$CLK \leq 160 \text{ kHz/NOC}.$$

In selecting NOC and CLK it is useful to remember that although the total number of stored readings is constant for a given number of memory modules, the Number of Samples (NOS) stored is dependent on the NOC:

$$NOS = 32768 \cdot NOM/NOC$$

where NOM=Number of 8800/12 Memory Modules.

ENGINEERING DEPARTMENT
LeCroy/CALIFORNIA
PALO ALTO, CALIFORNIA

NOC	W2 R2	W1 R1
4	0	0
8	0	1
16	1	0
32	1	1

NOTE: CAMAC lines are inverted so that a "1" is represented by zero volts.

SAMPLE CLOCK	W5 R5	W4 R4	W3 R3
External	0	0	0
0.2 KHz	0	0	1
1 KHz	0	1	0
2 KHZ	0	1	1
5 KHz	1	0	0
10 KHz	1	0	1
20 KHz	1	1	0
40 KHz	1	1	1

Bit settings for NOC, and CLK are summarized in these tables. These bit values are written/read with Write/Read Latch F(17)/ F(3) commands. These commands also control the Post-Trigger samples (PTS).

PTS is dependent on the Number of Memory modules (NOM) switches which are located in a small package on the digital board at position 2I and are accessible through a cutout on the side panel. The NOM switch must be set to the correct position or the data will become confused when read out. The PTS are counted by a pre-settable 16 bit counter that disables the sampling and switches to the readout mode when it counts to a number equal to 32768·NOM/2. The PTS counter begins counting on a Stop Trigger. Thus the PTS is dependent on the number the PTS counter is pre-set to which is designated PTSC:

$$PTS=(32768\cdot NOM/2) - PTSC.$$

The PTS must be set to 1 or greater or the 8212 will switch to the readout mode without a Stop Trigger. Thus the PTS is settable over a range from 1 (virtually all pre-trigger samples) to 32768·NOM/2. Although the PTS counter is 16 bits, it is settable by only the three bits W8, W7, and W6, which are called PTSL when output from the latch. These three latch bits must be connected to the 16 PTS bits on a jumper plug that plugs into a jumper socket on the digital board at position 1H and is accessible through a cutout in the side panel. The pin numbers of the jumper socket increase in a counterclockwise direction and pin 1 is located in the upper left hand corner. The identification of the pins is given on the following charts:

PTSL (outputs) bits	2^2	2^1	2^0
Jumper socket (1H) pin#	3	2	1

PTSC (inputs) bits	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	$2^{6}2^{5}2^{4}$	$2^{3}2^{2}2^{1}2^{0}$
Jumper (1H) pin #	6	11	12	13	14	15	16	8	10	all to 5	all to 7

Pin 9 is ground (a source of binary 0).

Pin 4 is +5 volts (a source of binary 1).

The PTSL pins are low impedance output voltages and should not be connected together or to +5 volts or ground. The PTSC pins are inputs and may be connected together and connected to an output voltage.

Judicious selection of the jumpers is necessary to optimize the versatility of the 8212 for a particular application. For all Post Trigger Samples, the PTS must be set equal to the Number of Samples (NOS),

$$PTS = NOS.$$

Substituting in the previous two equations gives

$$(32768 \cdot NOM/2) - PTSC = 32768 \cdot NOM/NOC$$

which becomes

$$PTSC = 32768 \cdot NOM \cdot (1/2 - 1/NOC).$$

For all Pre-Trigger Samples set PTS=1 so that:

$$PTSC = (32768 \cdot NOM/2) + 1.$$

Note that for all Pre-Trigger Samples, the PTSC setting depends only on the NOM, while for all Post-Trigger Samples, the PTSC is also dependent on the NOC. Various header connections are listed in Appendix A.

Example: The 8212 is to be used with 1 8800/12 memory module, and it is desired to have all pre-trigger and all post-trigger samples for each NOC setting. Substituting into the equation for all Pre-Trigger Samples, we find that:

$$PTSC = 16383 = 0011,\ 1111,\ 1111,\ 1111_2.$$

Substituting into the equation for all Post-Trigger Samples gives:

PTSC= 8192=0010, 0000, 0000, 0000_2 for 4 channels,

PTSC=12288=0011, 0000, 0000, 0000_2 for 8 channels,

PTSC=14336=0011, 1000, 0000, 0000_2 for 16 channels, and

PTSC=15360=0011, 1100, 0000, 0000_2 for 32 channels

It is impossible to achieve all 5 of these PTSC options with the three PTSC bits available. However, a nice compromise can be achieved by making the following connections:

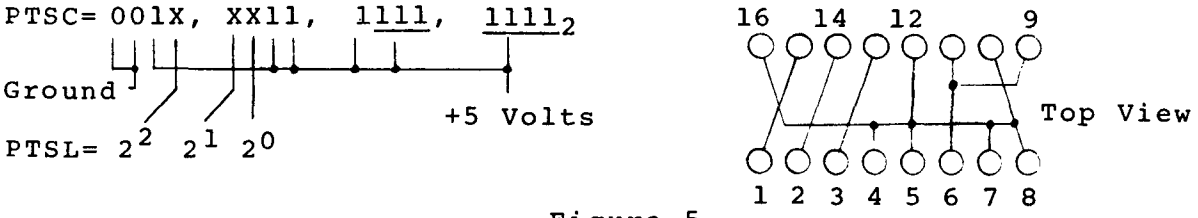


Figure 5

The jumper plug is wired with pins 6 and 11 connected to pin 9, pins 12, 16, 8, 10, 5 and 7 connected to pin 4, pin 13 connected to pin 3, pin 14 connected to pin 2, and pin 15 connected to pin 1. Of course, since only one memory module is used, switch 1 of the NOM switch is turned on while switches 2, 3 and 4 are turned off.

In order for the PTS to decrease monotonically as the PTSL increases, each PTSL bit must be connected to a PTSC bit that is higher than every PTSC bit that is connected to a less significant PTSL bit. In order that the PTS change in equal increments, the sum of the PTSC bits connected to PTSL bit must be twice the similar sum for the next less significant PTSL bit. In order that no two PTSL counts result in almost equal PTS's, it is recommended that each PTSL bit should be connected to a sum of PTSC bits whose total value is greater than or equal to the total PTSC value connected to the next less significant bit.

Reset (initialization) C, Z, or F(9)

The C, Z, or F(9) commands are completely equivalent except that C and Z do not return a X=1 response since they are not CAMAC functions. The reset removes the 8212 from the readout mode and also performs an implicit F(11) (see Continuously Sample) causing the system to continuously sample and store. A reset clears the LAM although it does not affect the Enable/Disable LAM interrupt modes. The reset does not change the contents of the NOC, CLK, PTS latch. A reset is the only way to enable the sample clock after the Post-Trigger Samples (PTS) have been counted out following a Stop Trigger. The data is invalidated by a Reset.

Single Sample F(19)

The Single Scan F(19) function causes the sample clock to be disabled at the end of the next scan and then causes an interrupt (LAM). The interrupt will occur approximately 5.5·NOC microseconds after the sample clock.

The sample clock can be re-enabled for just one sample by a Single Sample F(19) command or for many samples by Continuously Sample F(11) or Reset commands. Of course a Reset will invalidate previous data. However, F(19) and F(27) will not always enable the sample clock since after a Stop Trigger and PTS samples, only a Reset will enable the clock. Use of F(19) after a Stop Trigger should be avoided since it may be impossible to determine which command caused the ensuing interrupt.

Continuously Sample F(11)

A F(11) will cause the 8212 to keep the sample clock enabled until a Single Sample F(19) command, a Reset or Stop Trigger and PTS samples. After a Stop Trigger and PTS samples, only a Reset will enable the sample clock. A Reset also does everything done by a Continously Sample command F(11). The F(11) command also resets the channel counter, a necessary step if further samples are to be taken after reading internal memory.

CAMAC Sample Clock F(27)

With the CLK Latch set to external and the front panel EXT. CLOCK disconnected, a sample can be clocked on the first edge of CAMAC signal S2 during a F(27) CAMAC cycle. If the EXT CLOCK LEMO is held at TTL high, the CAMAC clock is disabled.

Read Internal Memory F(0), F(1)

Following the interrupt caused by a Single Sample F(19) Command, the internal memory may be read at the maximum CAMAC speed. If the commands have been executed in proper order, a Q response will be returned during Internal Memory Reads F(0), F(1) indicating that the data read is valid. Channels 1 through 16 are read by F(0) with the CAMAC subaddress set to one less than the channel (CH) to be read. Channels 17 through 32 are read by F(1) with the CAMAC subaddress set to 17 less than the channel (CH) to be read. Thus to read channel CH, execute the CAMAC function also given by:

$$F(INT(CH/17))\cdot A((CH-1)-INT(CH/17))$$

READING INTERNAL MEMORY

Channel	Command	Channel	Command
1	F(0)·A(0)	17	F(1)·A(0)
2	F(0)·A(1)	18	F(1)·A(1)
3	F(0)·A(2)	19	F(1)·A(2)
4	F(0)·A(3)	20	F(1)·A(3)
5	F(0)·A(4)	21	F(1)·A(4)
6	F(0)·A(5)	22	F(1)·A(5)
7	F(0)·A(6)	23	F(1)·A(6)
8	F(0)·A(7)	24	F(1)·A(7)
9	F(0)·A(8)	25	F(1)·A(8)
10	F(0)·A(9)	26	F(1)·A(9)
11	F(0)·A(10)	27	F(1)·A(10)
12	F(0)·A(11)	28	F(1)·A(11)
13	F(0)·A(12)	29	F(1)·A(12)
14	F(0)·A(13)	30	F(1)·A(13)
15	F(0)·A(14)	31	F(1)·A(14)
16	F(0)·A(15)	32	F(1)·A(15)

ENGINEERING DEPARTMENT
LeCroy/CALIFORNIA
PALO ALTO, CALIFORNIA

where INT(X) = the greatest integer less than or equal to X. For example to read channel 22 execute F(1)·A(5). The channels may be read any number of times in any order except that if further samples are to be taken, the internal channel counter must be reset by reading the lowest channel F(0)·A(0), executing a continously Sample F(11) command, or executing a Reset.

Stop Trigger F(25)

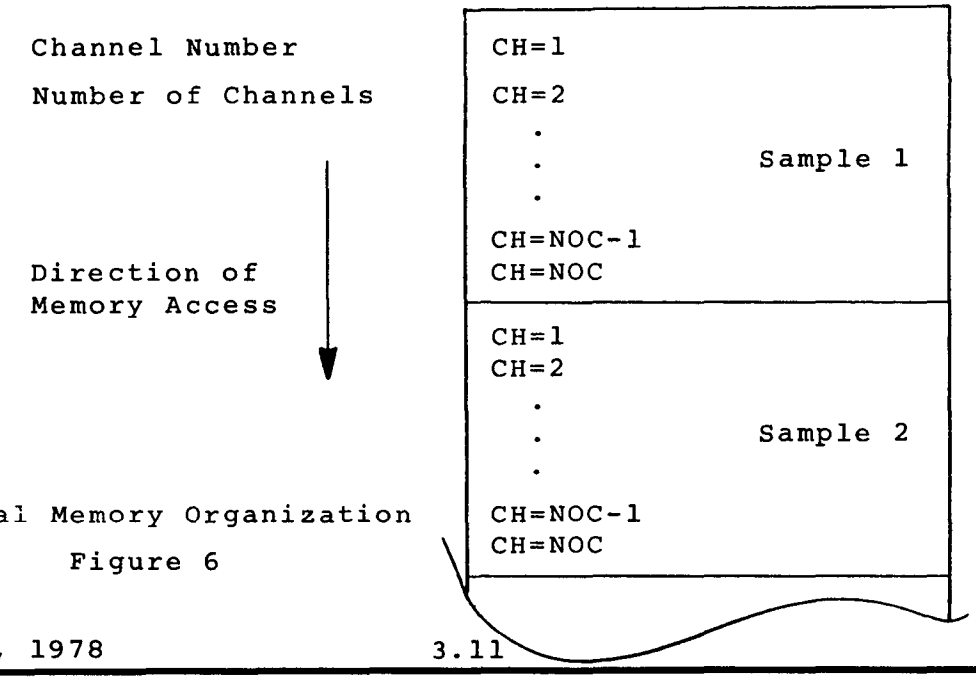
A Stop Trigger is caused by CAMAC strobe S2 during execution of a Stop Trigger F(25) command. This command is identical to, but independent of the front panel STOP TRIG. (See Front Panel Section). An interrupt is generated PTS samples (see Latch Section) after the Stop Trigger to indicate that the 8212 is ready for a Channel Select F(16) command in preparation for reading out the external 8800/12 memory modules. The interrupt occurs approximately 5.5·NOC+7 microseconds after the final Post Trigger Sample. At least one Sample Clock must be executed before a Stop Trigger. Use of the Single Sample F(19) command after a Stop Trigger should be avoided since it may be impossible to determine which command caused the ensuing interrupt.

Channel Select F(16)

Channel Select F(16) is used before reading external memory. A Channel Select should be executed only once after the interrupt following a Stop Trigger or a previous scan of external memory. The external memory is loaded with NOC number of words each sample clock.

CH = Channel Number

NOC = Number of Channels



External Memory Organization

Figure 6

The memory can be read two ways; the data from only one channel can be read or the entire memory can be read sequentially. Reading the entire memory is faster (see the following Read External Memory F(2) Section) but the data from each channel is read sequentially before the next chronological sample is read. To select a single channel and have the data read in chronological order, simply execute a Channel Select F(16) command with one less than the channel number to be read loaded onto the CAMAC write bus. To prepare for the sequential readout of every word in external memory (data streaming), execute a Channel Select F(16) command with the write bus set at any number between 32 and 63 inclusive. Adding any multiple of 64 to the setting of the CAMAC write bus for a Channel Select F(16) instruction will cause no change.

Read External Memory F(2)

After the Channel Select, the external memory 8800/12 module(s) may be read by executing F(2)s. The 12 bits of data will be returned on the CAMAC read bus (R1-R12). Reading the data invalidates the data until it is updated. Executing F(2) before the data is updated will result in no Q response (Q=0), indicating that the data is invalid because it has not yet been updated. When the data is valid, a Q response will be returned. If every word of external memory is to be sequentially read, the data can be read at the maximum CAMAC rate with valid data (Q=1) returned on every F(2) read. If however a single channel is selected, approximately 0.6·NOCμS (+0.6μS for NOC=32) will elapse between valid reads.

After the memory is scanned, the 8212 generates an interrupt which must be followed by a Channel Select F(16) or a Reset. The time between the Channel Select and the first valid read, and the time between the final valid read and the interrupt, depend on the channel selected and are between 0.6μS and the time between valid reads. The times given above vary by several microseconds from cycle to cycle.

The number of valid reads included in a memory scan is equal to the Number of Samples (NOS) when a single channel is selected and is equal to the number of words of memory (=32768·NOM) when every word of memory is read sequentially. Do not execute a Channel Select until the data previously selected has been read. After the data has been read, further reads will have no Q response. During all reads, the most significant bit of the data is read on R12 and the least significant bit is read on R1.

This page is for the 4, 8,and 16 channel version ONLY

ADDENDA:

This manual also describes the operation of models 8212A/4, 8212A/8 and 8212A/16. These units differ from the 8212A with respect to the available sampling frequencies and the number of active channels. The master oscillator frequency for units other than the 8212A is 100KHz.

Programming the sampling frequency for the 8212A/4,8 and 16 is given by the following table (replaces table on page 3.6).

SAMPLE CLOCK	W5 R5	W4 R4	W3 R3
EXTERNAL	0	0	0
.5KHz	0	0	1
2.5KHz	0	1	0
5KHz	0	1	1
12.5KHz	1	0	0
25KHz	1	0	1
50KHz	1	1	0
100KHz	1	1	1

NOTE:

a) 100KHz used only in the 1 channel mode.

b) 50 KHz used only in the 1 or 2 channel mode.

c) 25 KHz used only in the 1, 2, or 4 channel mode.

d) 12.5 KHz used only in the 1, 2, 4 or 8 channel mode.

Programming the number of active channels for the 8212A/4,8 and 16 is given by the following tables (replaces table on page 3.6).

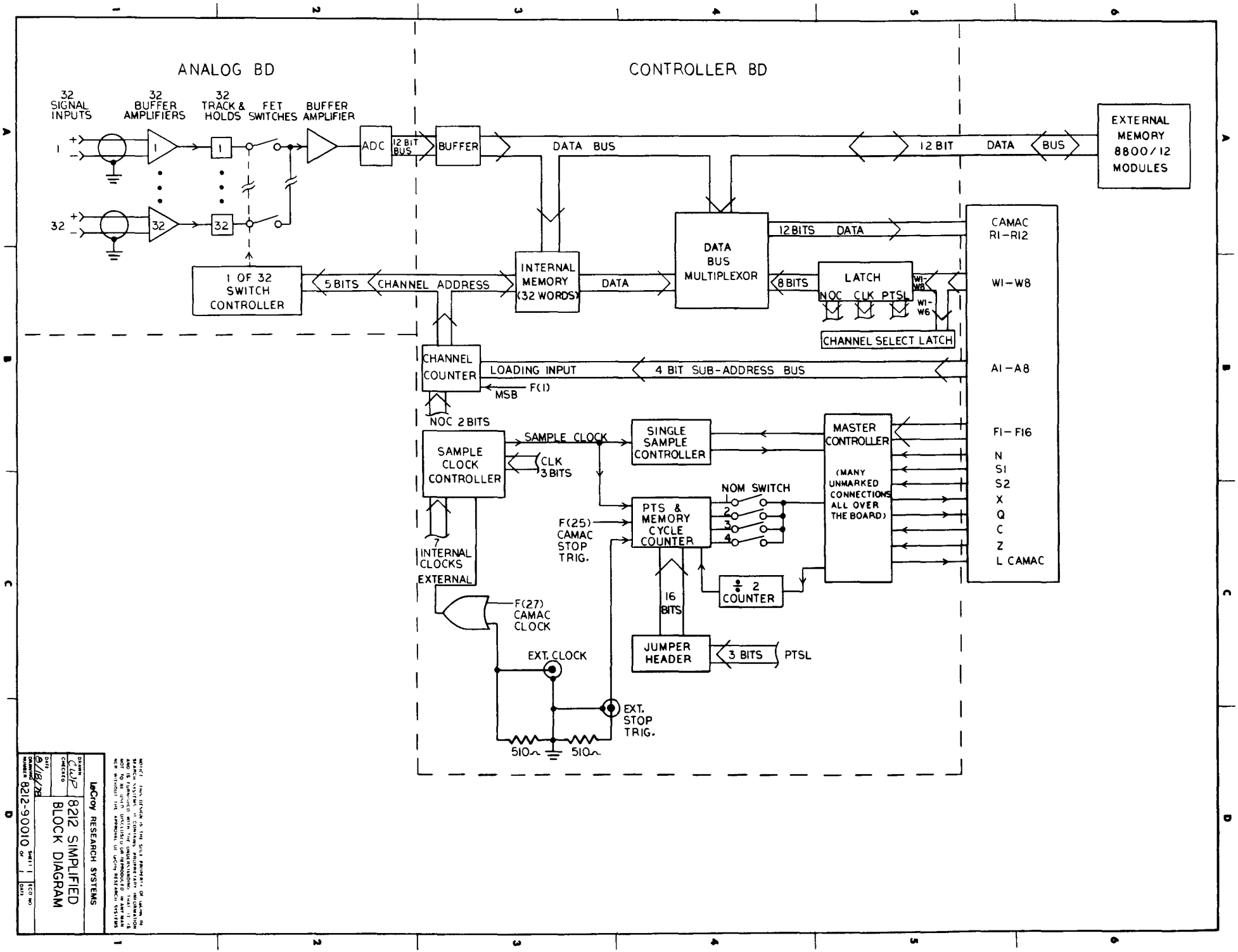
8212A/4 & 8212A/8

NOC	W2 R2	W1 R1
1	0	0
2	0	1
4	1	0
8	1	1

8212A/16

NOC	W2 R2	W1 R1
2	0	0
4	0	1
8	1	0
16	1	1

Not Valid for 8212A/4



LeCroy RESEARCH SYSTEMS

DRAWN

CHECKED CWP

DATE 9/18/78

8212 SIMPLIFIED BLOCK DIAGRAM

DRAWING NUMBER 8212-90010 OF

SHEET 1

ECO NO

DATE

4. FUNCTIONAL DESCRIPTION

4a. General

The Model 8212 data logger is a 32 channel waveform digitizer. The 8212 is built on two boards, the analog board and the digital control board. The analog board contains 32 buffer amplifiers, 32 track and hold circuits, 32 FET switches, 1 of 32 channel decoding circuitry, and a successive approximation analog to digital converter (ADC). The controller board includes a CAMAC interface, data buses, internal memory, and logic circuitry for controlling the analog bd., the CAMAC interface, and external Model 8800/12 memory modules. These boards are described separately and in detail in the following sections. Refer to the preceding block diagram while reading the following sections. To simplify the block diagram, control wires are left out.

4b. ADC Board

1. Buffer Amplifiers: A balanced shielded cable connects each front panel differential LEMO to one of 32 buffer amplifiers which convert the signal from differential to single ended so that only this first stage need adjustment for common mode rejection. The buffer amplifiers also provide 1MΩ input impedance.

2. Track and Hold Circuits: The output of each buffer amplifier is connected to a track and hold circuit. The track and hold control signals are connected together so that the outputs simultaneously track the all input voltages or simultaneously store in the hold capacitors the input voltages applied at the instant the track/hold control signal was set to hold.

3. FET Switches and Address Bus Decoder: Each voltage stored in a hold capacitor is sequentially switched to the ADC by FET switches. At a given moment only one track and hold output is connected to the ADC by a 1 of 32 FET switch controller which decodes a 5 bit channel address and determines which channel is to be connected.

4. Buffer Amplifier: Following the FET switches is a high input impedance buffer amplifier which reduces the effect of the FET switches output impedance to a negligible level.

5. Analog to Digital Converter (ADC): The output of the buffer amplifier is connected to a 12 bit hybrid successive approximation ADC which converts the voltage to a 12 bit digital representation. The ADC accepts a convert pulse on the "convert" bus

and returns a pulse on the"dardy" bus when the data is ready.

6. Operation Sequence: When a sample is taken, the track and hold circuits are first set from track to hold. The control and channel decode logic then connects the output of the first track and hold to the high impedance buffer via the FET switches. After a short wait to allow transients to settle, the control logic issues a convert command to the ADC. When the ADC has finished its conversion, it issues a signal on the dardy line. The controller stores the ADC output in memory, switches the output of the next track and hold to the buffer, and the cycle repeats until the last channel voltage is converted and stored. The control logic then sets the track and hold circuits to the track mode and the sample is complete.

4c. Controller Board

1. Master Controller: The master controller co-ordinates timing, sequencing, and synchronization of virtually every section of the 8212. Most of the connections to the master controller are not shown on the simplified block diagram. The master controller decodes the CAMAC commands and co-ordinates the CAMAC timing with the possibly asynchronous task specified by the CAMAC command, asynchronous external memory refresh, reads, and writes, asynchronous Sample Clocks, and the Stop Trigger.

2. Single Sample Controller: When sampling is enabled by the master controller, the single sample controller operates the sequencing of the analog board as explained in part b. of this chapter. The single sample controller starts sequencing on a Sample Clock pulse and returns a signal to the master controller at the end of the sample.

3. Data Bus Multiplexing, Latch, Channel Select Latch: During sampling, the data flows from the ADC through a 12 bit buffer on the controller bd. and is simultaneously stored in both internal memory and external memory. The next sample is overwritten onto internal memory and stored in the next sequential locations of external memory. In the data bus multiplexor, a series of latches and buffers allow this data bus, the output bus of internal memory, or the output bus of the NOC, CLK, PTSL Latch, to be connected to the CAMAC read lines. In all reads, CAMAC bit R1 is the least significant bit. CAMAC write lines W1-W8 are connected to the NOC, CLK, PTSL Latch while only W1-W6 are used for the Channel Select Latch.

4. Sample Clock Controller: The sample clock controller decodes the 3 CLK bits from the Latch and selects 1 of 7 internal clocks or the external clock. As can be seen in the simplified block diagram, the CAMAC clock and the Ext. Clock front panel connector are connected through an inclusive OR gate to the external input of the sample clock controller. Thus if the Ext. Clock LEMO is connected to TTL high (logical true), the output of the OR gate will remain high regardless of the condition of the CAMAC clock function.

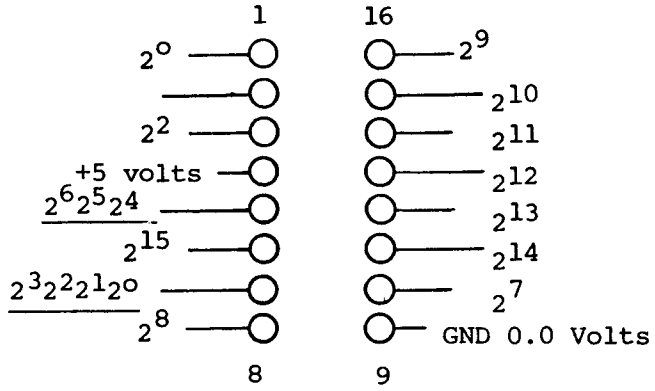
5. PTS and Memory Cycle Counter: The same counter is used to count the Post Trigger Samples and to keep track of the external memory address during external memory reads. Since the memory is cyclic, the absolute location of the data is ignored during conversion and storage, but it is necessary to indicate the end of a complete read of external memory. The NOM switches are numbered 1 through 4, and the switch corresponding to the NOM should be switched on while the other switches should be switched off, otherwise an improper number of reads will result and the data will be confused. The NOM switch setting also affects the PTS count. The counter only counts up to 32768·NOM/2 which is 1/2 the total memory size; the External Memory reads are first connected to a ÷2 counter so that the total number of reads counted is 32768·NOM. The 3 PTSL bits from the latch are connected via the jumper header to the 16 bit loading input of the PTS counter. The counter is loaded with the data at the loading inputs at the end of every sample that occurs before the Stop Trigger. If a Stop Trigger is executed before a sample is taken, the PTS counter will not be loaded with the information from the jumper header.

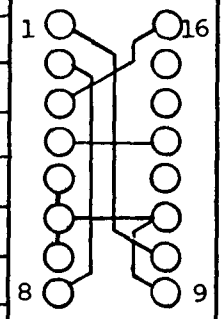
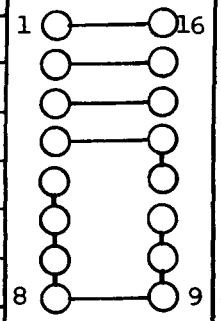
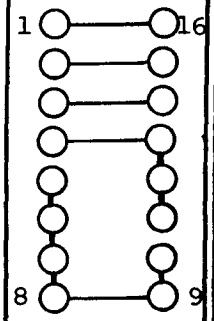
6. Channel Counter and Internal Memory: During sampling, the 5 bit channel counter provides the channel address used by the FET switch controller on the analog board. This same channel address is used by the internal memory. During F(0)/F(1) reads, the channel counter is loaded from the 4 bit CAMAC subaddress bus and the decoded F(1) signal which is connected to the MSB of the 5 bit channel counter. If further samples are to be taken after reading internal memory, the channel counter must be reset by executing a RESET, F(11), or reading the lowest channel F(0)·A(0). The CAMAC function F(19) can be executed in the middle of a sample and does not reset the channel counter.

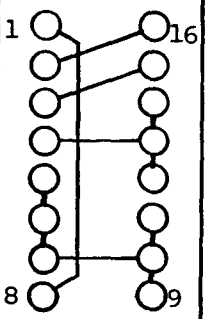
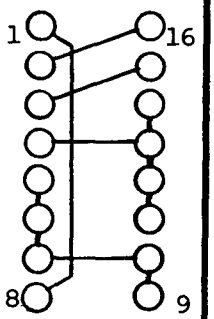
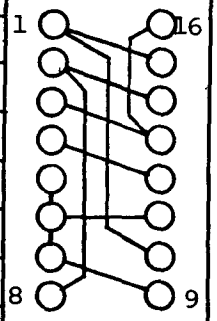
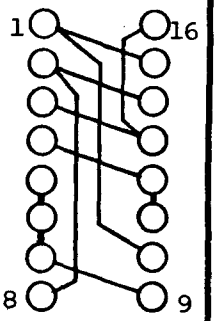
7. External Memory: The operation of the external memories is explained in Technical Information Manual Model 8800 Memory Module. However for convenience, Appendix B contains a chart showing the connections of the cable that runs from the 8212 controller board to the external memory modules.

APPENDIX A

Header connections for setting the PTS in equal increments.



PTSL	PTS	NOM=1	NOM=2
0	1024		TOP VIEWS
1	896		
2	768		
3	640		
4	512		
5	384		
6	256		
7	128		
0	4096		
1	3584		
2	3072		
3	2560		
4	2048		
5	1536		
6	1024		
7	512		

PTSL	PTS	NOM=1	NOM=2
0	2048		
1	1792		
2	1536		
3	1280		
4	1024		
5	768		
6	512		
7	256		
0	8192		
1	7040		
2	5888		
3	4736		
4	3584		
5	2432		
6	1280		
7	128		

NOM = (Number of Memories)

PTS = (Post Trigger Sample)

PTSL = (Post Trigger Scans)

Appendix C

LIST OF ABBREVIATIONS

CH = The channel number as written on the front panel of the 8212.

CLK = The sample clock frequency in Hertz.

NOC = The number of active channels (CAMAC settable to 4, 8, 16, or 32).

NOM = The number of 8800/12 memory modules used.

NOS = The number of samples (each sample includes NOC measurements).

PTS = The number of post-trigger samples.

PTSC = The 16 bit binary number loaded into the post-trigger sample counters preset inputs.

PTSL = A 3 bit number output by the latch used to control the PTSC via a strap option.

LeCroy 8212 header and switch setting explanation

John Wertenbaker 8/18/2005

The following is an explanation of the header and switch settings on the 8212 and 8800 memories.

The switches on the side panel of the 8212 reflect how many 8800 memory modules are to be connected. An 8212 can address 1, 2, 3, or 4 memory modules. The following chart describes the memory switch settings:

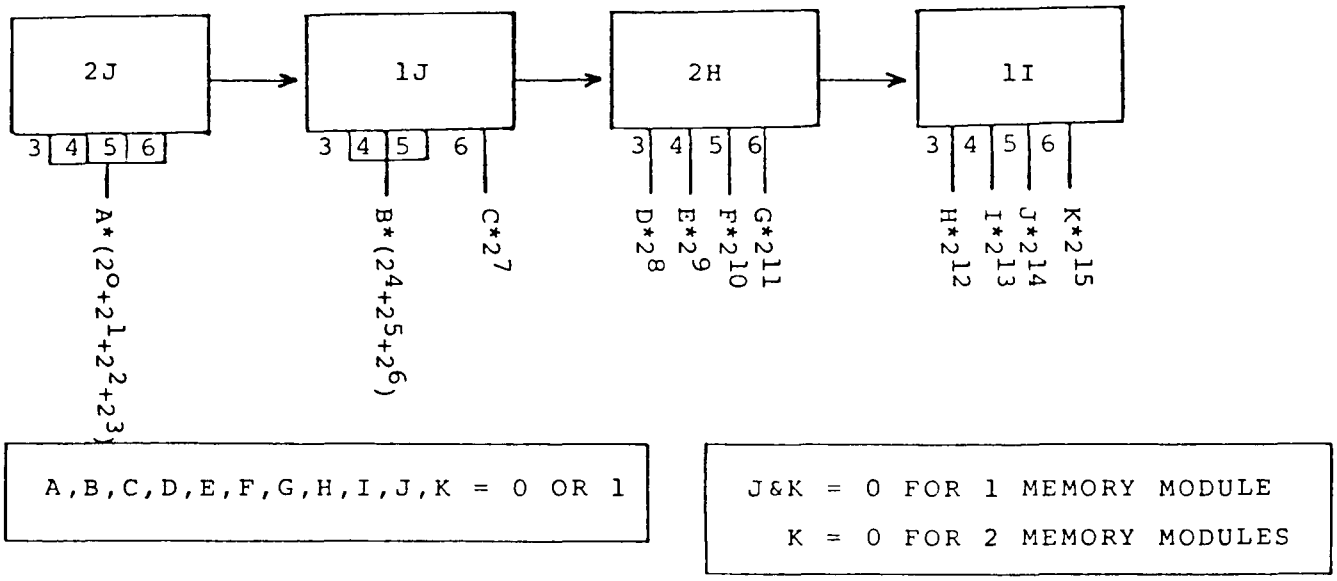
1 memory	2 memories	3 memories	4 memories
1 On	1 Off	1 Off	1 Off
2 Off	2 On	2 Off	2 Off
3 Off	3 Off	3 On	3 Off
4 Off	4 Off	4 Off	4 On

The jumper settings allow for many different configurations of memories and post-trigger sample counts. In the late 1970's, when this module was designed, it took many TTL chips to make these parameters programmable, and real estate on the 8212 module is at a premium. The jumpers were, at the time, the best compromise between functionality, cost, and size.

Refer to Figure 1 on Page 5.1 of this manual. The figure on the top of the page shows 2J, 1J, 2H, and 1I. These are the actual 74LS161 4-bit counter chips on the board. These counters are loaded with the selected number upon receipt of the "Stop Trigger" command. They then count up to "FFFF", and stop the module from digitizing further. The letters A through K are connected to the "counter load" inputs of those counters. These lines are brought out to the header. The header jumpers those inputs to either GND, +5V, or the PTS (Post Trigger Samples) control. The PTS control is made up of bits 6, 7, and 8 on the F(3) and F(17) CAMAC commands. Pins 1, 2 and 3 of the header are bits W6, W7, and W8 of the F(17) command, respectively. The PTS tables on pages 5.4, 5.5, and 5.6 indicate the number of Post Trigger Samples per channel that can be expected for each style of header. Each style has 8 possible combinations of the 3 PTS control bits, corresponding to 8 different numbers of Post Trigger Samples. Once a suitable style is selected, it can be built using the PTS tables and the bottom drawing on Page 5.1. A logic 1 is +5V, and a logic 0 is GND. The 6 pages after Page 5.6 of this manual show all 14 header styles with 1, 2, or 4 memory modules. It may be easier to refer to these drawings rather than figuring it out based on the PTS tables.

The 8212 must be connected to a number of 8800 modules. Recommended configurations are either 1, 2, or 4 memory modules. Each 8800 module is 32K words. Figure 2.2, which is taken from the 8800 Memory Module manual, shows the configuration of the 40-pin ribbon cable and the switch settings for the 8800 memory modules. This is the view from the front of the crate. The cuts refer to the top (or bottom) 2 wires on the cable, which must be cut in the places shown. The Controller is the 8212, or other LeCroy digitizers that are compatible with the 8800 memory module.

8212A PTS CONFIGURATION



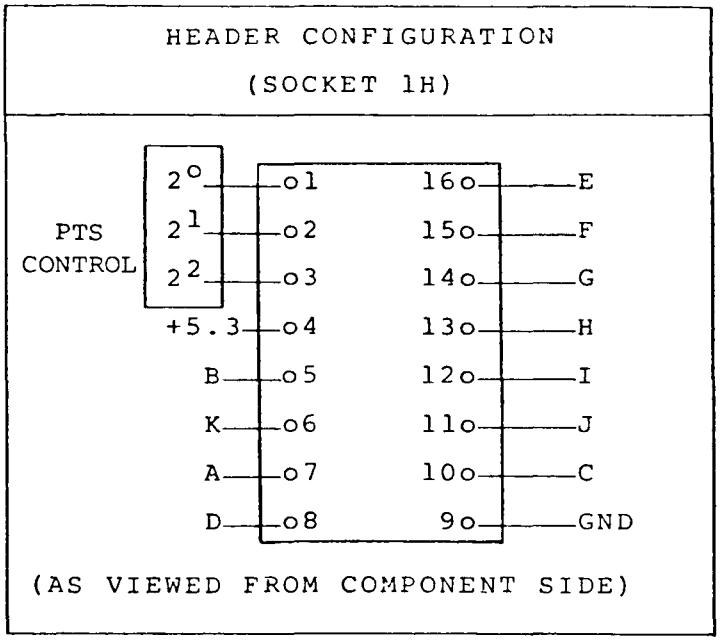


FIGURE 1

PTS TABLE

(ONE MEMORY - J&K = 0)*

1.

K	J	I	H	G	F	PTS CONTROL 2^2 2^1 2^0 E	D	C	B	A	PTS
0	0	1	1	1	1	0	0	0	0	0	1024
						0	0	1			8967
						0	1	0			7688
						0	1	1			6403
						1	0	0			5125
						1	0	1			3844
						1	1	0			2562
						1	1	1			1281

2.

K	J	I	H	G	F	PTS CONTROL 2^2 2^1 2^0 E	D	C	B	A	PTS
0	0	1	1	1	1	0	0	0	1	1	8975
						0	0	1			7691
						0	1	0			6413
						0	1	1			5137
						1	0	0			3859
						1	0	1			2574
						1	1	0			1296
						1	1	1			1

3.

K	J	I	H	G	PTS CONTROL 2^2 2^1 2^0 F	E	D	C	B	A	PTS
0	0	1	1	1	0	0	0	0	0	0	2048
					0	0	1				1792
					0	1	0				1536
					0	1	1				1280
					1	0	0				1024
					1	0	1				768
					1	1	0				512
					1	1	1				256

4.

K	J	I	H	G	PTS CONTROL 2^2 2^1 2^0 F	E	D	C	B	A	PTS
0	0	1	1	1	0	0	0	1	1	1	1793
					0	0	1				1537
					0	1	0				1281
					0	1	1				1025
					1	0	0				769
					1	0	1				513
					1	1	0				257
					1	1	1				1

5.

K	J	I	H	PTS CONTROL 2^2 2^1 2^0 G	F	E	D	C	B	A	PTS
0	0	1	1	0	0	0	0	0	0	0	4096
				0	0	1					3584
				0	1	0					3072
				0	1	1					2560
				1	0	0					2048
				1	0	1					1536
				1	1	0					1024
				1	1	1					512

6.

K	J	I	H	PTS CONTROL 2^2 2^1 2^0 G	F	E	D	C	B	A	PTS
0	0	1	1	0	0	0	1	1	1	1	3585
				0	0	1					3073
				0	1	0					2561
				0	1	1					2049
				1	0	0					1537
				1	0	1					1025
				1	1	0					513
				1	1	1					1

*FOR TWO MEMORIES, SET J=1, FOR SAME PTS AS SHOWN IN TABLES
FOR FOUR MEMORIES, SET J&K=1, FOR SAME PTS AS SHOWN IN TABLES

PTS TABLE

(ONE MEMORY - J&K=0)*

7.

K	J	I	PTS CONTROL 2^2 2^1 2^0 H	G	F	E	D	C	B	A	PTS
0	0	1	0	0	0	0	0	0	0	0	8192
			0	0	1						7168
			0	1	0						6144
			0	1	1						5120
			1	0	0						4096
			1	0	1						3072
			1	1	0						2048
			1	1	1						1024

8.

K	J	I	PTS CONTROL 2^2 2^1 2^0 H	G	F	E	D	C	B	A	PTS
0	0	1	0	0	0	1	1	1	1	1	7169
			0	0	1						6145
			0	1	0						5121
			0	1	1						4097
			1	0	0						3073
			1	0	1						2049
			1	1	0						1025
			1	1	1						1

9.

K	J	PTS CONTROL 2^2 2^1 2^0 I	H	G	F	E	D	C	B	A	PTS
0	0	0	0	0	0	0	0	0	0	0	16384
		0	0	1							14336
		0	1	0							12288
		0	1	1							10240
		1	0	0							8192
		1	0	1							6144
		1	1	0							4096
		1	1	1							2048

10.

K	J	PTS CONTROL 2^2 2^1 2^0 I	H	G	F	E	D	C	B	A	PTS
0	0	0	0	0	1	1	1	1	1	1	14337
		0	0	1							12289
		0	1	0							10241
		0	1	1							8193
		1	0	0							6145
		1	0	1							4097
		1	1	0							2049
		1	1	1							1025

* FOR TWO MEMORIES, SET J=1, FOR SAME PTS AS SHOWN IN TABLES

FOR FOUR MEMORIES, SET J&K=1, FOR SAME PTS AS SHOWN IN TABLES

PTS TABLES
(TWO MEMORIES - K=0)*

11.

PTS CONTROL $2^2 2^1 2^0$															
K	J	I	H	G	F	E	D	C	B	A	P	T	S/CH		
0	0	0	0	0	0	0	0	0	0	0	3	2	7	6	8
	0	0	1								2	8	6	7	2
	0	1	0								2	4	5	7	6
	0	1	1								2	0	4	8	0
	1	0	0								1	6	3	8	4
	1	0	1								1	2	2	8	8
	1	1	0									8	1	9	2
	1	1	1									4	0	9	6

12.

PTS CONTROL $2^2 2^1 2^0$															
K	J	I	H	G	F	E	D	C	B	A	P	T	S		
0	0	0	0	1	1	1	1	1	1	1	2	8	6	7	3
	0	0	1								2	4	5	7	7
	0	1	0								2	0	4	8	1
	0	1	1								1	6	3	8	5
	1	0	0								1	2	2	8	9
	1	0	1									8	1	9	3
	1	1	0									4	0	9	7
	1	1	1												1

PTS TABLES
(FOUR MEMORIES)

13.

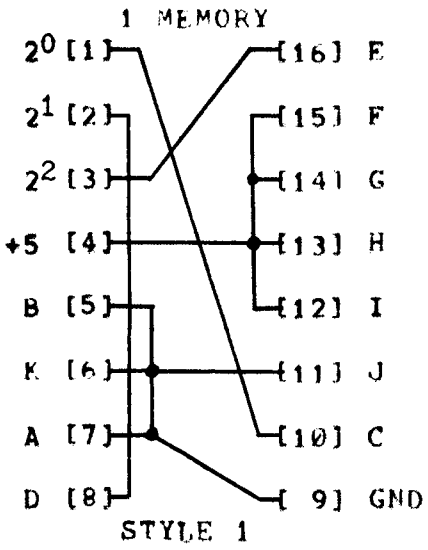
PTS CONTROL $2^2 2^1 2^0$														
K	J	I	H	G	F	E	D	C	B	A	P	T	S	
0	0	0	0	0	0	0	0	0	0	0	6	5	5	3	6
0	0	1									5	7	3	4	4
0	1	0									4	9	1	5	2
0	1	1									4	0	9	6	0
1	0	0									3	2	7	6	8
1	0	1									2	4	5	7	6
1	1	0									1	6	3	8	4
1	1	1										8	1	9	2

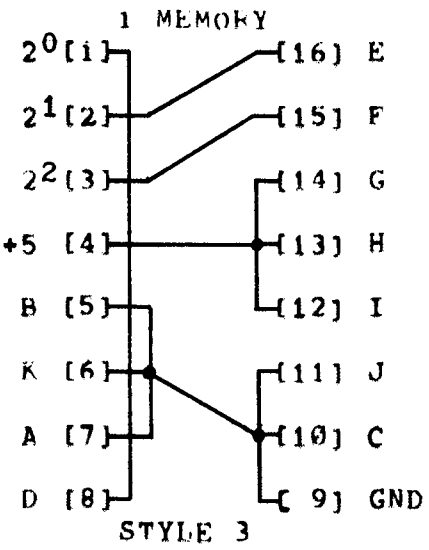
14.

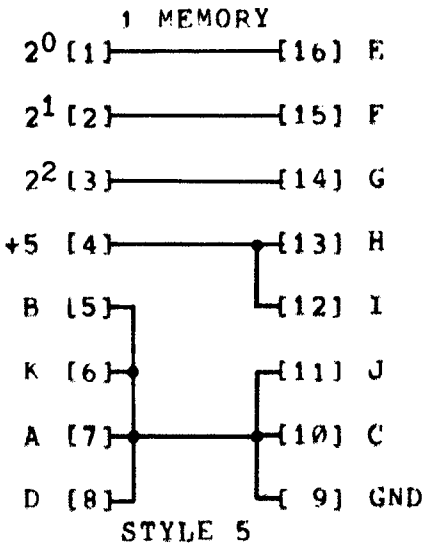
PTS CONTROL $2^2 2^1 2^0$														
K	J	I	H	G	F	E	D	C	B	A	P	T	S	
0	0	0	0	1	1	1	1	1	1	1	5	7	3	4	5
0	0	1									4	9	1	5	3
0	1	0									4	0	9	6	1
0	1	1									3	2	7	6	4
1	0	0									2	4	5	7	7
1	0	1									1	6	3	8	5
1	1	0										8	1	9	3
1	1	1													1

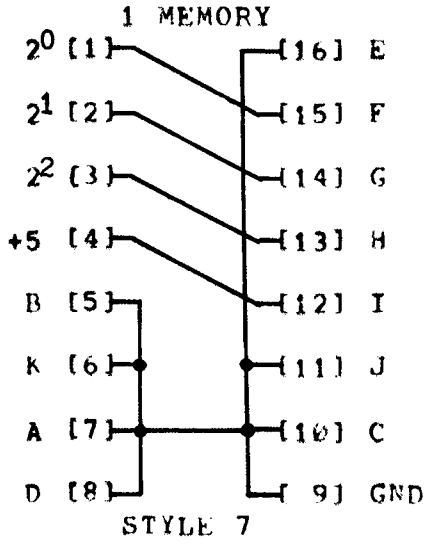
* FOR FOUR MEMORIES, SET K=1 FOR SAME PTS AS SHOWN IN TABLES

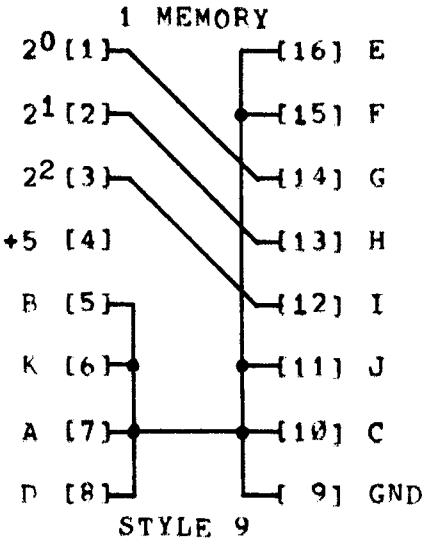
*****CAMAC PTS HEADERS FOR 8212 DATA LOGGERS--1/19/82*****



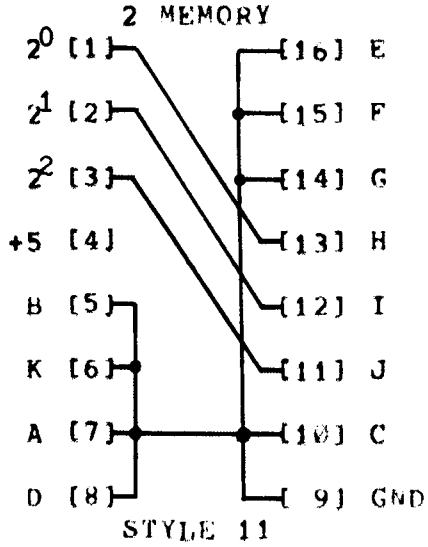


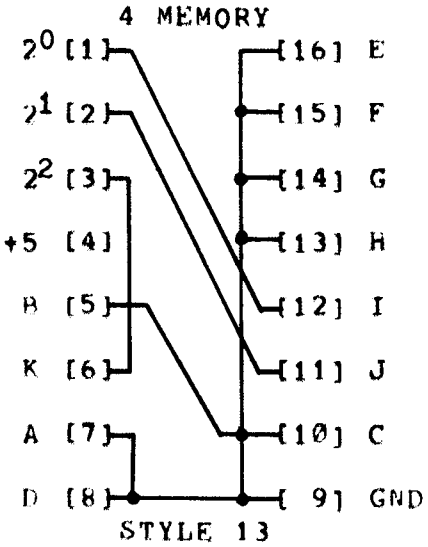




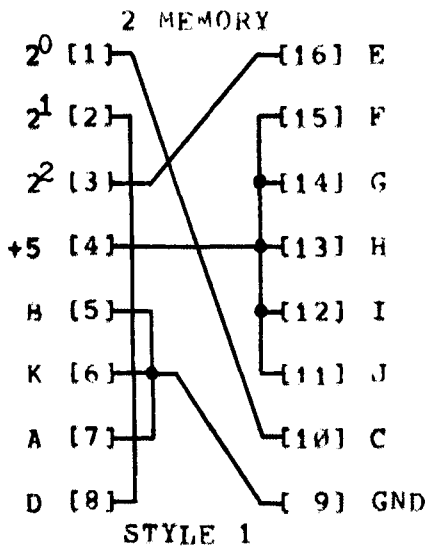


Note:
1 memory J&K=0
2 memory J=1,K=0
4 memory J&K=1

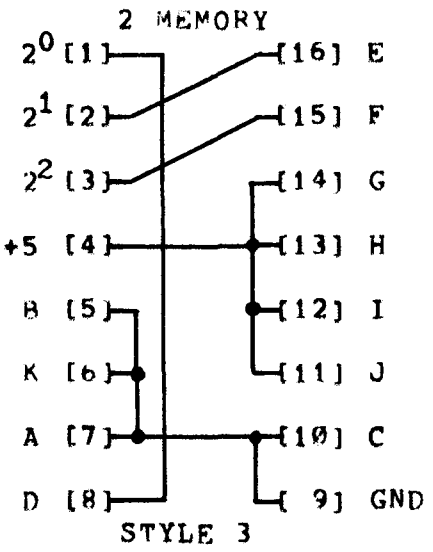




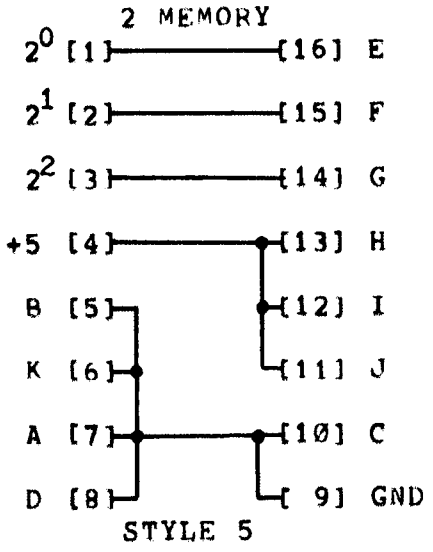
*****CAMAC PTS HEADERS FOR 8212 DATA LOGGERS--1/19/82*****



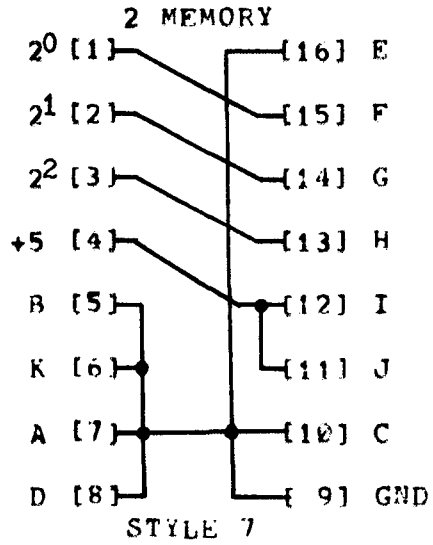
STYLE 1



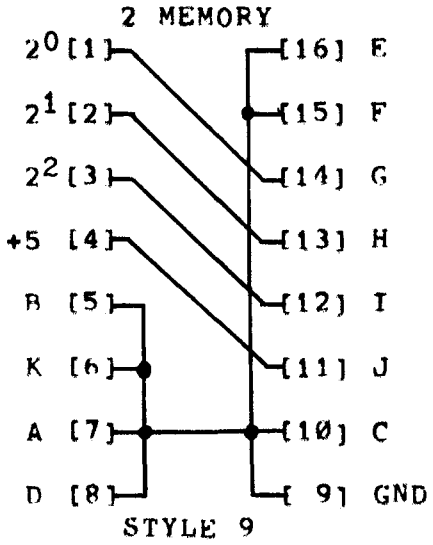
STYLE 3



STYLE 5

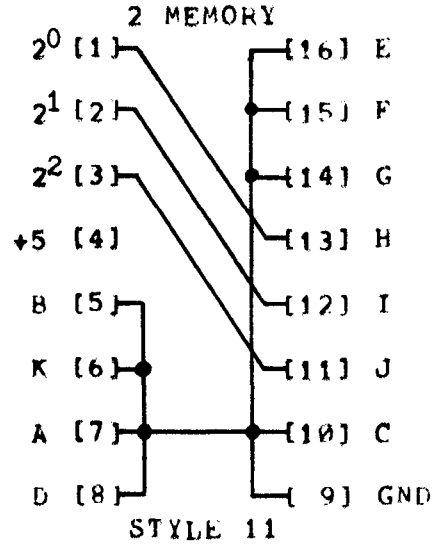


STYLE 7

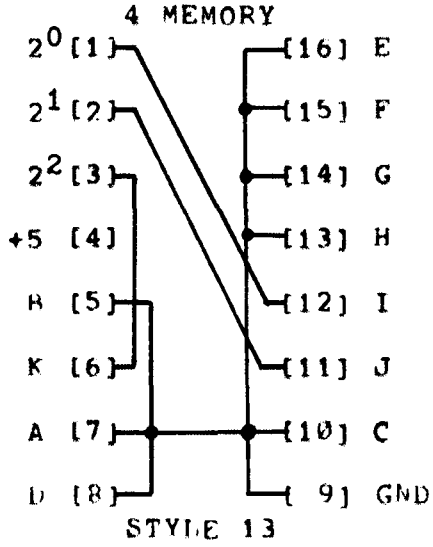


STYLE 9

Note:
1 memory J&K=0
2 memory J=1,K=0
4 memory J&K=1

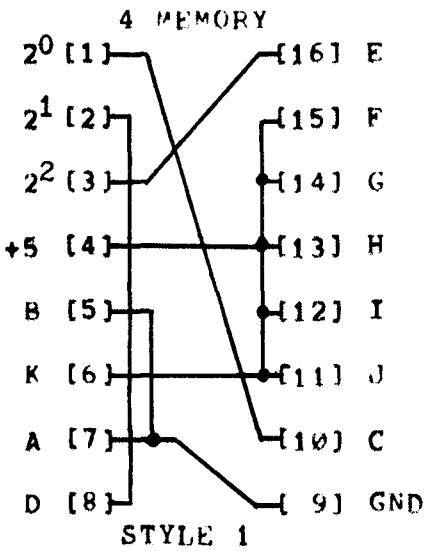


STYLE 11

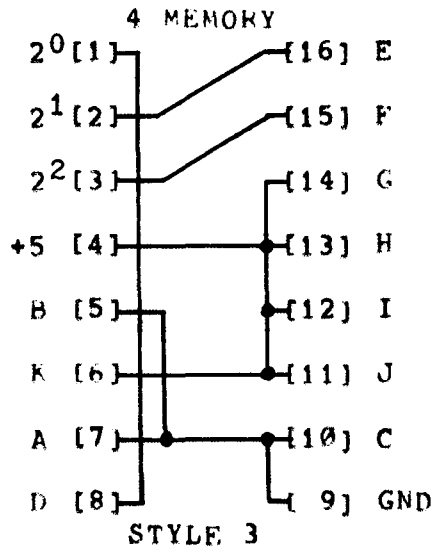


STYLE 13

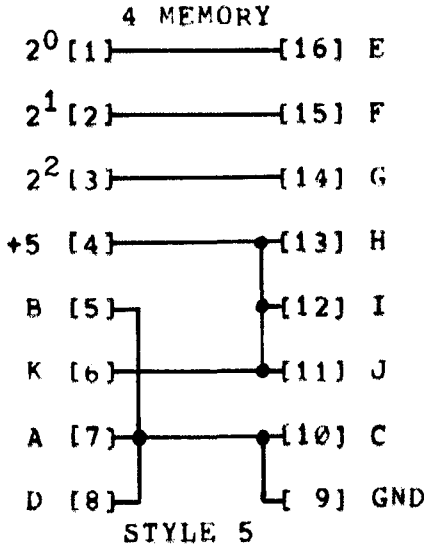
*****CAMAC PTS HEADERS FOR 8212 DATA LOGGERS--1/19/82*****



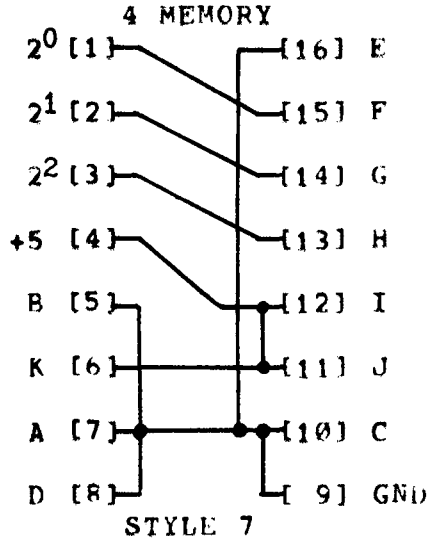
STYLE 1



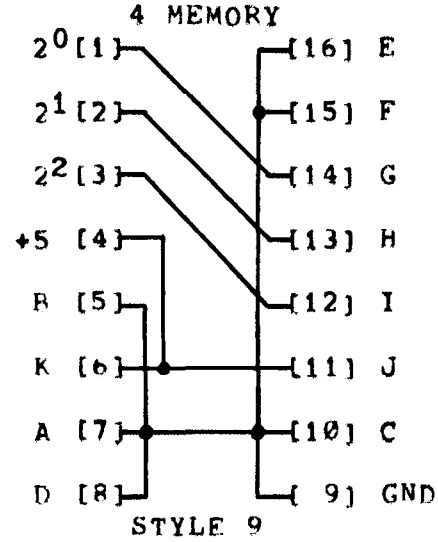
STYLE 3



STYLE 5

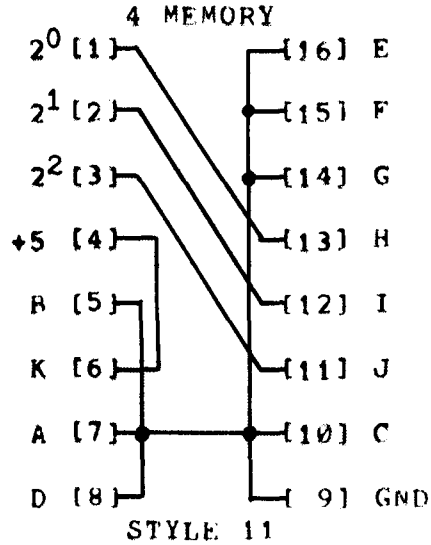


STYLE 7

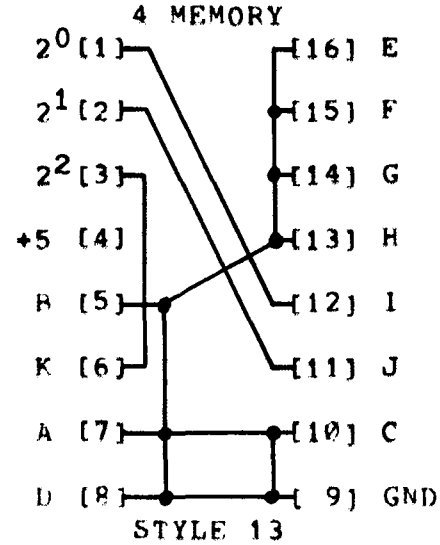


STYLE 9

Note:
1 memory J&K=0
2 memory J=1,K=0
4 memory J&K=1

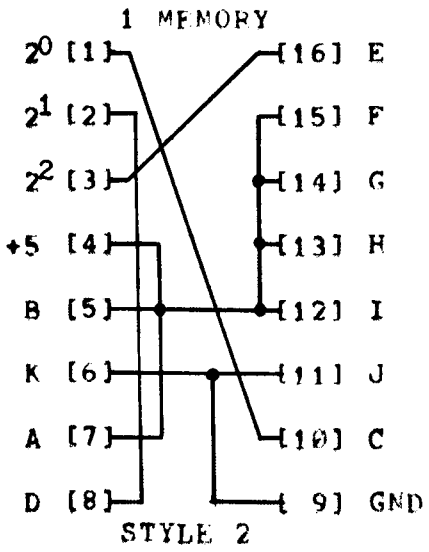


STYLE 11

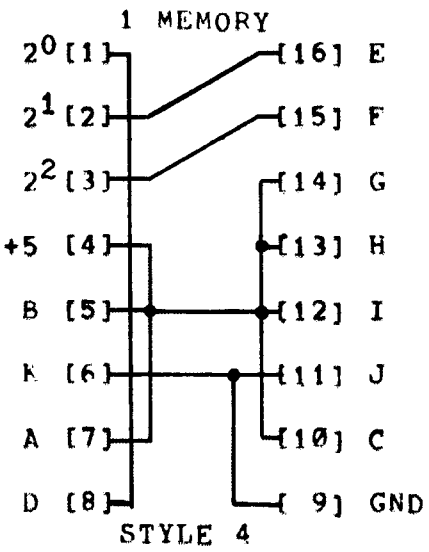


STYLE 13

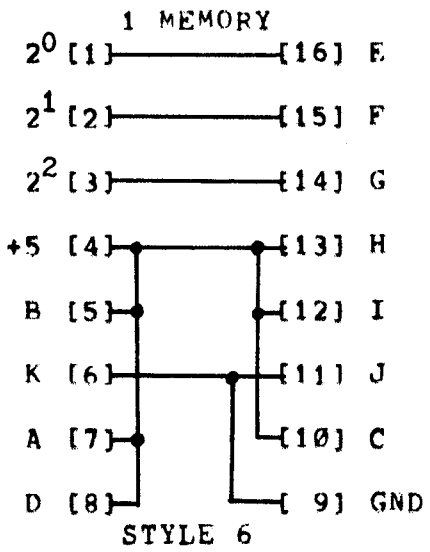
*****CAMAC PTS HEADERS FOR 8212 DATA LOGGERS--1/19/82*****



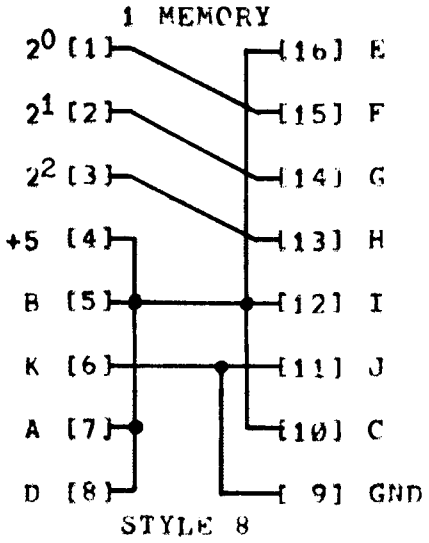
STYLE 2



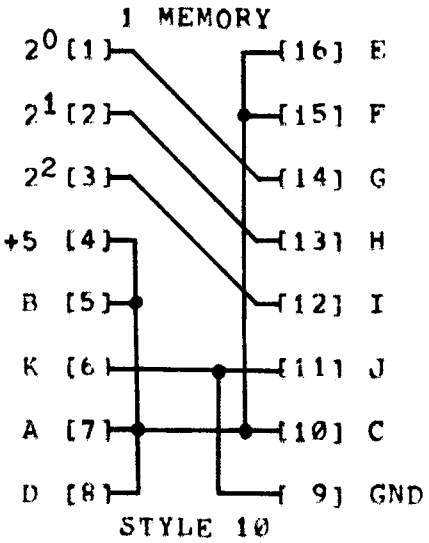
STYLE 4



STYLE 6

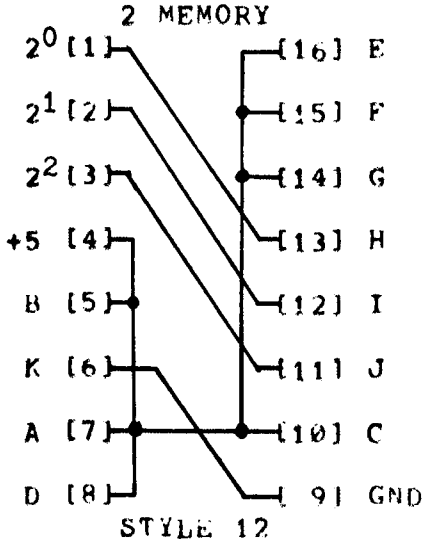


STYLE 8

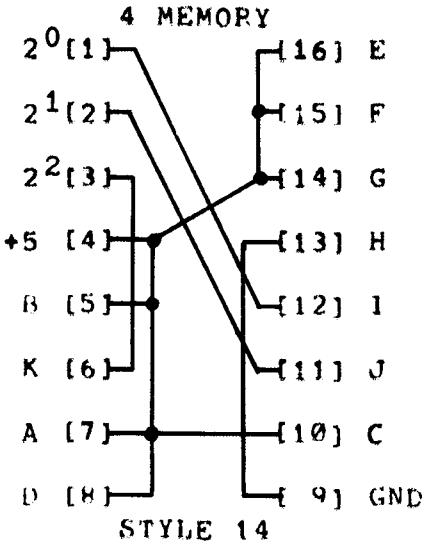


STYLE 10

Note:
1 memory J&K=0
2 memory J=1,K=0
4 memory J&K=1

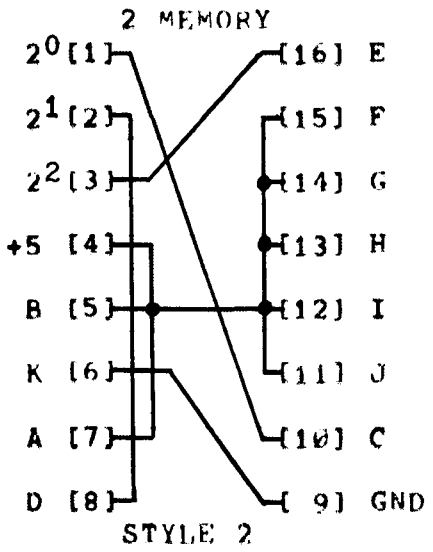


STYLE 12

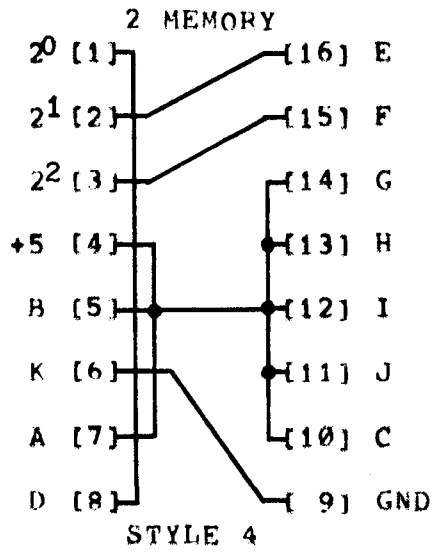


STYLE 14

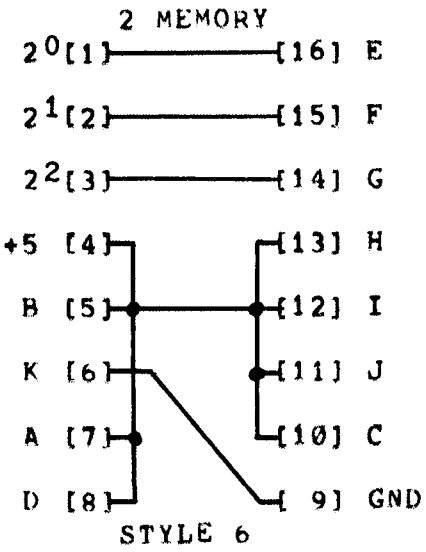
*****CAMAC PTS HEADERS FOR 8212 DATA LOGGERS--1/19/82*****



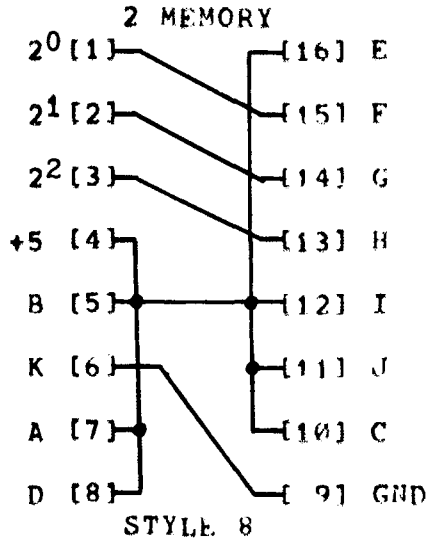
STYLE 2



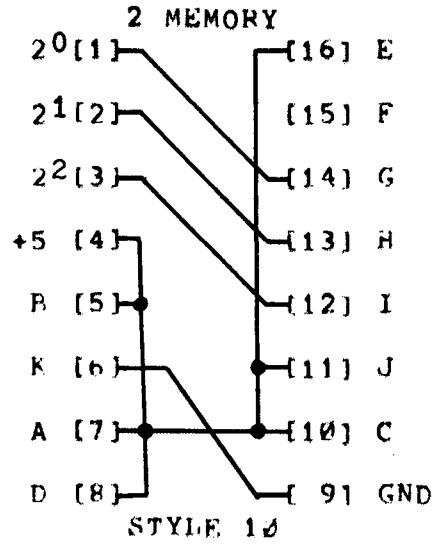
STYLE 4



STYLE 6

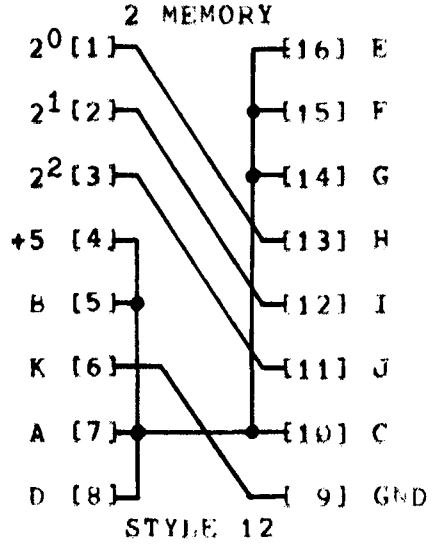


STYLE 8

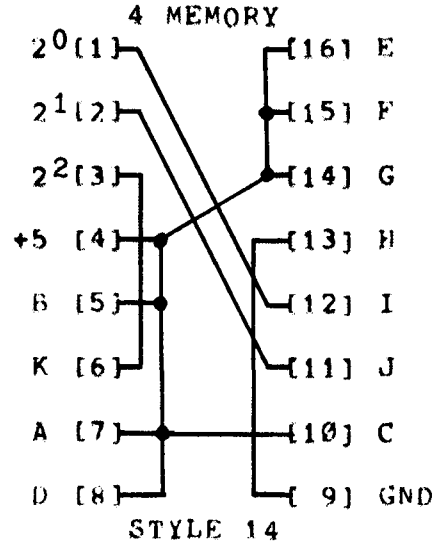


STYLE 10

Note:
1 memory J&K=0
2 memory J=1,K=0
4 memory J&K=1

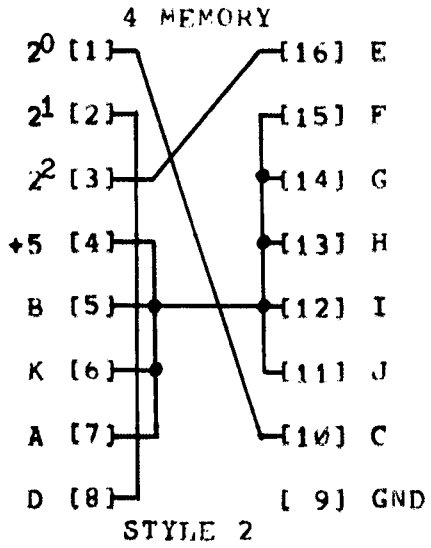


STYLE 12

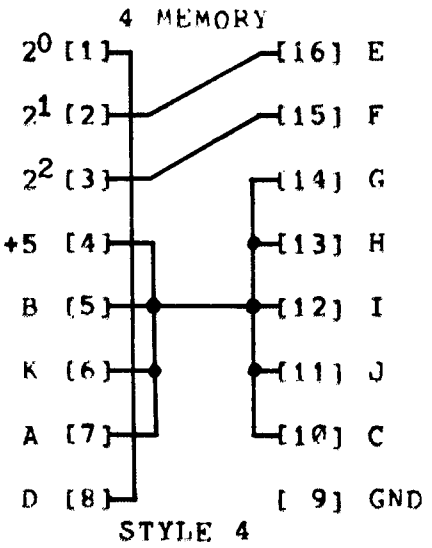


STYLE 14

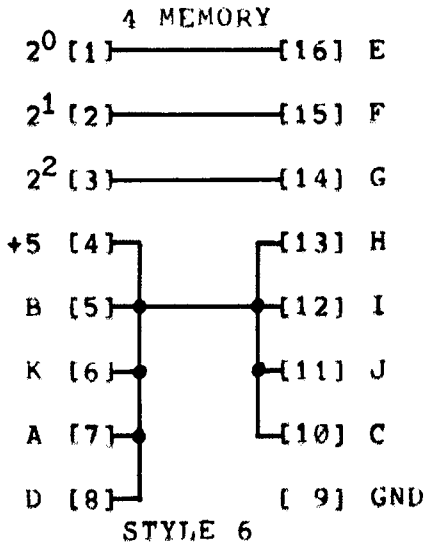
*****CAMAC PTS HEADERS FOR 8212 DATA LOGGERS--1/19/82*****



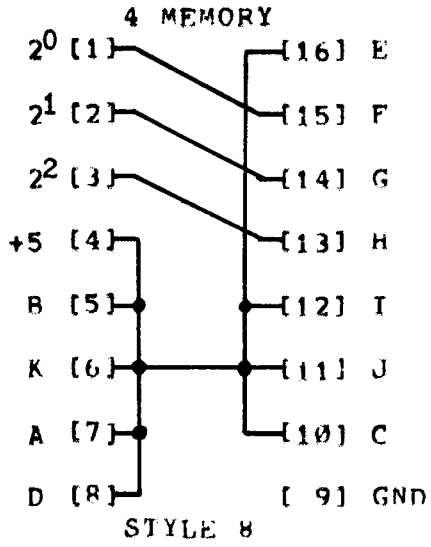
STYLE 2



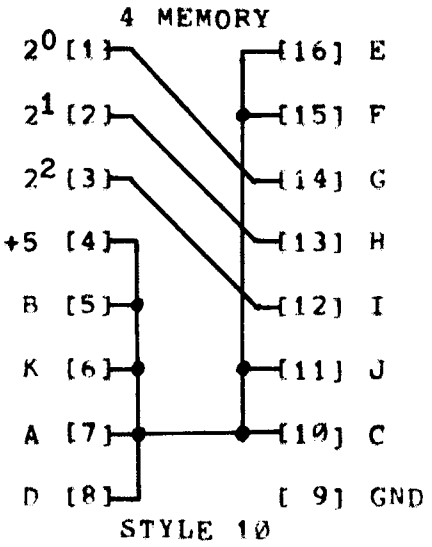
STYLE 4



STYLE 6

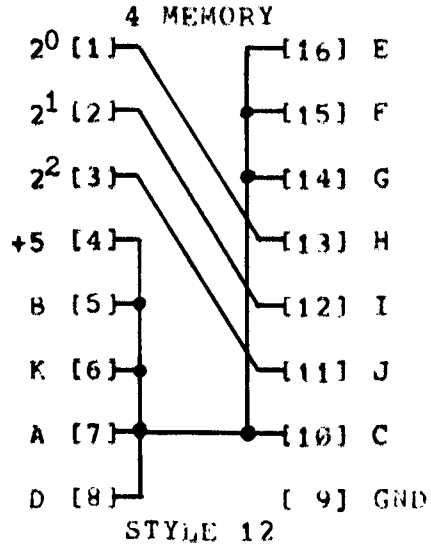


STYLE 8

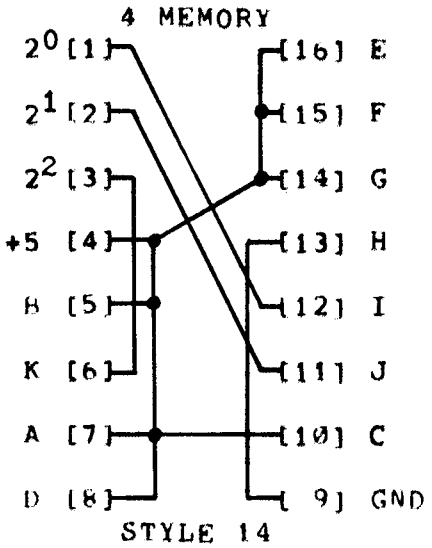


STYLE 10

Note:
1 memory J&K=0
2 memory J=1,K=0
4 memory J&K=1



STYLE 12



STYLE 14

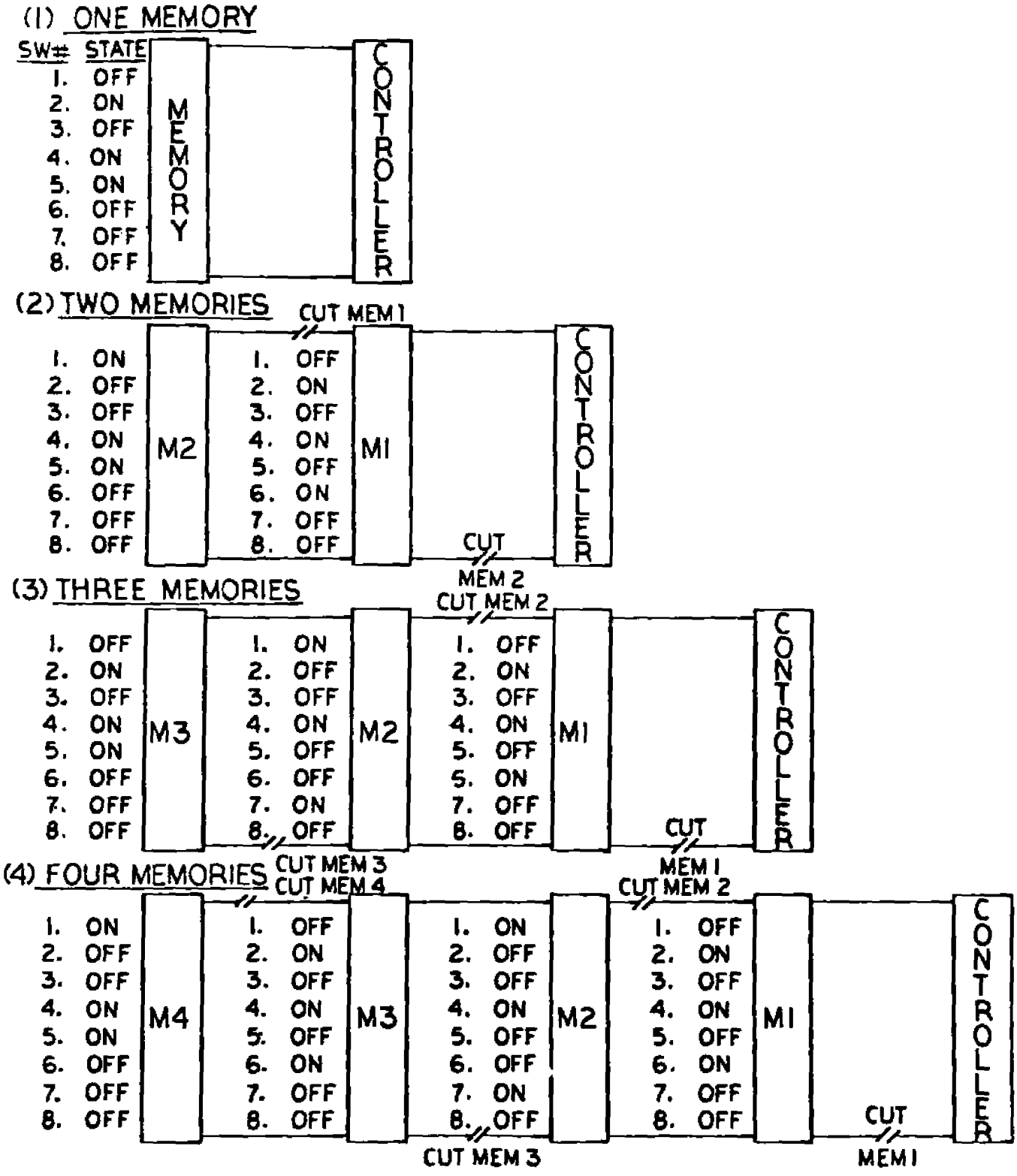
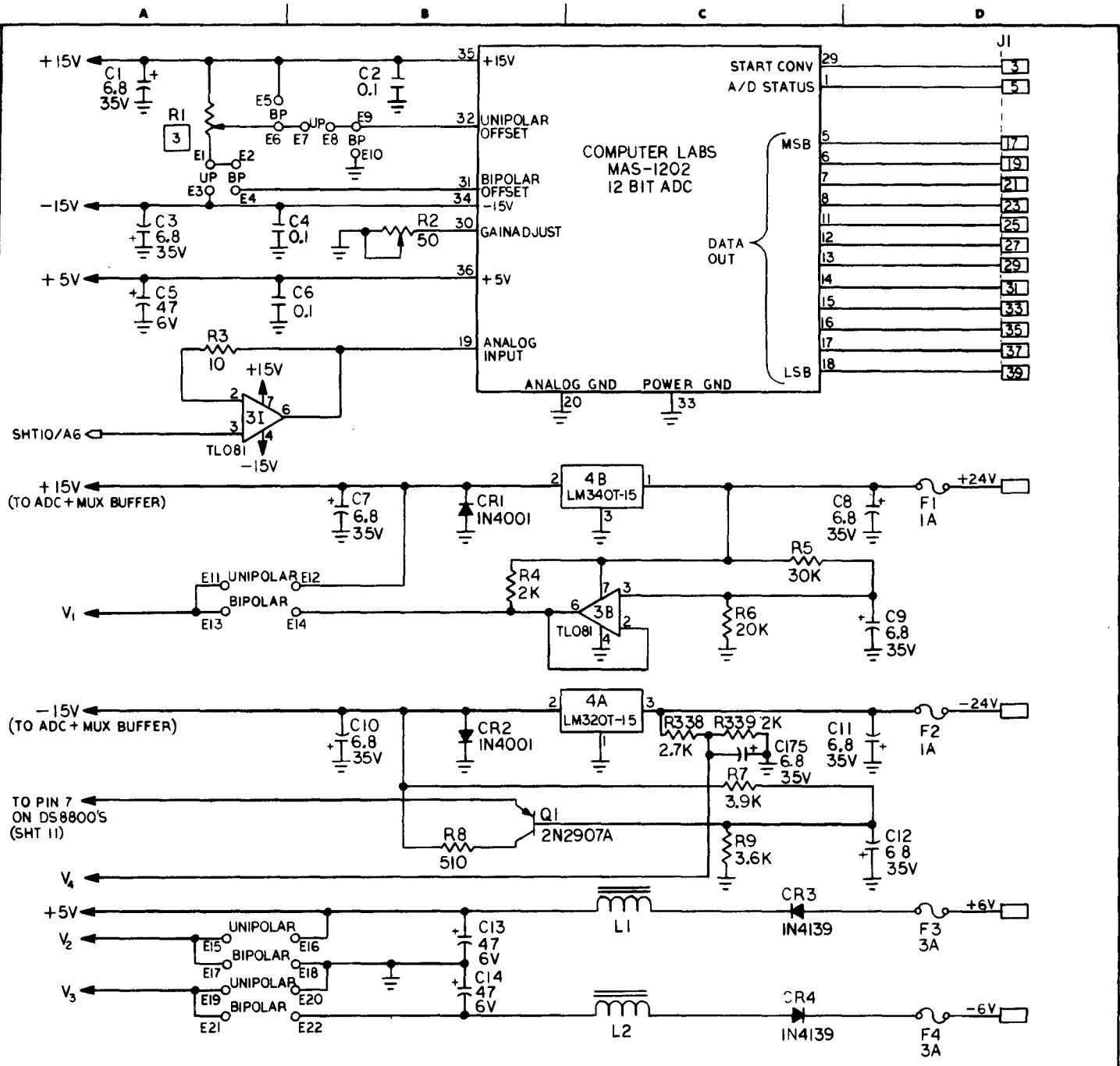

(1) ONE MEMORY
SW# STATE
1. OFF
2. ON
3. OFF
4. ON
5. ON
6. OFF
7. OFF
8. OFF
MEMORY
CONTROLLER
(2) TWO MEMORIES
CUT MEM 1
1. ON
2. OFF
3. OFF
4. ON
5. ON
6. OFF
7. OFF
8. OFF
M2
1. OFF
2. ON
3. OFF
4. ON
5. OFF
6. ON
7. OFF
8. OFF
M1
CUT
MEM 2
CONTROLLER
(3) THREE MEMORIES
CUT MEM 2
1. OFF
2. ON
3. OFF
4. ON
5. ON
6. OFF
7. OFF
8. OFF
M3
1. ON
2. OFF
3. OFF
4. ON
5. OFF
6. OFF
7. ON
8. OFF
M2
1. OFF
2. ON
3. OFF
4. ON
5. OFF
5. ON
7. OFF
8. OFF
M1
CUT
MEM 1
CONTROLLER
(4) FOUR MEMORIES
CUT MEM 3
CUT MEM 4
CUT MEM 2
1. ON
2. OFF
3. OFF
4. ON
5. ON
6. OFF
7. OFF
8. OFF
M4
1. OFF
2. ON
3. OFF
4. ON
5. OFF
6. ON
7. OFF
8. OFF
M3
1. ON
2. OFF
3. OFF
4. ON
5. OFF
6. OFF
7. ON
8. OFF
M2
1. OFF
2. ON
3. OFF
4. ON
5. OFF
6. ON
7. OFF
8. OFF
M1
CUT
MEM 1
CUT MEM 3
CONTROLLER

FIGURE 2.2



NOTES: (UNLESS OTHERWISE SPECIFIED)

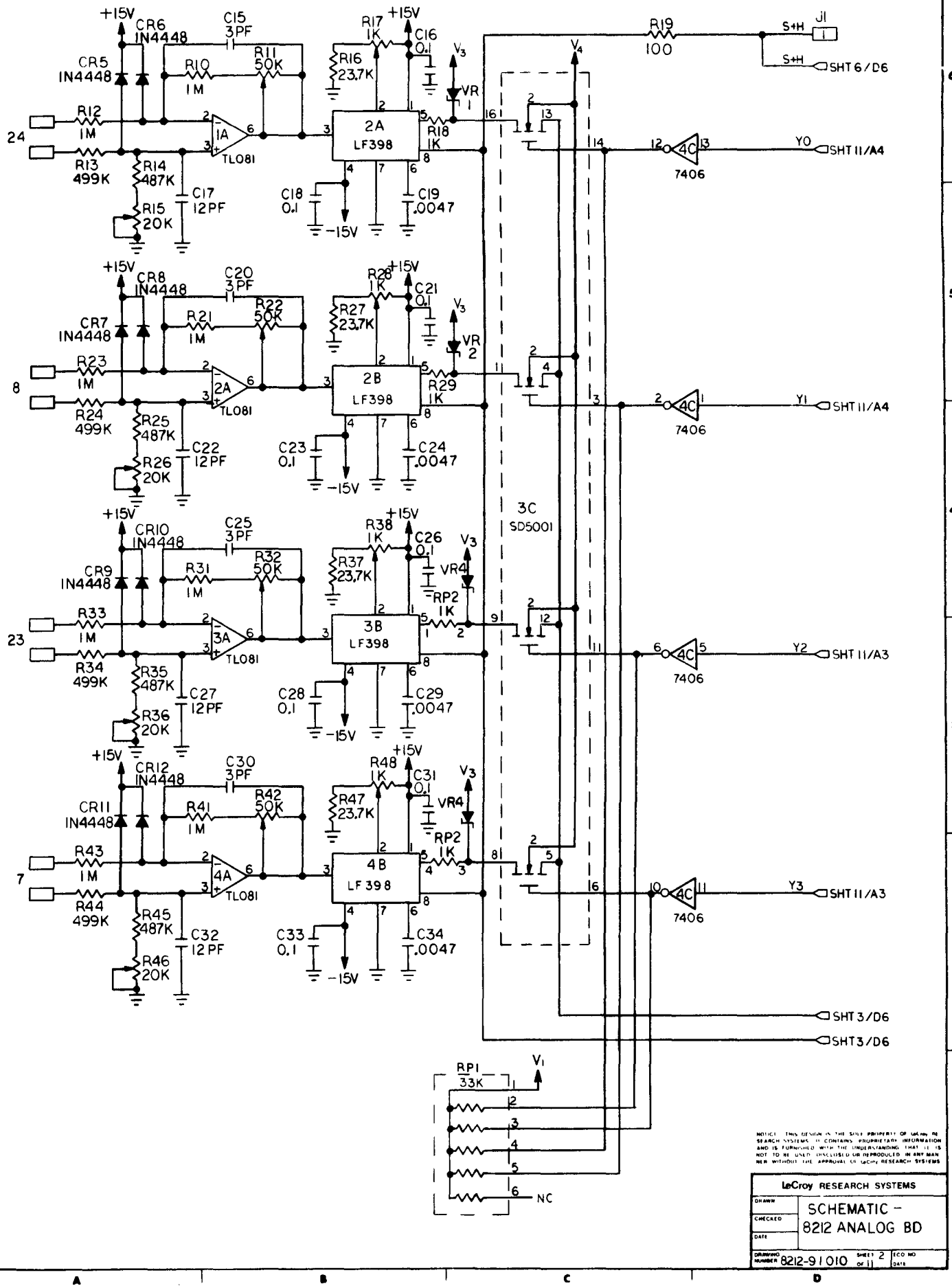
1. ALL RESISTOR VALUES ARE IN OHMS.
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS.
3. VALUES FOR R1 ARE:
   BIPOLAR -200
   UNIPOLAR -20K
4. ALL "VR'S" ARE HP 5082-2811.
5. DS8800 IC'S ARE INSTALLED ONLY IN BIPOLAR UNITS.
   74LS04 IC'S ARE INSTALLED ONLY IN UNIPOLAR UNITS.
6. ALL EVEN PINS ON CONNECTOR J1 ARE GROUND.
7. R20,30,39,40,49,50,59,60,69,70,80,90,110,119,120,129,130,139,140, 149,150,160,170,181,191,200,201,210,211,220,221,230,231,241,251, 261,271,280,281,290,291,300,301,310,311,321,331,332,336,337, ALL ARE NOW IN RESISTOR PACKS RP1 - RP13.

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
R339	7
C175	
CR68	
VR32	
E22	
F4	
L2	
Q1	
RP13	

LeCroy RESEARCH SYSTEMS

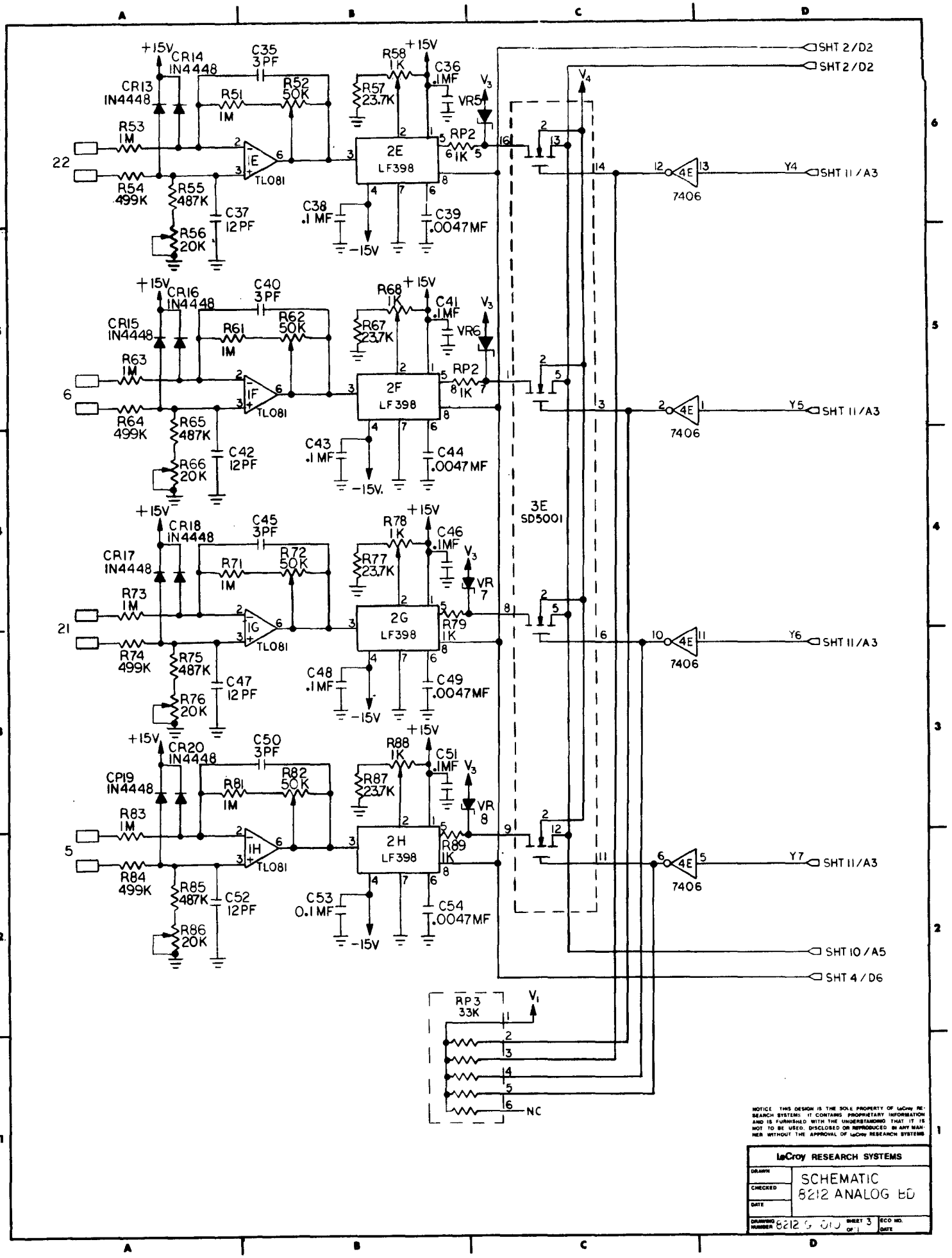
SCHEMATIC - 8212 ANALOG BD

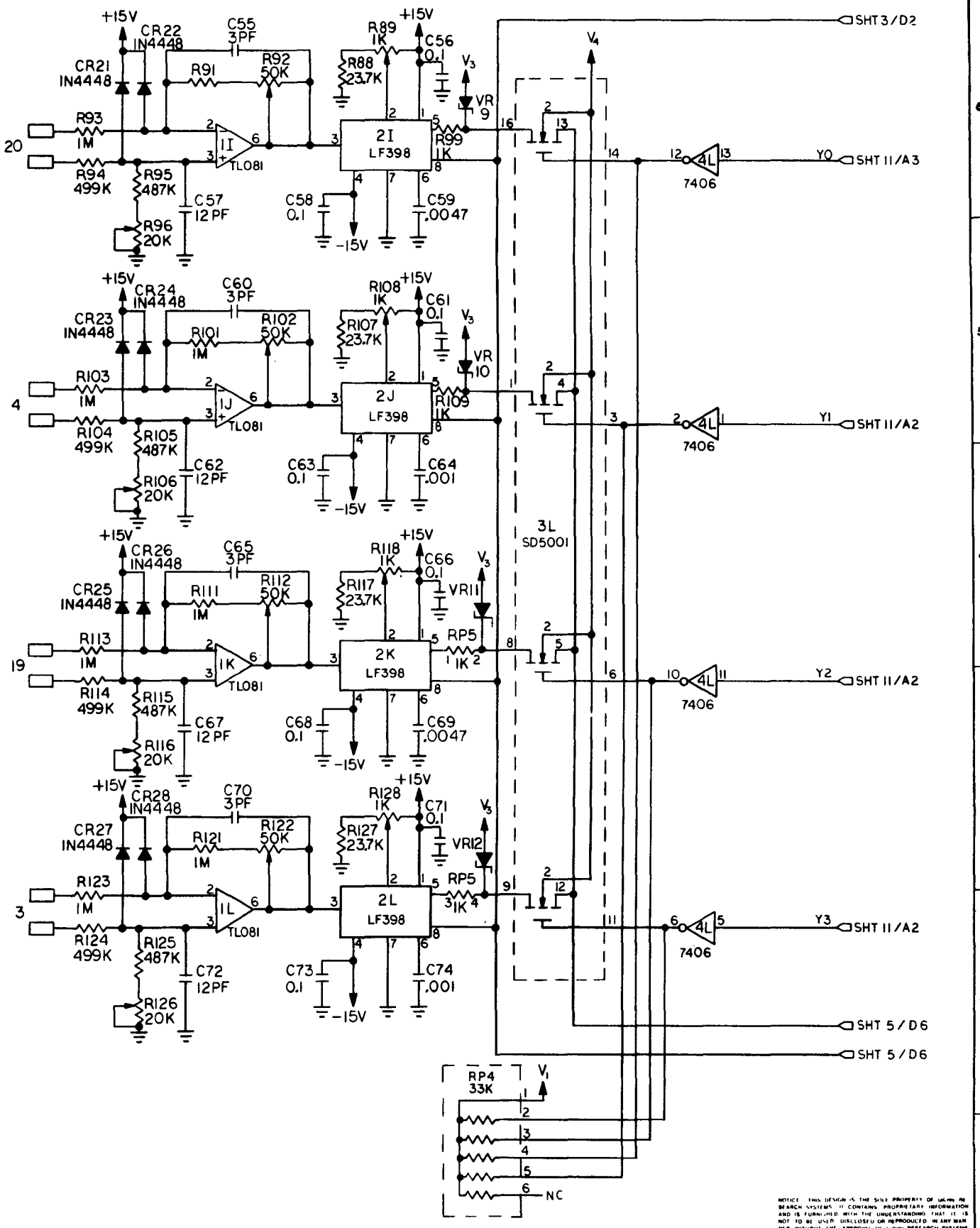
DRAWN CWP
CHK'D
DATE 6/21/78
DRAWING NUMBER 8212-91010
SHEET 1 OF 11
ECO NO
DATE



LeCroy RESEARCH SYSTEMS

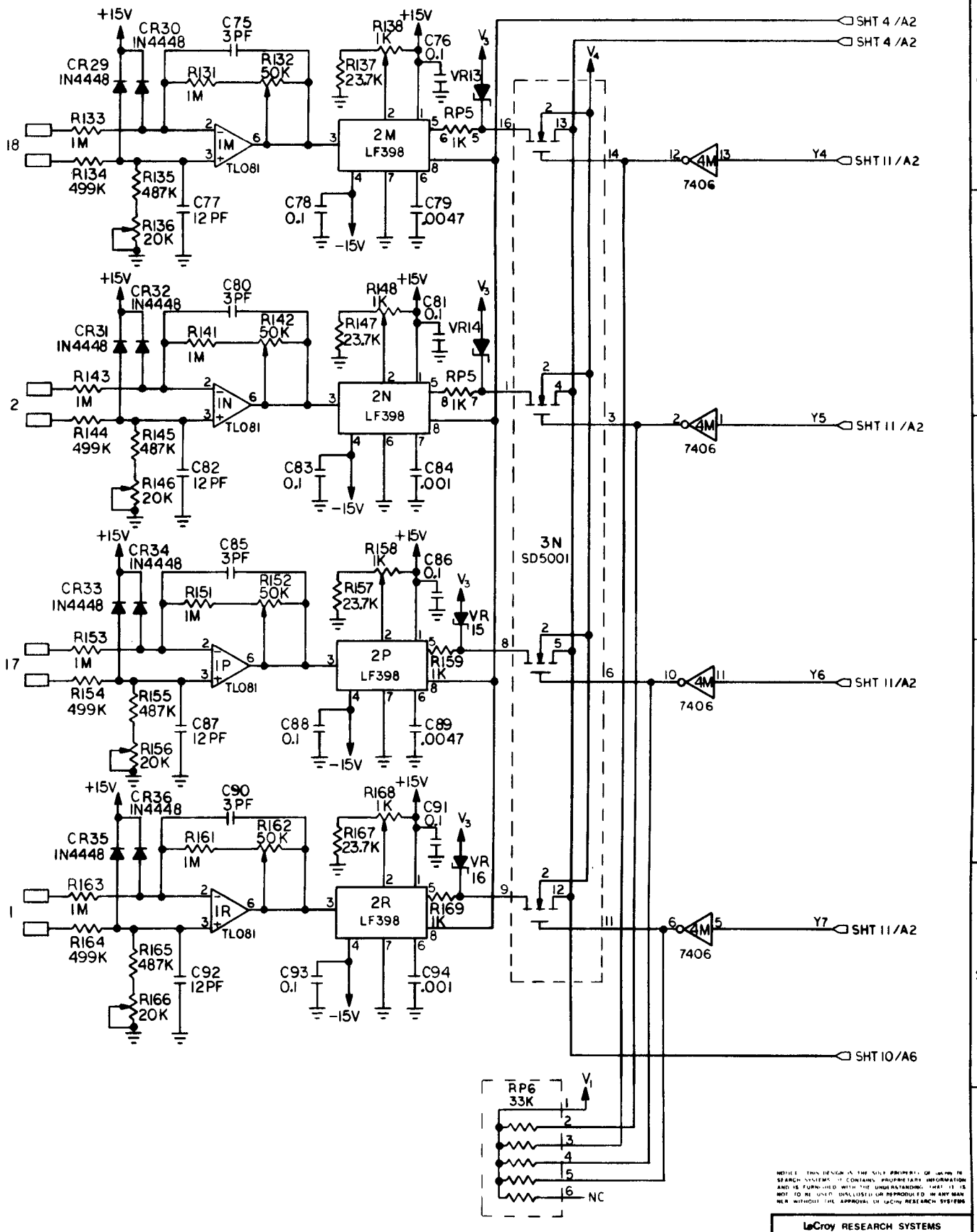
DRAWN	SCHEMATIC – 8212 ANALOG BD
CHECKED	
DATE	
DRAWING NUMBER 8212-91010	SHEET 2 OF 11 ECO NO DATE


+15V
CR14 IN4448
C35 3PF
R58 1K
C36 .1MF
V3
VR5
CR13 IN4448
R51 1M
R52 50K
R57 23.7K
R53 1M
22
1E TLO81
2E LF398
RP2 1K
R54 499K
R55 487K
C37 12PF
R56 20K
C38 .1 MF
C39 .0047MF
-15V
SHT 2/D2
SHT2/D2
V4
Y4
SHT 11/A3
4E 7406
CR16 IN4448
C40 3PF
R68 1K
C41 .1MF
CR15 IN4448
R61 1M
R62 50K
R67 23.7K
R63 1M
6
1F TLO81
2F LF398
R64 499K
R65 487K
C42 12PF
R66 20K
C43 .1 MF
C44 .0047MF
-15V.
Y5
CR18 IN4448
C45 3PF
R78 1K
C46 .1MF
CR17 IN4448
R71 1M
R72 50K
R77 23.7K
R73 1M
21
1G TLO81
2G LF398
R79 1K
R74 499K
R75 487K
C47 12PF
R76 20K
C48 .1MF
C49 .0047MF
3E SD5001
Y6
CR20 IN4448
C50 3PF
R88 1K
C51 .1MF
CPI9 IN4448
R81 1M
R82 50K
R87 23.7K
R83 1M
5
1H TLO81
2H LF398
R89 1K
R84 499K
R85 487K
C52 12PF
R86 20K
C53 0.1 MF
C54 .0047MF
Y7
SHT 10/A5
SHT 4/D6
RP3 33K
V1
NC
NOTICE THIS DESIGN IS THE SOLE PROPERTY OF LeCroy RESEARCH SYSTEMS IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCroy RESEARCH SYSTEMS
LeCroy RESEARCH SYSTEMS
DRAWN
CHECKED
DATE
SCHEMATIC
8212 ANALOG BD
DRAWING NUMBER 8212 S 010
SHEET 3 OF 1
ECO NO.
DATE

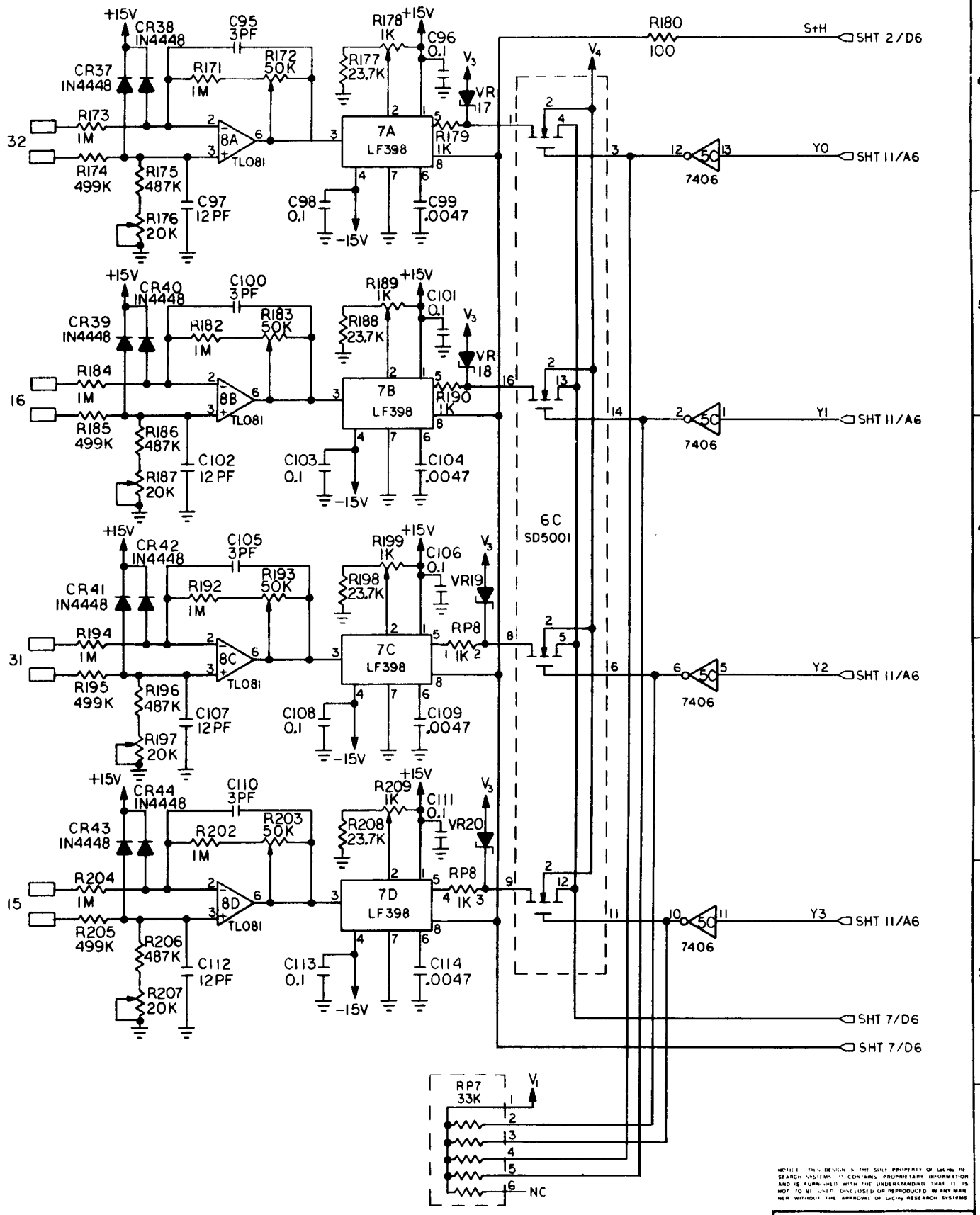


LeCroy RESEARCH SYSTEMS

DRAWN	SCHEMATIC – 8212 ANALOG BD
CHECKED	
DATE	
DRAWING NUMBER 8212-91010	SHEET 4 OF 11
ECO NO.	DATE

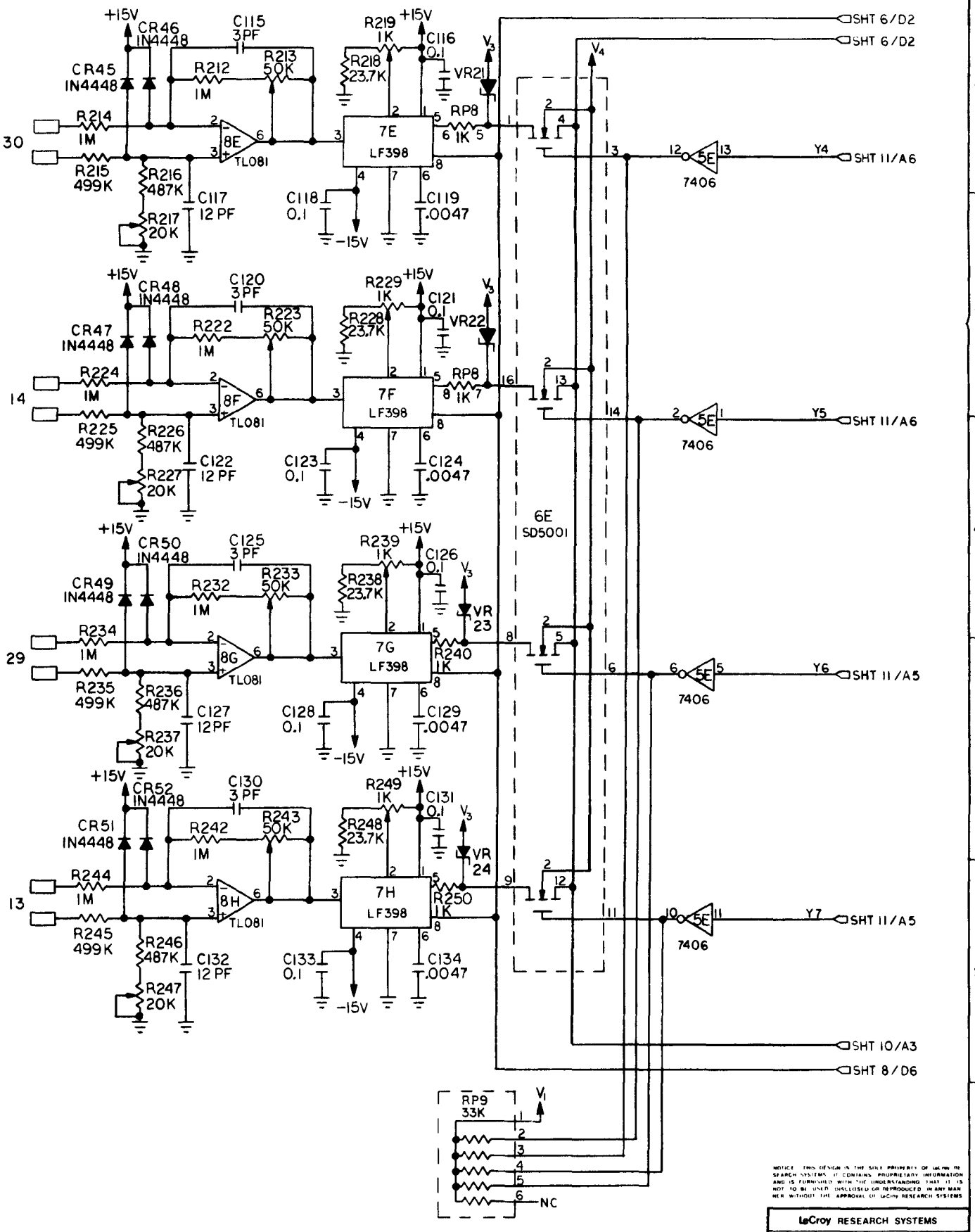


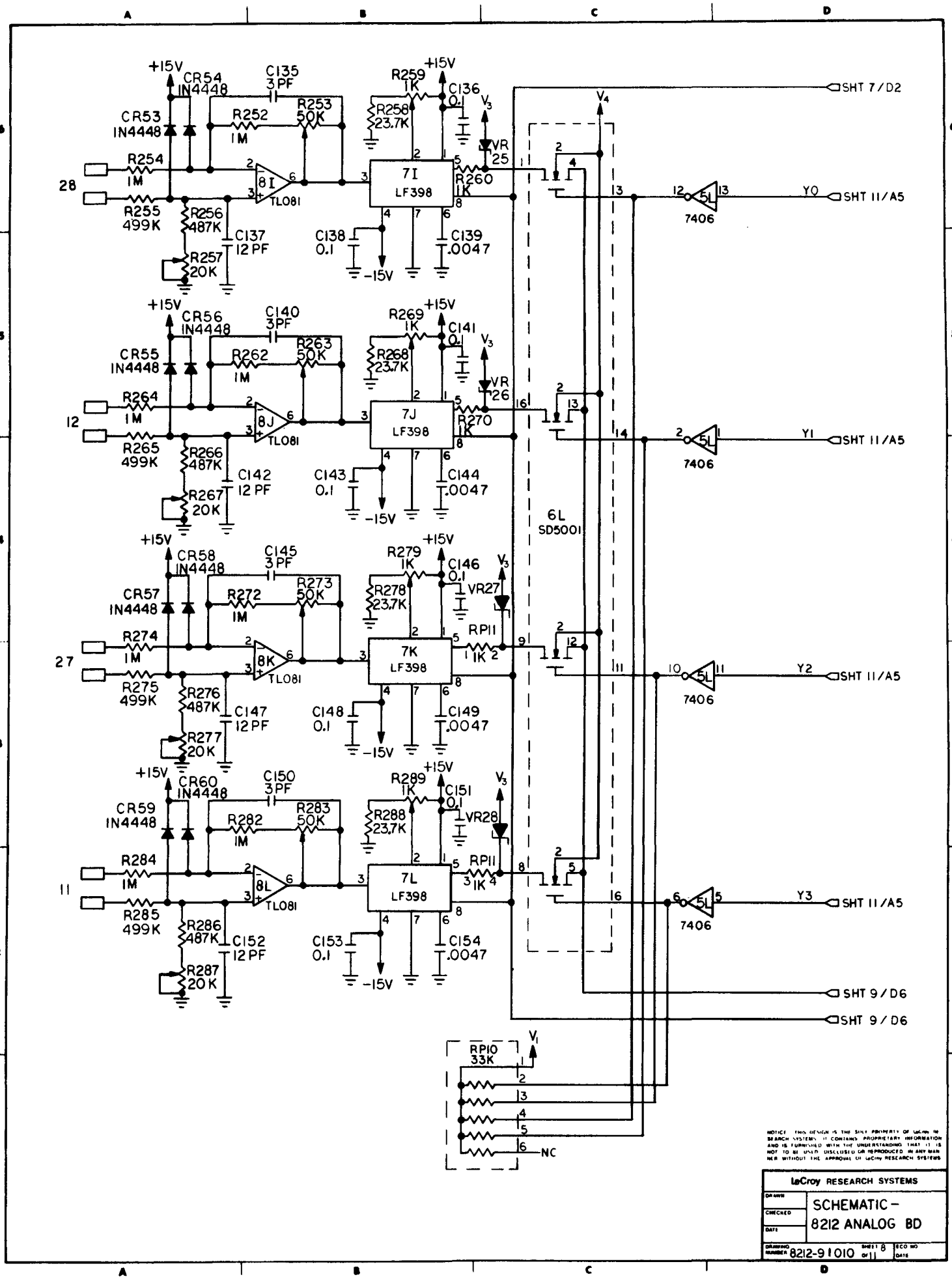
LeCroy RESEARCH SYSTEMS	
DRAWN	SCHEMATIC – 8212 ANALOG BD
CHECKED	
DATE	
DRAWING NUMBER 8212-91 010	SHEET 5 OF 11 ECO NO DATE



LeCroy RESEARCH SYSTEMS

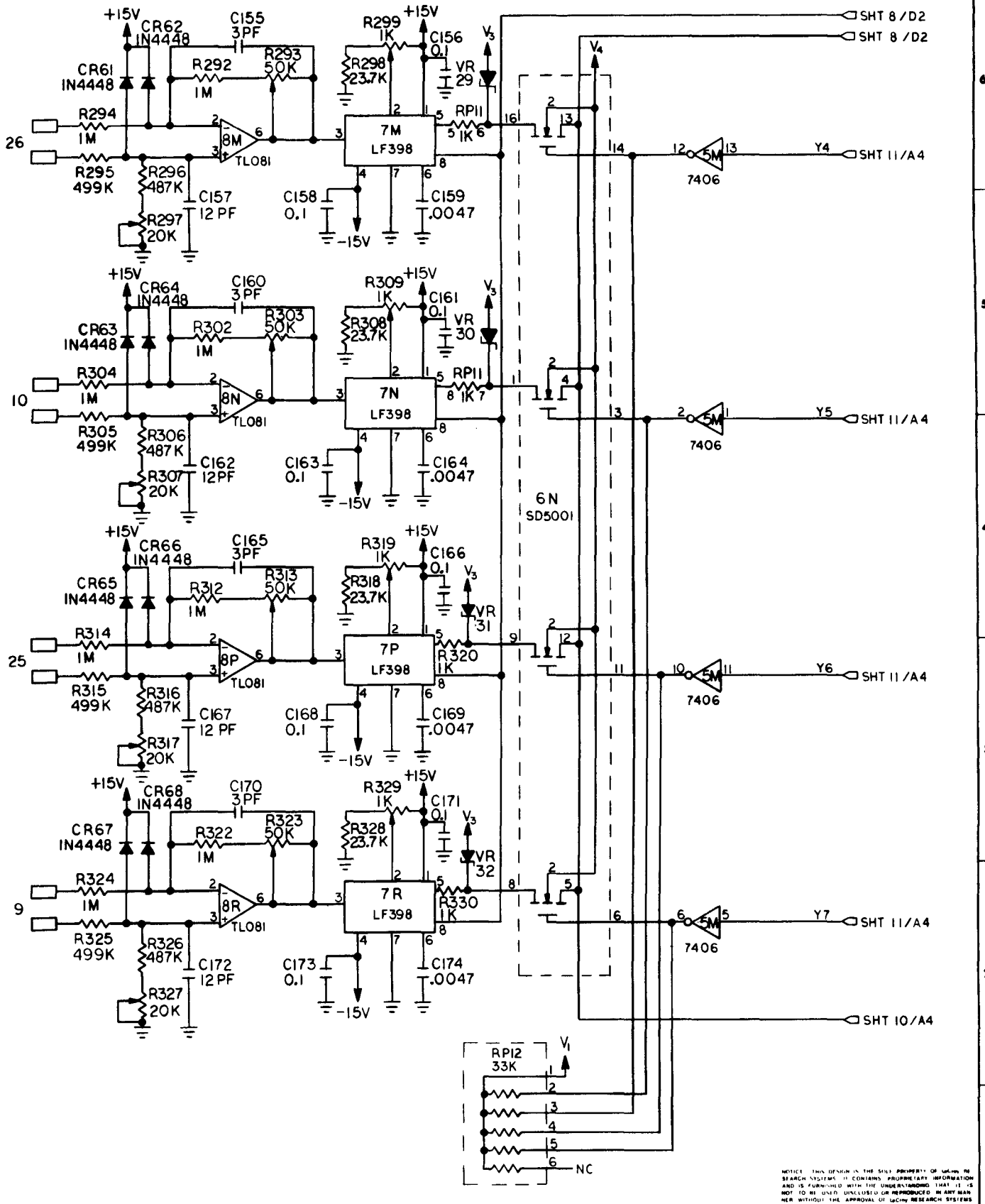
DRAWN	SCHEMATIC – 8212 ANALOG BD
CHECKED	
DATE	
DRAWING NUMBER 8212-91010	SHEET 6 OF 11 ECO NO. DATE


+15V
CR46 IN4448
C115 3PF
R213 50K
R212 1M
CR45 IN4448
R214 1M
R215 499K
R216 487K
C117 12 PF
R217 20K
8E TL081
30
R219 1K
C116 0.1
R218 23.7K
VR21
7E LF398
RP8 6 1K 5
C118 0.1
C119 .0047
-15V
SHT 6/D2
SHT 6/D2
V3
V4
12 5E 13
7406
Y4
SHT 11/A6
CR48 IN4448
C120 3PF
R223 50K
R222 1M
CR47 IN4448
R224 1M
R225 499K
R226 487K
C122 12 PF
R227 20K
8F TL081
14
R229 1K
C121 0.1
R228 23.7K
VR22
7F LF398
RP8 8 1K 7
C123 0.1
C124 .0047
2 5E 1
7406
Y5
SHT 11/A6
6E SD5001
CR50 IN4448
C125 3PF
R233 50K
R232 1M
CR49 IN4448
R234 1M
R235 499K
R236 487K
C127 12PF
R237 20K
8G TL081
29
R239 1K
C126 0.1
R238 23.7K
VR 23
7G LF398
R240 1K
C128 0.1
C129 .0047
6 5E 5
7406
Y6
SHT 11/A5
CR52 IN4448
C130 3PF
R243 50K
R242 1M
CR51 IN4448
R244 1M
R245 499K
R246 487K
C132 12 PF
R247 20K
8H TL081
13
R249 1K
C131 0.1
R248 23.7K
VR 24
7H LF398
R250 1K
C133 0.1
C134 .0047
10 5E 11
7406
Y7
SHT 11/A5
SHT 10/A3
SHT 8/D6
RP9 33K
V1
NC
NOTICE THIS DESIGN IS THE SOLE PROPERTY OF LeCROY RESEARCH SYSTEMS IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCroy RESEARCH SYSTEMS
LeCroy RESEARCH SYSTEMS
DRAWN
CHECKED
DATE
SCHEMATIC—
8212 ANALOG BD
DRAWING NUMBER 8212-91 010
SHEET 7 OF 11
ECO NO
DATE



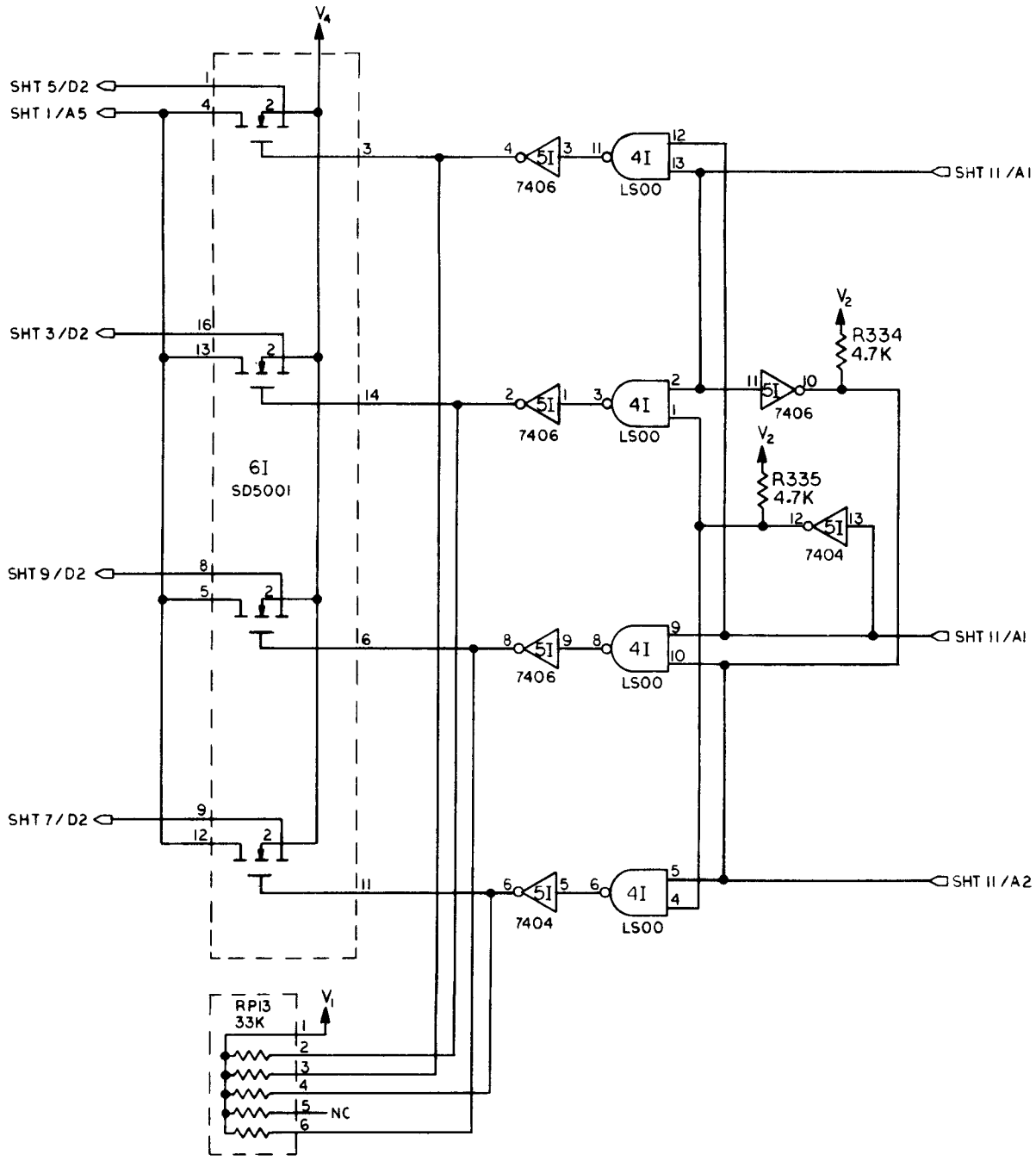
LeCroy RESEARCH SYSTEMS

DRAWN	SCHEMATIC – 8212 ANALOG BD
CHECKED	
DATE	
DRAWING NUMBER	8212-91010 SHEET 8 OF 11 ECO NO DATE



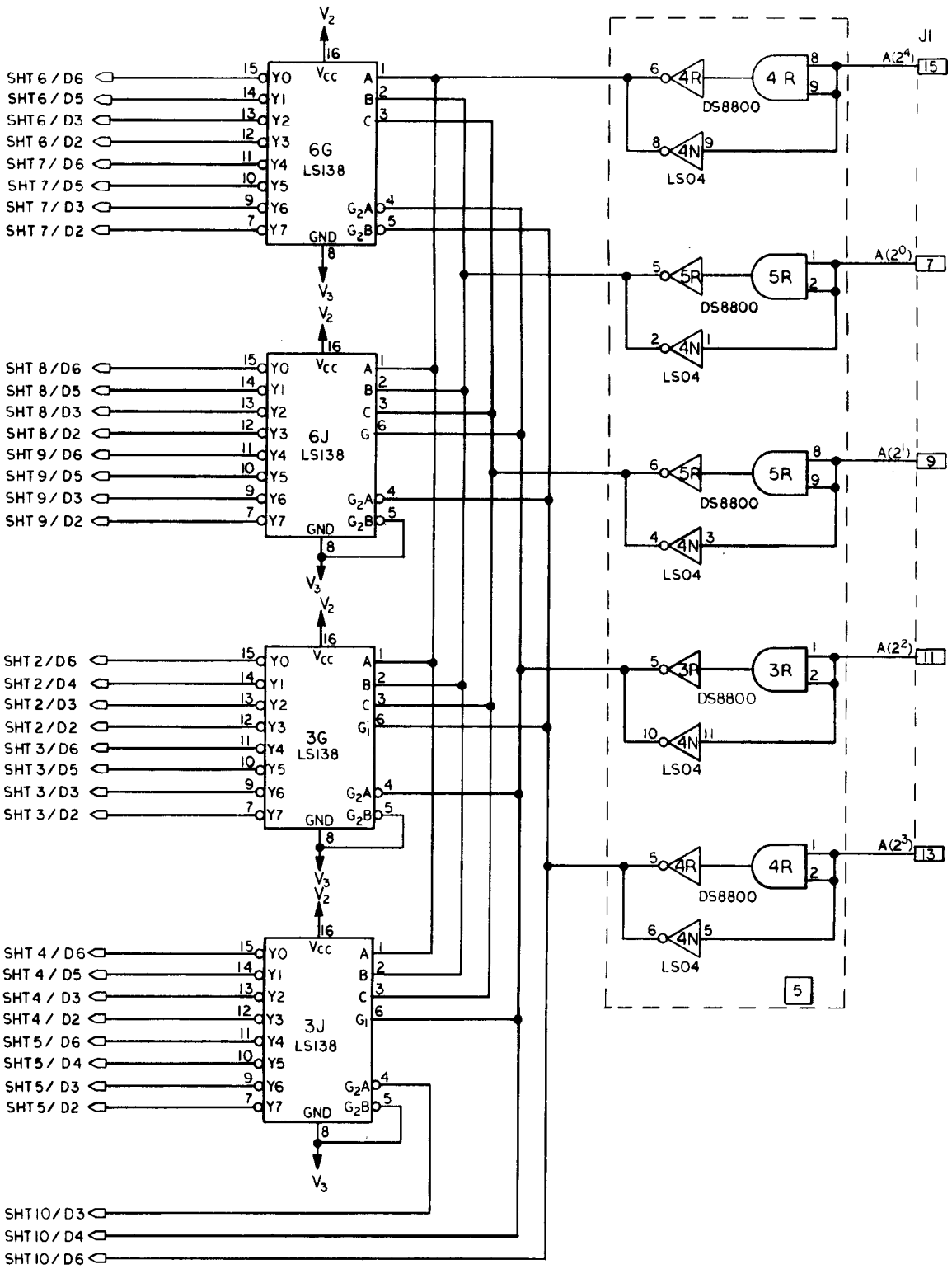
LeCroy RESEARCH SYSTEMS

DRAWN	SCHEMATIC– 8212 ANALOG BD
CHECKED	
DATE	
DRAWING NUMBER	8212-91010 SHEET 5 OF 11 ECO NO DATE



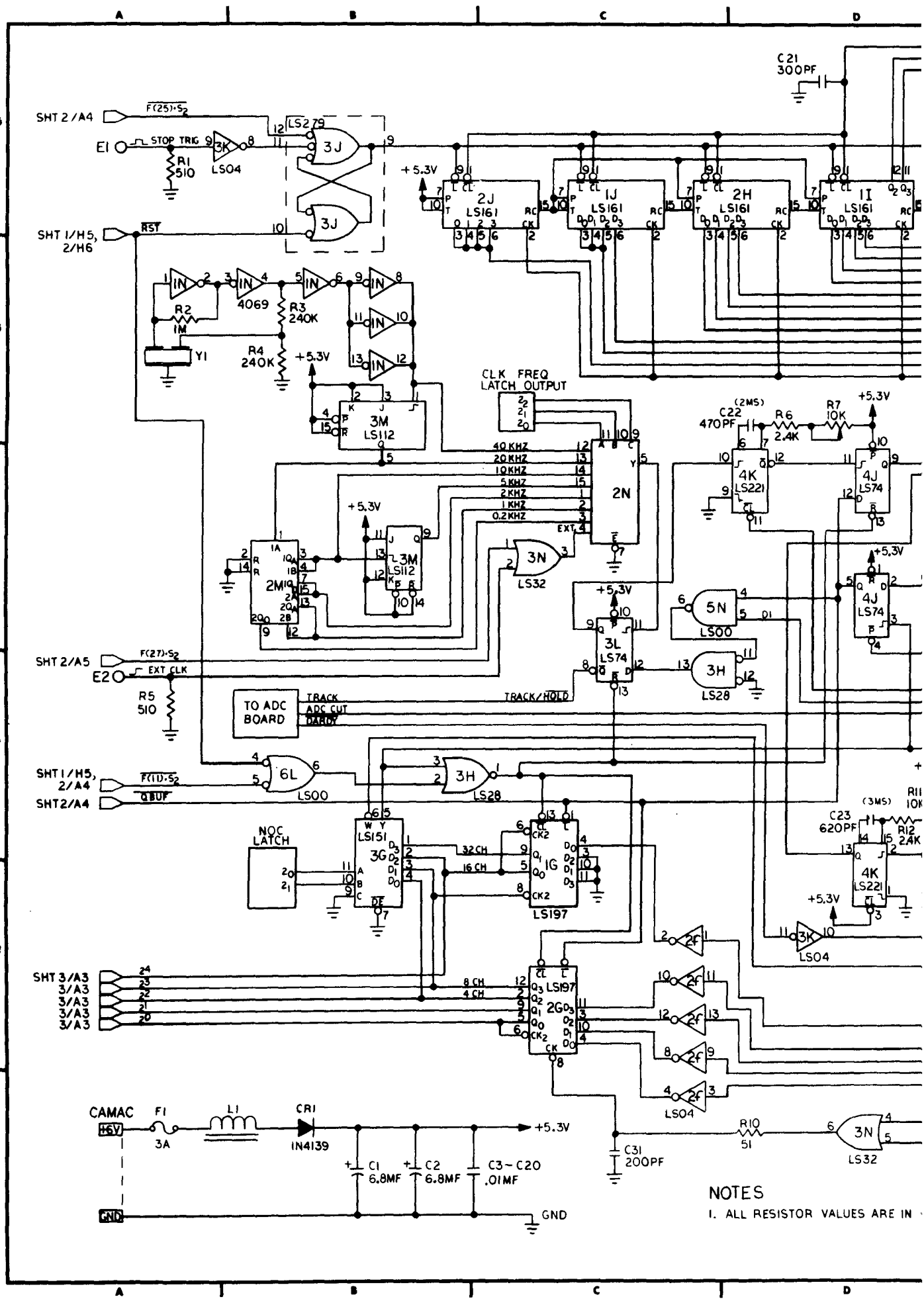
LeCroy RESEARCH SYSTEMS

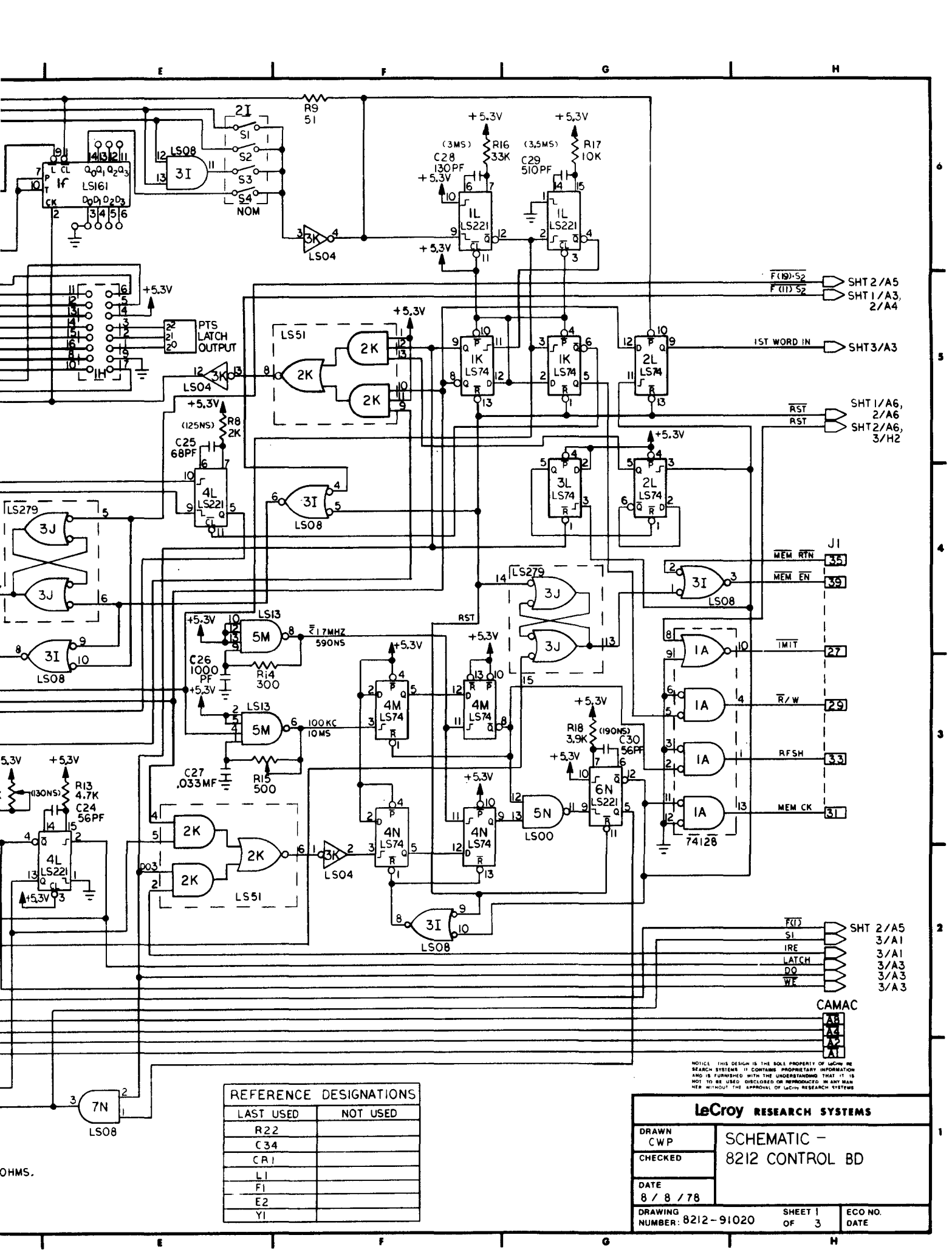
DRAWN	SCHEMATIC— 8212 ANALOG BD
CHECKED	
DATE	
DRAWING NUMBER 8212-91010	SHEET 10 OF 11
ECO NO.	DATE



LeCroy RESEARCH SYSTEMS

DRAWN	SCHEMATIC
CHECKED	8212 ANALOG BD
DATE	
DRAWING NUMBER 8212 91010	SHEET 11 OF 11
ECO NO	DATE


SHT 2/A4
E1
STOP TRIG
R1 510
LS04
SHT 1/H5, 2/H6
RST
3J
LS279
+5.3V
2J LS161
1J LS161
2H LS161
1I LS161
C21 300PF
4069
R2 1M
R3 240K
R4 240K
Y1
3M LS112
CLK FREQ LATCH OUTPUT
40 KHZ
20 KHZ
10 KHZ
5 KHZ
2 KHZ
1 KHZ
0.2 KHZ
EXT
2N
3N LS32
2M
C22 470PF
(2MS)
R6 2.4K
R7 10K
4K LS221
4J LS74
5N LS00
3L LS74
3H LS28
SHT 2/A5
E2
EXT CLK
R5 510
TO ADC BOARD
TRACK
ADC CUT
DARDY
TRACK/HOLD
SHT 1/H5, 2/A4
SHT2/A4
F(11)·S2
QBUF
6L LS00
NOC LATCH
LS151
3G
1G
LS197
32 CH
16 CH
8 CH
4 CH
2G
2F
LS04
SHT 3/A3
3/A3
3/A3
3/A3
3/A3
CAMAC
+6V
F1
3A
L1
CR1
IN4139
+5.3V
GND
C1 6.8MF
C2 6.8MF
C3~C20 .01MF
C31 200PF
R10 51
3N LS32
C23 620PF
(3MS)
R12 2.4K
NOTES
1. ALL RESISTOR VALUES ARE IN

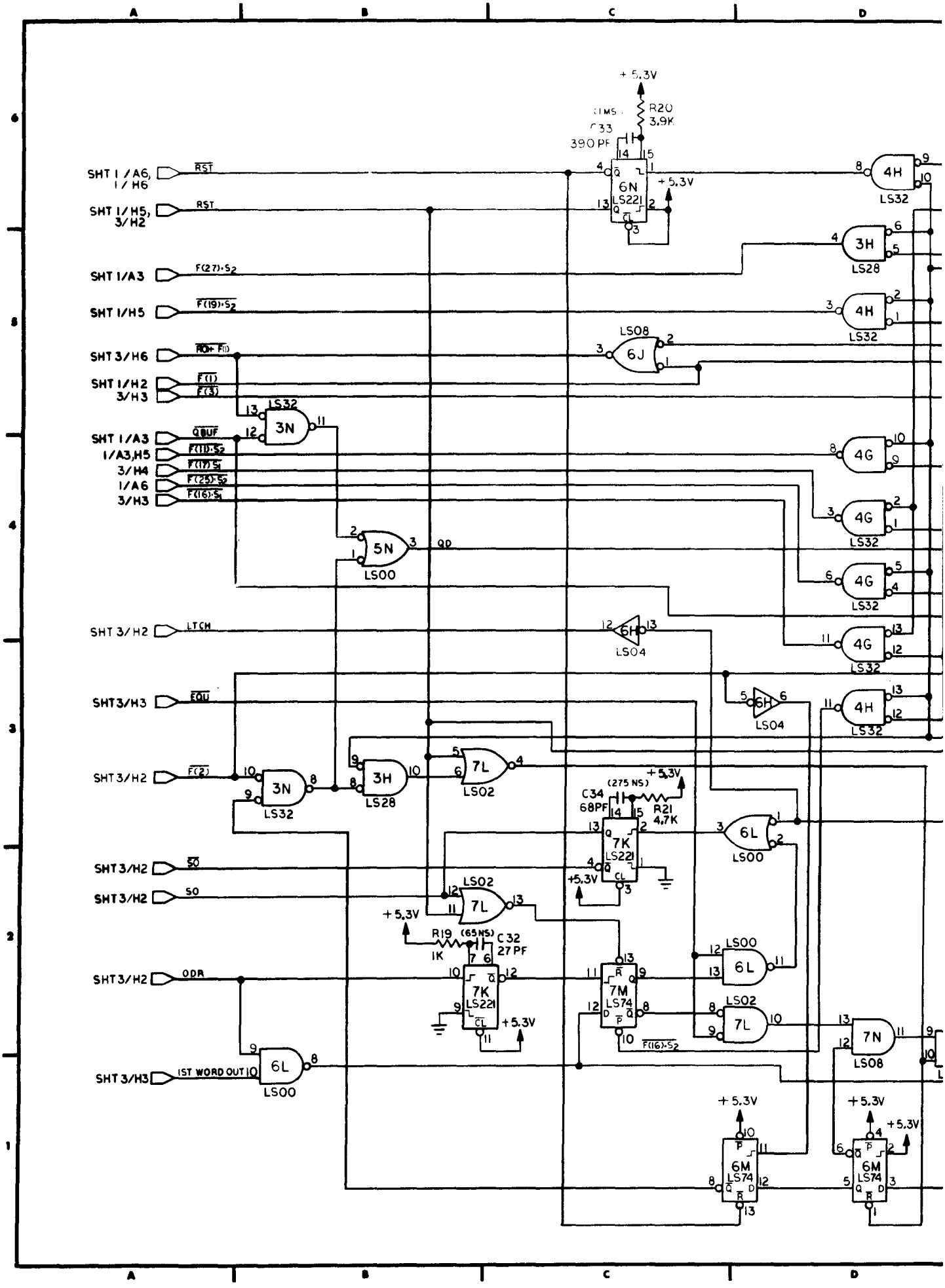


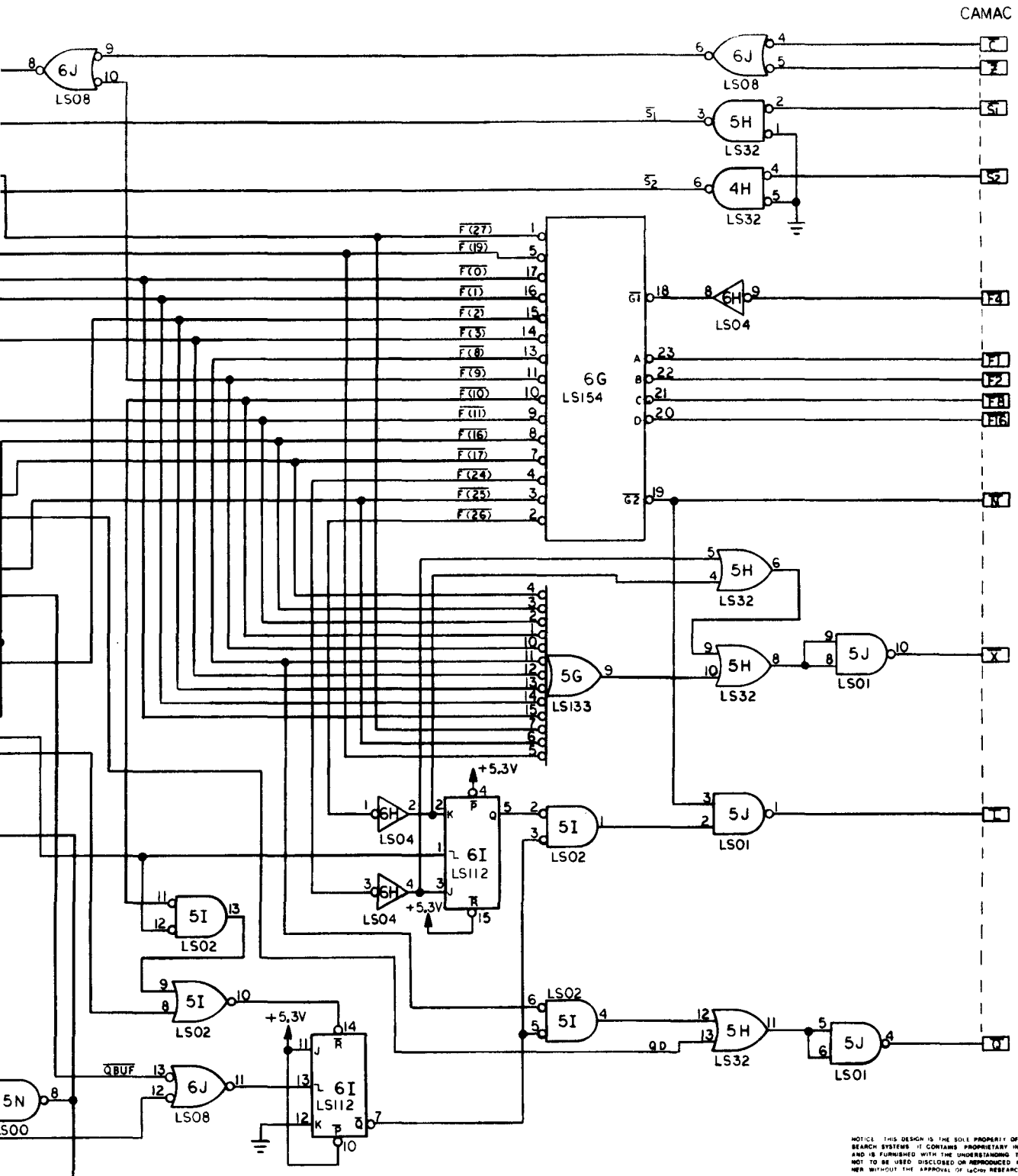
OHMS.

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
R22	
C34	
CR1	
L1	
F1	
E2	
Y1	

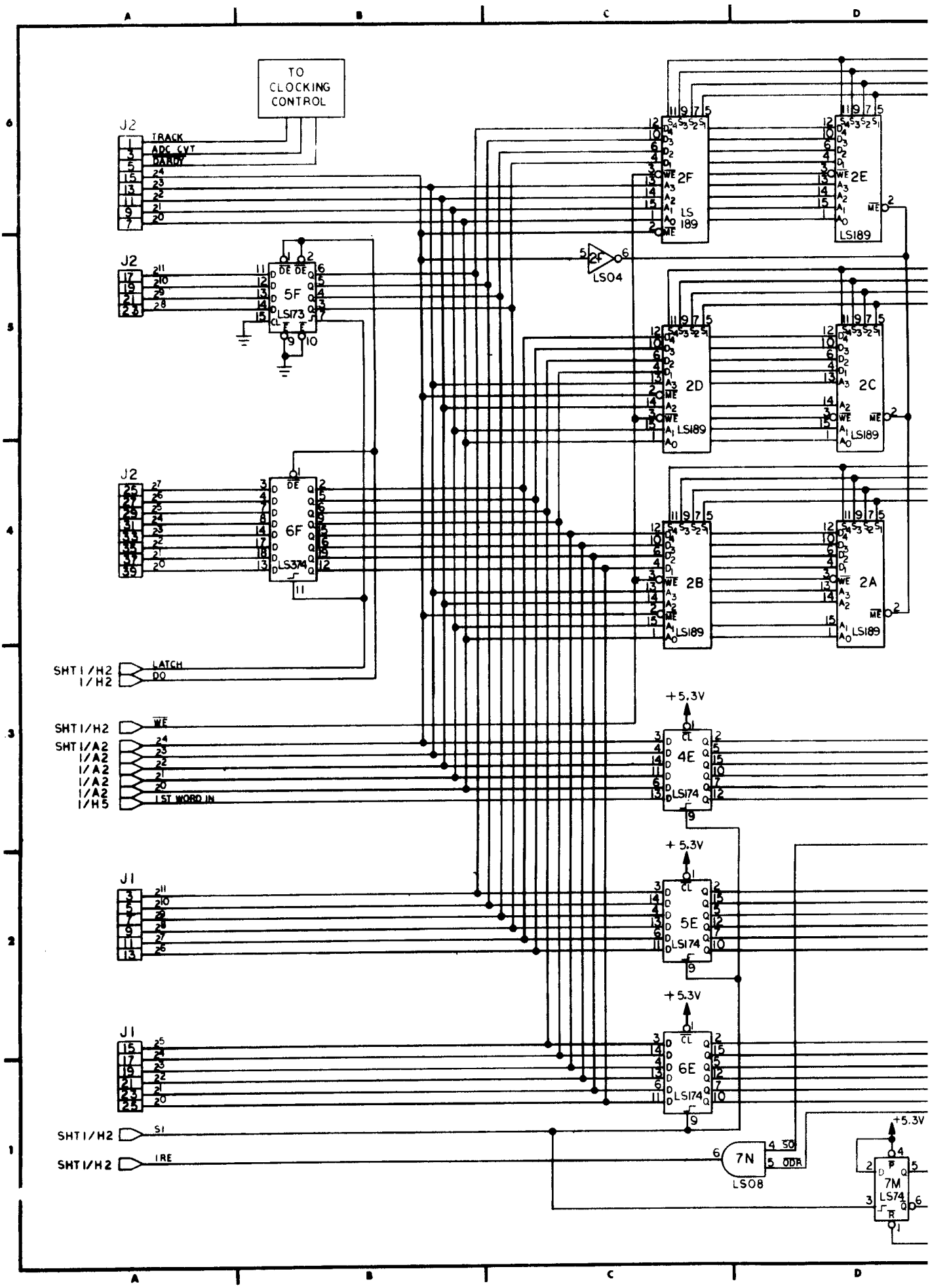
LeCroy RESEARCH SYSTEMS

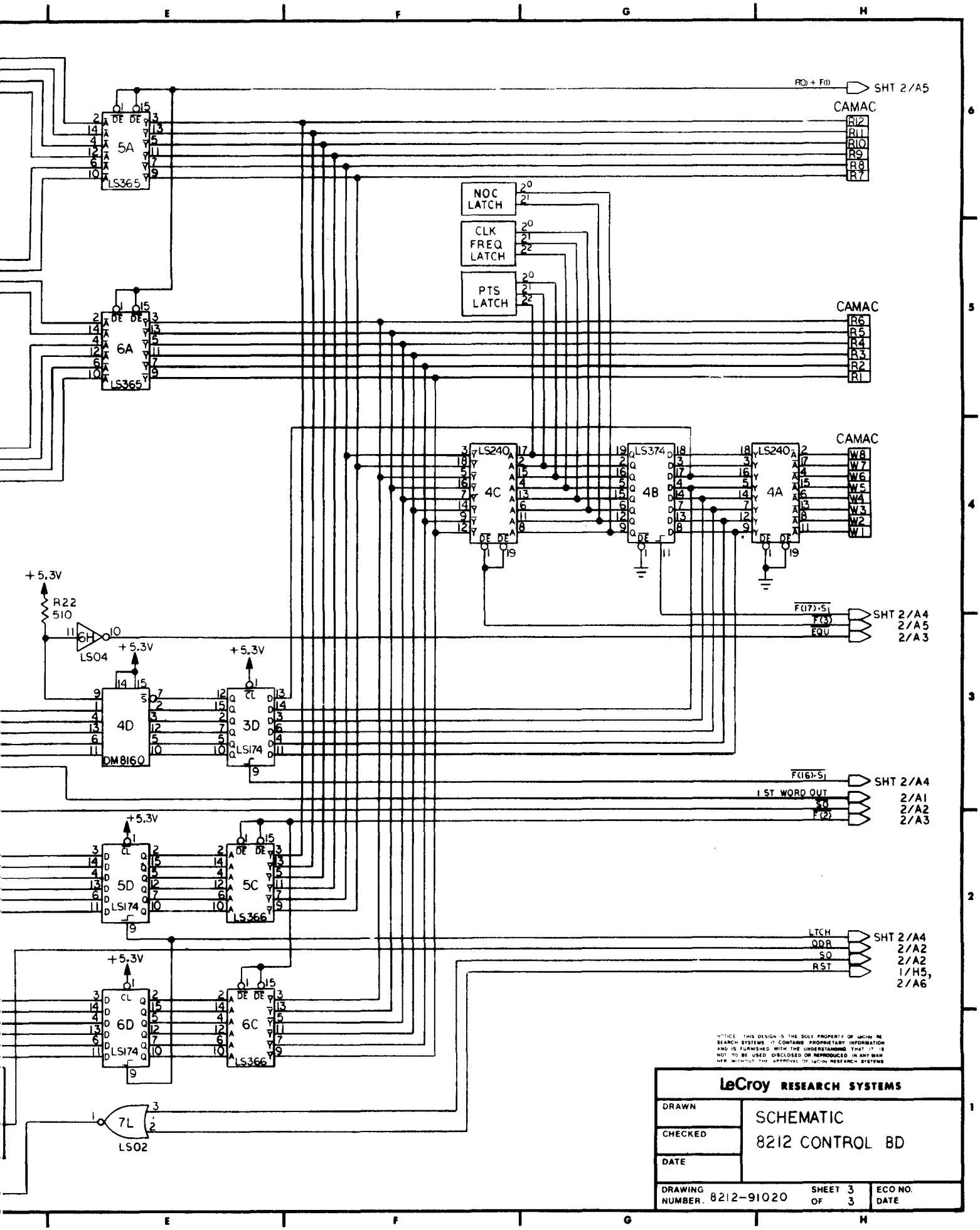
DRAWN CWP	SCHEMATIC – 8212 CONTROL BD
CHECKED	
DATE 8 / 8 / 78	
DRAWING NUMBER: 8212-91020	SHEET 1 OF 3
ECO NO.	DATE


SHT 1/A6, 1/H6
RST
SHT 1/H5, 3/H2
RST
SHT 1/A3
F(27)·S2
SHT 1/H5
F(19)·S2
SHT 3/H6
RO+F(1)
SHT 1/H2 3/H3
F(1)
F(3)
SHT 1/A3
QBUF
1/A3,H5
F(11)·S2
3/H4
F(17)·S1
1/A6
F(25)·S2
3/H3
F(16)·S1
SHT 3/H2
LTCH
SHT3/H3
EQU
SHT3/H2
F(2)
SHT3/H2
SO
SHT3/H2
SO
SHT3/H2
ODR
SHT3/H3
1ST WORD OUT
+5.3V
R20 3.9K
C33 390 PF
6N LS221
4H LS32
3H LS28
4H LS32
LS08 6J
4G LS32
4G LS32
5N LS00
QD
4G LS32
6H LS04
4G LS32
6H LS04
4H LS32
3N LS32
3H LS28
7L LS02
C34 68PF
(275 NS)
R21 4.7K
7K LS221
6L LS00
7L LS02
R19 1K
(65NS)
C32 27 PF
7K LS221
7M LS74
6L LS00
7L LS02
6L LS00
F(16)·S2
7N LS08
6M LS74
6M LS74



LeCroy RESEARCH SYSTEMS			
DRAWN	SCHEMATIC — 8212 CONTROL BD		
CHECKED			
DATE			
DRAWING NUMBER: 8212-91020	SHEET 2 OF 3	ECO NO. DATE	


TO CLOCKING CONTROL
J2
TRACK
ADC CVT
DATRDY
5F LS173
6F LS374
2F LS 189
2E LS189
2D LS189
2C LS189
2B LS189
2A LS189
2F LS04
SHT I/H2 LATCH
I/H2 DO
SHT I/H2 WE
SHT I/A2
I/A2
I/A2
I/A2
I/A2
I/H5 I ST WORD IN
+5.3V
4E LS174
5E LS174
6E LS174
J1
SHT I/H2 SI
SHT I/H2 IRE
7N LS08
7M LS74


F(0) + F(1)
SHT 2/A5
CAMAC
R12
R11
R10
R9
R8
R7
5A
LS365
NOC LATCH
CLK FREQ LATCH
PTS LATCH
6A
R6
R5
R4
R3
R2
R1
4C
LS240
4B
LS374
4A
W8
W7
W6
W5
W4
W3
W2
W1
+5.3V
R22
510
6H
LS04
F(17)·S1
F(3)
EQU
SHT 2/A4
2/A5
2/A3
4D
DM8160
3D
LS174
F(16)·S1
1 ST WORD OUT
SO
F(2)
2/A1
2/A2
5D
5C
LS366
LTCH
QDR
SO
RST
2/A6
6D
6C
7L
LS02
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LeCroy RESEARCH SYSTEMS. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCroy RESEARCH SYSTEMS
LeCroy RESEARCH SYSTEMS
DRAWN
CHECKED
DATE
SCHEMATIC
8212 CONTROL BD
DRAWING NUMBER. 8212-91020
SHEET 3 OF 3
ECO NO.
DATE