OPERATOR'S MANUAL

MODEL 3412/3412E

16-CHANNEL, 200 MHz CAMAC DISCRIMINATOR

CE

PRELIMINARY
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LeCroy

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CE CONFORMITY

CONDITIONS FOR CE CONFORMITY

Since this product is a subassembly, it is the responsibility of the end user, acting as the system integrator, to ensure that the overall system is CE compliant. This product was demonstrated to meet CE conformity using a CE compliant crate housed in an EMI/RFI shielded enclosure. It is strongly recommended that the system integrator establish these same conditions.

CAUTION

COOLING

The high power dissipation of the Model 3412 requires that it be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature at less than 50° C.

6 V POWER REQUIREMENT

The 3412 uses significant power from -6 V power line. -Be sure that your crate can supply enough current to this and other modules, especially if multiple 3412s are to be used.

INSTALLATION

Crate power should be turned off during insertion or removal of modules to avoid possible damage caused by momentary misalignment of contacts.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

NOTE: Except where differences occur, references to Model 3412 also include Model 3412E.

TABLE OF CONTENTS

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

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Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for more information.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

SERVICE PROCEDURE

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department at (914) 578-6030.

PRODUCT DESCRIPTION

OVERVIEW

The LeCroy Model 3412 is a 16-input discriminator in a single width CAMAC-module. The module accepts NIM-level inputs and operates to 200 MHz. The outputs of the 3412 are differential ECL-levels which are compatible with LeCroy's ECLine series of programmable logic modules. Output widths are adjusted from less than 5 to over 100 nsec.

Each of the 16 channels share a common threshold which is set by a front-panel potentiometer or via CAMAC commands. The threshold range extends from -10 mV to -1.034 V for Model 3412 and -15 mV to -1.034 V for Model 3412E. The unit also has a common front-panel VETO input as well as a TEST-input. However, the TEST mode can also be initiated by CAMAC commands and only the desired channels can be tested using a CAMAC write mask, or Ext Rear panel mask. If either the CAMAC or Rear Panel Inhibit is true the selected channel will be inhibited. In addition, the unit has a sum output which generates a current proportional to the input multiplicity.

The high density is made possible through the use of 16 MDC100 custom IC chips. These chips enhance the reliability of the Model 3412 as well as provide for the 200 MHz counting rate operation.

The Models 3412 and 3412E have the same circuitry except for one potentiometer value. R331 is 10 kΩ for the 3412 and 20 kΩ for the 3412E.

SPECIFICATIONS

Input

Signal Inputs: Sixteen inputs via Lemo front-panel connectors. Protected to ±2 A for 0.5 μsec. Reflections < 5% for input pulses of 3.5 nsec rise time for amplitudes up to -1 V. Input offset voltage typically ±3 mV. Minimum input width is 3 nsec.

Signal Input Threshold (see note below): -1.023 V to +0 V ±(5% or 2 mV, whichever is greater) common to all channels; front-panel screwdriver adjustment in local mode or through 12-bit DAC in remote mode (0.25 mV resolution). Stability better than 0.3%/°C to 60°C operating temperature. Threshold monitor point on front panel has 10:1 ratio of monitor voltage to actual voltage ±5%; minimum usable threshold is 8 mV ±2 mV for 3412 and 12 mV ±3 mV for the 3412E.

Note: $V_T = \frac{-X}{4095}$ (1024) - 10 mV (15 mV for 3412E)

where V_T = Threshold Voltage in (mV) and X = DAC-Counts (0-4095)

Signal Input Hysteresis: Approximately 5 mV for 3412 and 6 mV for 3412E.

Test Input: One Lemo connector on front panel, 50 Ω ±2%, triggers all enabled channels. Requires NIM level signal (< -600 mV). Minimum width, 6 nsec. Maximum rate, 20 MHz. Rise time < 2 nsec.

Veto Input: One Lemo front-panel connector, 50 Ω ±2%. Permits simultaneous fast inhibiting of all channels. Requires NIM level signals. Direct coupled. Must precede input signal by approximately 6 nsec. Minimum duration, 8 nsec.

Individual Inhibits (masking): 16 differential (110 Ω twisted pairs) ECL lines ("Emitter ORed" with CAMAC mask) inhibit selected discriminator channels. Differential True signals inhibit channel; unconnected inputs go to False or uninhibited state; 34-pin rear-panel connector.

Output

Discriminator Outputs: Two separate outputs per channel. ECL level (-0.8, -1.7 V) into 100 Ω twisted-pair. Duration: approximately < 5 nsec to > 100 nsec, continuously variable via screwdriver control in the Local mode or by CAMAC control in Remote mode. Common to all channels. Rise times and fall times < 2 nsec. Output pulse width matching < ±10% at widest width.

Current Sum Out: Rear-panel Lemo, high impedance current source sinks a current proportional to the input multiplicity at a rate of 1 mA ±10% per hit (50 mV per hit into a 50 Ω load) for output width > 15 nsec.

Output Operation Modes: Non-updating or Updating with or without Burst Guard. The modes are selectable by a side-panel DIP switch in Local mode or CAMAC control in Remote mode.

General

Maximum Rate: 200 MHz guaranteed.

Time Jitter: 30 psec for inputs of constant amplitude.

Mode Select: Local mode and remote mode selectable via CAMAC command, or front panel push-button to enable Local mode.

LED Indicators: Two front-panel LEDs indicate that Remote mode and N have been selected.

Double Pulse Resolution: 5 nsec typical.

Time Slewing: Less than 500 psec for input amplitudes from 2x to 20x over threshold.

Input-Output Delay: < 8 nsec. Delay matching better than ±950 psec.

Test-Output Delay: 11 nsec typical, 13 nsec maximum.

Remote to Local Switch: Recessed front panel forces unit from remote to Local mode.

Packaging: RF-shielded, CAMAC #1 module.

Power Requirements: 2.5 A at -6 V; 1.4 A at +6 V; 30 mA at -24 V; 60 mA at +24 V.

Environment: Proper operation of the 3412 requires +25°C air intake with sufficient airflow to maintain temperature rise of exhaust air to < 20°C.

Timing Characteristics

Double Pulse Resolution: 8 nsec typical. The speed of a discriminator is practically defined by its double pulse resolution or the time between the leading edges of the most closely spaced pulse pairs for which the discriminator produces two distinct output pulses. Although simple in

concept, this specification can be misleading unless the input conditions are precisely defined and ambiguities in performance are disclosed. One should indeed investigate the double pulse resolution as a function of the input amplitude over threshold and of the input width.

Tracking Error: The ability of a discriminator to be used for precise timing (coincidence or TOF) in an environment which encounters narrow pulse pair separations is demonstrated by considering the time shift (or tracking error) introduced as the time interval between successive inputs is reduced. In an experiment, tracking error is equivalent to time dispersion as a function of input rate. For many experiments, this can be critical, since it is often in high rate situations that the best timing resolution is required.

Time Slewing: < 500 psec for input amplitudes from 2 times to 20 times over threshold. Slewing is the variation in propagation delay from the beginning of the pulse input to the output pulse as a function of input pulse amplitude. The intrinsic slewing is measured as a function of input crossing threshold to output pulse. In addition, pulses of varying rise times give different delays from the beginning of the pulse since the threshold crossing time relative to the pulse's leading edge depends upon the amplitude the pulse. Only the intrinsic slewing is specified for the Model 3412 since rise time slewing is application dependent. Slewing is typically measured as the difference between propagation delay for input pulse amplitudes twice that of threshold and input pulses whose amplitudes are 20 times threshold. Threshold is defined as the input pulse level which results in discriminator firing for 50% of the pulses.

CONTROL AND CONNECTORS

Signal Input

Signal input to each of the 16 channels is made via a front-panel Lemo connector. The inputs of the 3412 discriminator are protected to 2 A for 0.5 μsec.

The DC-protection is limited by the 0.125 W dissipation limit of the input resistor, which can be assumed to offer protection against DC-signals less than 25 V.

Threshold

The threshold range is from -10 mV to -1.034 V for the 3412 and -15 mV to -1.034 V for the 3412E. It is adjustable by a front-panel, 10-turn potentiometer. Threshold is increased by turning this control clockwise. Alternatively, threshold can be programmed by CAMAC F(16)(A1) command. In either case, threshold is common to all channels and the adjustment is uniform and does not present any discontinuity or changes in sensitivity.

A front-panel test point is a 10:1 monitor of the actual threshold value within ±5%.

Test Input

A front-panel Test input allows all channels to be triggered once a negative NIM pulse is received. This useful feature allows complete testing of the module without removing any input cable and also permits the use of the 3412 as a 32-fold fan-out. The Test pulse will have the same effect as a similar pulse on the normal inputs.

VETO Input

A common front-panel Lemo input connector allows vetoing of all channels simultaneously, when a negative NIM pulse is applied. A complementary NIM signal applied to the VETO input permits the 3412 to be used as an 16-channel strobed coincidence unit. In other words, the discriminators will only generate an output when the input level exceeds the set threshold and while these signals occur during a logical 0 (≥ -100 mV) state of the complementary input to the VETO.

However, the action of the VETO input can be different depending on the operation mode of the unit (Updating or Burst Guard) and on the static level of the VETO input.

Updating Mode: In the Updating mode, the leading edge of the input pulse triggers the discriminator timing stage. A VETO input must be coincident and precede the input pulse leading edge by 1 nsec for the input to be inhibited.

Burst Guard Mode (Time-Over-Threshold): When the Burst Guard section is enabled an overlap coincidence between the discriminator output and the VETO-pulse is activated. A negative VETO-pulse of the same width as the discriminator output will VETO the output during this time. If a pulse wider than the VETO-pulse is applied at the input, an output will result due to the part of the pulse exceeding the VETO. Therefore, an efficient VETO-should completely overlap the input pulses.

The same applies when a complementary NIM-VETO pulse is used to gate or enable the module. The gate pulse should completely overlap the input pulses. In this case, the unit is working as a strobed overlap coincidence unit.

Output

The output of the 3412 is differential ECL pulse pairs suitable for driving twisted-pair cables. Two outputs per channel are provided from two 34-pin front-panel connectors.

The output of selected channels in the TEST-mode can be disabled or masked by loading a 16-bit word via CAMAC F(16)•A(0) command into a storage register, “or” by applying an ECL “1” logic level to the rear panel mask input.

Width Adjustment

The output width is common for each channel and is continuously adjustable via a front-panel potentiometer or via CAMAC-F(16)•A(2) from < 5 nsec to > 100 nsec. Minimum width is set by turning the potentiometer fully counter clockwise. See Figure 1.

The main contributors to output width uncertainty are a function of the external conditions. Variations in both temperature and supply voltage can cause significant changes in output width.

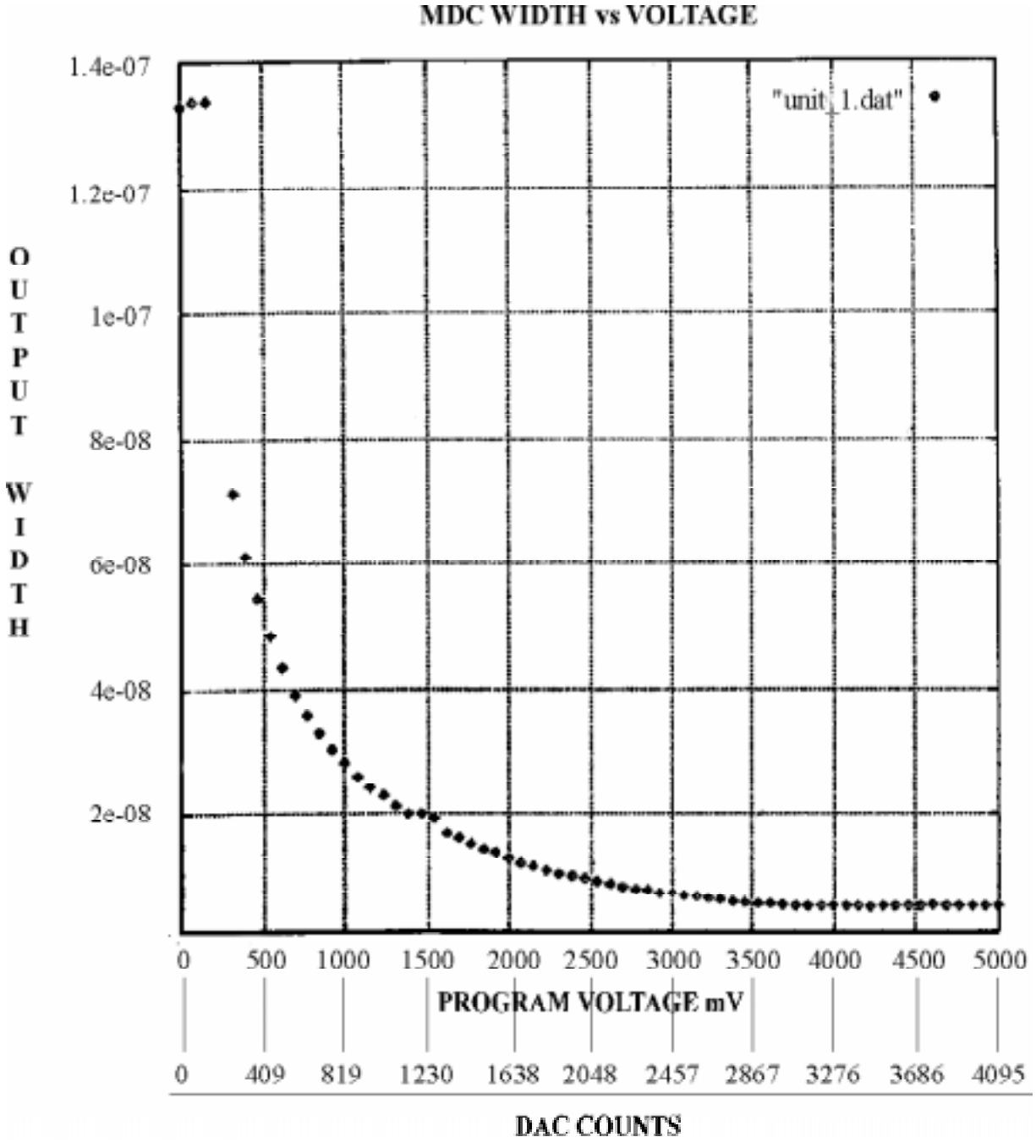
MDC WIDTH vs VOLTAGE
"unit_1.dat"
1.4e-07
1.2e-07
1e-07
8e-08
6e-08
4e-08
2e-08
OUTPUT WIDTH
0
500
1000
1500
2000
2500
3000
3500
4000
4500
5000
PROGRAM VOLTAGE mV
0
409
819
1230
1638
2048
2457
2867
3276
3686
4095
DAC COUNTS

Figure 1

Current Sum Output

An analog signal which is proportional to the number of channels which exceed the threshold is available via a rear-panel Lemo connector. This analog majority information consists of 1 mA ±10% per enabled channel for the duration of that channel (minimum of 15 nsec). When the sum output is used with 50 Ω loads, the output is 50 mV/hit. The output amplitude is limited to a maximum of -0.8 V. Figure 2 shows an example of the current sum output.

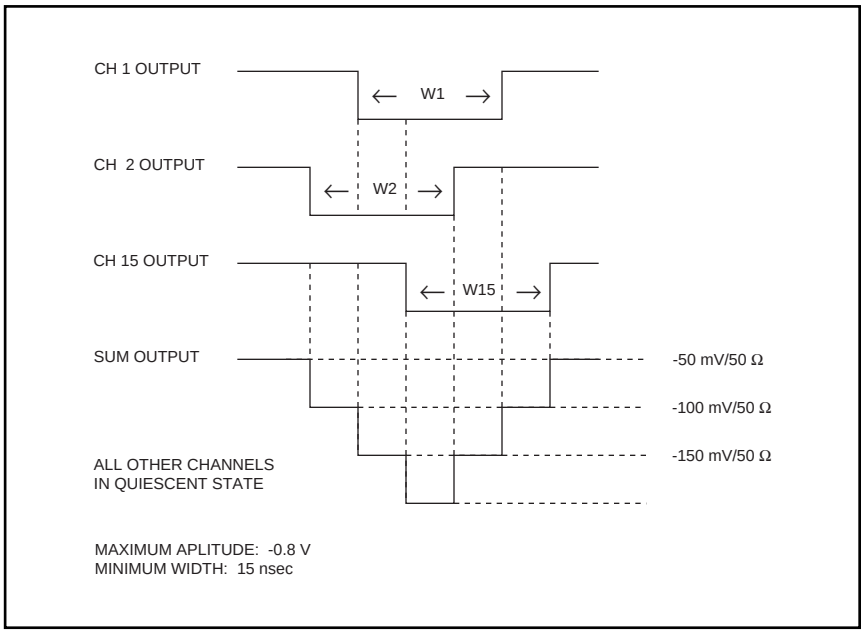

Figure 2

Updating/Burst Guard Switch

The module has a side-panel DIP switch which allows the selection of the operational mode.

Updating: In Updating mode, the output is extended if a second pulse arrives before the first output returns to zero, as long as the second pulse arrives at a time later than the double pulse resolution of the unit. Thus, the second pulse will be seen by the front end of the unit even though an output pulse is still present from the first signal. The second pulse will cause a new output to be generated and added (in time) to the portion of the original output already occurring.

Updating mode is controlled by switch position 1 on the DIP switch block, when the unit is set to “LOCAL”, or by the command F(16)•A(3) N•S1(W1), when the unit is set to “REMOTE” (see CAMAC-Function Codes).

Burst Guard: In Burst Guard mode, the output of the front end is OR’d with the conventional mode output. For input pulse arriving at a rate which exceeds the double pulse resolution of the unit, the discriminator output duration will be equal to the time interval between the first leading edge threshold crossing and the last trailing edge threshold recrossing or the preset output width, whichever is greater.

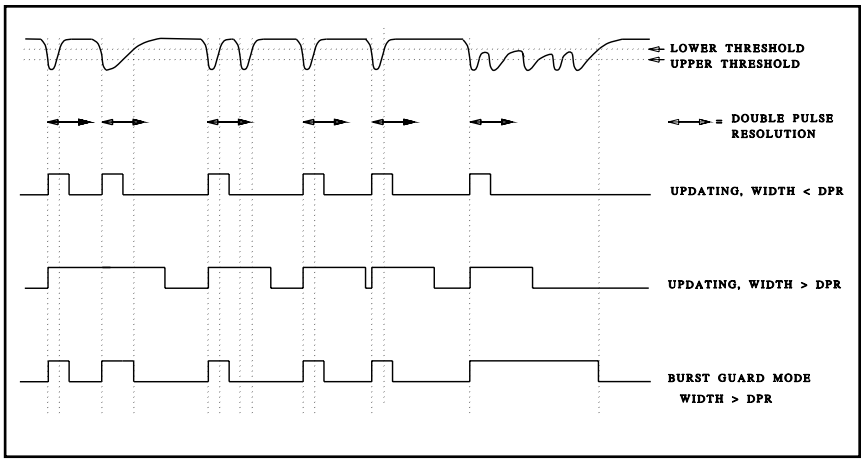

Figure 3

This feature is especially important in veto applications when the discriminator output must be enabled as the detector is hit by unwanted and immeasurable high rates. A discriminator without Burst Guard would see the first pulse and generate the preset output width, but would be paralyzed at quiescent level or would trigger only randomly for subsequent pulses separated by less time than the DPR of the unit. Burst Guard assures a logical 1 output level during these high rate bursts.

Burst Guard mode is also useful in any application where the output width has to be proportional to the input width.

Burst Guard mode is controlled by switch position 2 on the DIP switch block, when the unit is set to “LOCAL”, or by the command F(16)•A(3)N•S1(W2), when the unit is set to “REMOTE” (see CAMAC-Function Codes).

CAMAC COMMANDS AND FUNCTION CODES

The commands for the 3412 conform to the CAMAC Standard-IEEE Std. 583-1975. If the user is unfamiliar with the CAMAC standard, a good reference is “*CAMAC-Instrumentation and Interface Standards”*. It is published by: The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY-10017.

Commands

I:	Inhibits all discriminator channels.
Z•S2:	Clears all registers. Sets Local/Remote to Local.
C•S2:	Clears all registers. Sets Local/Remote to Local.
X:	Generated for all valid functions.
Q:	Generated if a function can be executed.

Function Codes

F(0)•A(0) N:	Reads mask (R1-R16).
F(0)•A(1) N:	Reads Threshold (R1-R12).
F(0)•A(2) N:	Reads Width (R1-R12).
F(0)•A(3) N:	Reads Updating Status (R1). 1 = Updating, 0 = Non-Updating.
F(0)•A(3) N:	Reads Updating Status (R2). 1 = Burst Guard On, 0 = No Burst Guard.
F(16)•A(0) N S1:	Writes Mask (W1-W16).
F(16)•A(1) N S1:	Writes Threshold (W1-W12).
F(16)•A(2) N S1:	Writes Width (W1-W12).
F(16)•A(3) N S1:	Sets Updating Mode (W1). 1 = Updating, 0 = Non-Updating.
F(16)•A(3) N S1:	Sets Burst Guard (W2). 1 = Burst Guard, 0 = No Burst Guard.
F(24)•A(0) N S1:	Set to Local mode.
F(25)•A(0) N S1:	Test.
F(26)•A(0) N S1:	Set to Remote mode.
F(27)•A(0) N S1:	Checks Remote/Local mode. Q = 1 only if in Remote mode.

Note: The 3412 will power up in the Local mode. In Local mode the user can set the threshold and width by front-panel pots, the mode of the discriminator (Updating and Burst Guard) can be set by a side-panel DIP switch.

INSTALLATION

GENERAL

The LeCroy Model 3412 is a CAMAC-module and as such, must be installed in a CAMAC-crate. It is intended for use within a standard CAMAC crate, such as the LeCroy Model 8025 CAMAC Crate with 25 slot positions or the Model 8007A with 7 positions. The following voltage sources must be properly connected to the backplane: +24 V, +6 V, -6V, and -24V. Each crate must be controlled by either a slave or intelligent controller. The controller must occupy the right-most slot in the crate. Its purpose is to issue CAMAC commands to the modules and transfer information between a computer (or other digital device) and the CAMAC modules. LeCroy offers such crate controllers, including the Model 8901A. The 8901A is a GPIB/CAMAC slave interface that operates as a “Talker/Listener”, allowing the crate to act as one GPIB instrument.

With the power off, the 3412 is inserted into one of the slots of the CAMAC crate. The edge connector on the module should mate with the bus connector with modest pressure. The thumb screw located on the lower edge of the card should be engaged and tightened. Note the slot number of the module, as it will later be used for addressing.

Care must be taken to ensure the crate power is off before the module is installed. It can be installed in any slot except the crate controller slot (slots 24 and 25).

The 3412 requires significant power from the crate due to its high working frequency. It should be determined prior to installation whether the crate can support one or more 3412s with other modules which are to be used in the crate.

One the unit is in the crate, input signals must be applied to the front-panel connectors. Then the minimum output width must be adjusted via the front-panel potentiometer and the threshold set either by the front-panel control or via CAMAC commands. The threshold can be monitored via a front-panel test point with a voltmeter. The output of this connector is a 10 to 1 ratio with the actual applied threshold voltage level.

To complete cable connections to the 3412, the VETO, and Test signals, if utilized, must be connected. Of course, outputs of the unit must be connected to associate units including the current sum output if desired.

CABLES

Interconnections between the output of the Model 3412 and various other ECLine modules can be made either by multiwire cables or by single twisted-pair cables for one-to-one connections suitable for the transmission of differential ECL-pulse pairs. Such interconnecting cables can be purchased from LeCroy. In particular there are two types of 34 conductor multiwire cables available, one for short connections using flat cable and the second for long connections using twisted and flat ribbon cable.

The model number of such cables are as follows:

- **STP-DC/02-L -** single twisted pair cable for control signals.
- **STC-DC/34-L -** flat multiwire cable for short interconnections.
- **LTC-DC/34-L or DC2/34-L -** twisted-pair multiwire cable for long interconnection.

Note: "L" is the cable length in feet that must be specified by the user. All signal inputs are differential ECL and have a balanced 120 ohm termination.

Inputs to the 3412 are lemo connections so that standard Lemo-to-Lemo cables can be used such as the following LeCroy cables:

480-122-301	3 ft RG-174 cable
480-101-003	1 ft RG 174 cable
480-216-002	6 ft RG-58/L cable

GENERAL

Setup of the Model 3412 can be split into four categories: adjustment of the threshold and output width, setting up the veto input, and initiating the Test mode.

Threshold

The main function of the discriminator is to generate a logic pulse output when the input exceeds a given threshold. Therefore, correct adjustment of the threshold is one of the most important duties to be performed.

The threshold is adjusted via a front-panel potentiometer or programmed via CAMAC. The resulting change in threshold level is monitored with a high impedance voltmeter connected to the front-panel probe point. This voltage is 10x the actual threshold voltage. The threshold can be set at some level which corresponds to a physical quantity (i.e., 100 mV may equal 100 keV) or it can be set above the noise level depending on the application. In either case, it is necessary to determine the level that the threshold should be set to. This action may be as easy as measuring the maximum noise level input or as complex as calibrating the system by accurately determining the relationship between pulse height (voltage level) and some quantity.

There are several phenomena to be aware of when setting the threshold since the actual value can be a function of environmental conditions as well as internal properties of the module itself.

Threshold Uncertainty

The external factors with the strongest effect upon the threshold value are the temperature coefficient of threshold and the power supply coefficient of threshold. Combining these, the actual threshold vale VT is given by:

VT: Threshold according to front-panel control setting ± DC offset + hysteresis/2 ± temperature coefficient X temperature change from calibration temperature ± supply coefficient X voltage change from nominal supply voltage.

Threshold Hysteresis

The 3412 discriminator has 5 mV hysteresis built into each MDC100. Every threshold crossing will not trigger the discriminator unless the previous signal has returned to below, for example, approximately -25 mV for threshold setting of -30 mV. This feature avoids multiple pulsing due to fine structure riding on a flat-topped pulse that may bring the pulse above and below threshold. The two examples in Figure 4 illustrate this point.

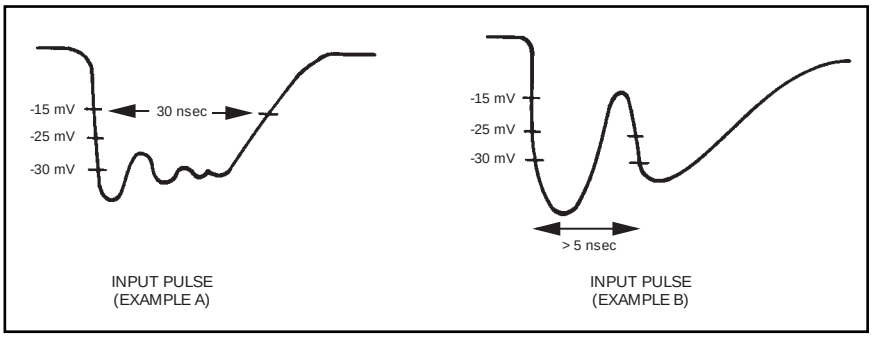

Figure 4: Examples of input pulses with structure which results in only one pulse output (A) or more than one output pulse (B).

In Example A of Figure 4, the input pulse will not retrigger the discriminator if set for -30 mV threshold, even though it crosses the threshold level at a time exceeding the Double Pulse Resolution (DPR) of the unit.

In Example B of Figure 4, the input signal does go back through the threshold of -30 mV but goes beyond to exceed the threshold plus hysteresis level. Two discriminator output pulses would result.

Since LeCroy discriminators are most often used with photomultipliers and plastic scintillators, and since the characteristic pulses out of this type of detector are typically smooth for each individual event, multiple outputs should occur only when they represent multiple events.

OUTPUT WIDTH

The output of a discriminator is a logic pulse which can be used for various functions and purposes in the rest of the system. The output pulse width must be compatible with the equipment following the discriminator. However, the maximum repetition rate of the unit is limited by this width. Therefore, certain trade-offs may have to be made in determining the required output width.

The output width is adjustable via CAMAC control or a front-panel potentiometer. The width adjustment can be monitored by using a scope connected to one of the module's output connectors. Width is increased as the control is turned clockwise, or the DAC count is decreased.

The output width in the Burst Guard mode will either be equivalent to the time-over-threshold of the input or the preset width, whichever is greater.

Veto (Mask) Input(s)

The 3412 provides 4 mask functions, two are common to all 16 channels, and the other two inhibit only selected channels. The two provisions that are common to all 16 channels are the front-panel Fast Veto and the CAMAC “I” command. The Rear Panel and the CAMAC Mask select individual channels. A channel that is masked will not produce an output pulse under any input condition.

The front panel Veto inhibits the firing of all 16 channels when a NIM true logic level (-0.8 V) input pulse is applied. In order to be effective, the veto input pulse must precede the input by at least 6 nsec. In Update mode the veto input must overlap the leading edge of the input pulse. In burst guard mode the Veto must completely overlap the entire input pulse.

The 34-pin rear panel connector provides 16 individual 100 ohm complementary pairs to select the channels to be inhibited. An applied ECL logic “1” level will inhibit the respective channel. Any input that is unconnected (floating) will go to the false state and not provide an inhibit.

In the remote mode the user can also inhibit any individual channel by CAMAC control with a 16-bit word (W1-W16). Bits 1-16 in the data word correspond to discriminator channels 1 to 16 respectively. Since the 16 bit word is stored in an internal register, the 3412 will retain the Masking pattern and only update during S1 of a CAMAC F(16) A(0) cycle, or upon initialization.

The rear panel inhibit is OR'ed with the CAMAC inhibit. Both the CAMAC controlled inhibit and the Rear Panel Mask will prevent any inhibited channel from firing with a Test input as opposed to the front panel Fast Veto, and the CAMAC "I", which will not.

Test Mode

A test pulse is a very useful function for multi-channel discriminators. It allows a means for rapid checking of all discriminator channels without requiring an input signal that exceeds the preset threshold. The Test function is also useful for checking other units in the system following the discriminator. The 3412 provides two methods to supply a test pulse, locally by a front panel lemo and by a CAMAC controlled command in the remote mode. Either method will trigger all channels that are not masked and produce an output. The output pulse width will be determined by the setting of the Pulse Width pot in local mode and the CAMAC controlled Width DAC setting in remote mode.

A Nim logic "1" signal applied to the front panel Test input lemo will trigger any channel that is not masked by either the Rear panel or CAMAC Mask (individual channel mask). The front panel Fast Veto and the common CAMAC "1" will not mask the Test function. To initiate Test from CAMAC in Remote mode an F(25) command is required. This will trigger all unmasked channels.

THEORY OF OPERATION

GENERAL

The Models 3412 and 3412E have the same circuitry except for one potentiometer value; R331 is 10 kΩ for the 3412 and 20 kΩ for the 3412 E. The block diagram of the 3412 is shown in Figure 5. The 3412 consists of the following basic sections:

- 16 MDC100 Discriminator Chips
- Threshold Adjustment
- Width Adjustment
- Veto and Mask (inhibit) Circuit
- Test Circuit
- Analog Sum Circuit
- CAMAC Decoder

MDC100 DISCRIMINATOR CHIP

The 3412 front end consists of 16 custom designed bipolar chips. Each of the 16 channels uses 1 MDC100 chip. The chip is packaged in a 28-pin PLCC package. The MDC100 has built-in hysteresis to prevent misfiring due to fine structure riding on a flat topped pulse that may cross the threshold level many times. The amount of hysteresis is externally adjusted by a pot, common to all MDC100s, and set for about 5 mV. The signal applied to the input lemo connector of each channel is connected by a 50 ohm microstrip to the inverting input of the MDC100's comparator. The threshold level is applied to the non-inverting input of this comparator. When the input is large enough to cross the threshold level the output of the comparator switches from a high level to a low level. This negative going transition is applied as the clock to an internal D flop. If the specific channel is not masked by either the CAMAC Controlled Inhibit, Rear Panel Mask or the Front Panel Veto its D input will be forced to a logic "1". Upon receipt of the clock edge the flop will be triggered, and the Q output will be set to a logic "1" condition. The flop will remain set only long enough to start a timing ramp and then will be reset by the pulse timing section. It is this section that sets the width of the output pulse. The run up rate of the timing ramp and the threshold of the ramp comparator (used to sense the run up complete condition of the ramp) determine the output width. The current that is supplied to the ramp capacitor determines the run up rate, this current is set by "V Width". Likewise, the ramp comparator threshold voltage is also set by this voltage. Increasing V Width will increase the ramp run up current and also decrease the threshold level of the ramp comparator resulting in a decrease of the output width as shown in Figure 1.

The update mode will allow the channel to retrigger upon a second pulse crossing threshold before the first output pulse has timed out. The output pulse will be extended by the preset width. If the update mode is not true and a second pulse crosses the threshold before the first pulse has timed out, a logic gate forces the D input to a logic "0". This prevents the clock from triggering the flop, thereby ignoring the input.

In addition to a valid input pulse, the D flop can also be set by the Test input. This input DC sets the flop (provided that the masks are not true).

Threshold Adjustment (common to all 16 channels)

The threshold is adjusted by a front panel pot in local mode or by a 12-bit DAC in remote mode. The wiper of the pot and the output of the DAC are connected to an analog switch. If the mode is set to local, the pot's

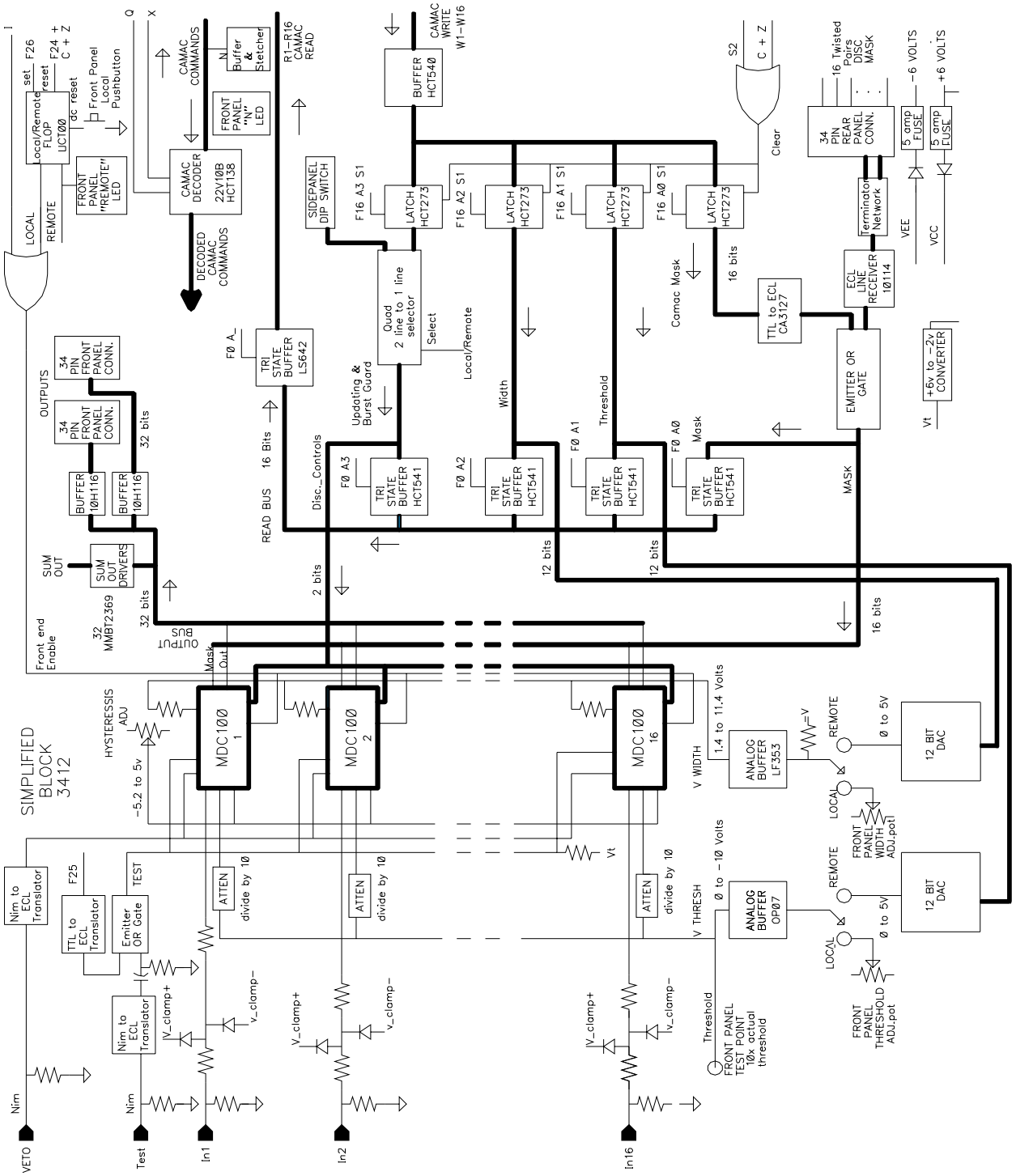

Figure 5: Model 3412 Block Diagram.

output is connected through the switch to the input of a buffer amplifier, if the mode is set to remote the DAC's output is connected through the switch to the input of the buffer amplifier. The buffer amplifier is configured to have an inverting gain of 2. The amplifiers output voltage (V THRESH) ranges from 0 to -10 Volts. A front panel Threshold test point allows the user to monitor this voltage. Each of the 16 MDC100s have a precision divide by 10 attenuator. The output of the attenuator is applied to the Threshold input of the MDC100.

In remote mode, the threshold is set by a 12-bit DAC (AD7245). A 12-bit data word written into a register (1_ HCT273's) during S1 time of the F(16) (A1) cycle, sets the input to the DAC. The output voltage Vo of the DAC is equal to 5(X/4095) Volts, where X = DAC count.

Width Adjustment (common to all 16 channels)

Similar to the Threshold adjustment, the width adjustment can be set by a front panel pot in local or a 12-bit DAC in remote mode. The 12-bit data word is written into its register during S1 time of the F(16) A(2) cycle. The output voltage of the DAC can be found using the same equation as used for Threshold Adjustment above. The circuits that control the width are very similar to the threshold except for the amplifier. In the width circuitry the amplifier is configured to provide a non-inverting gain of 2 with a 1.4 V DC offset. The amplifier's output level (V WIDTH) ranges from about 1.4 to 11.4 V. This allows the MDC100 output pulse width to range from less than 5 nsec to over 100 nsec. The output pulse width decreases as V WIDTH increases.

Veto and Mask (inhibit) Circuits

The 3412 has the following 4 methods to Mask the inputs:

1. **Front panel Fast Veto (Common to all 16 Channels)**
   The front panel Veto NIM level signal is buffered by an emitter follower (Q40) fanned out and supplied to one of the two front end enable inputs of each MDC100. The VBE drop of the emitter follower is all that is required to provide the translation from a NIM to an ECL level. In order to be effective, the leading edge of the veto must precede the input that is to be vetoed by at least 6 nsec. Internal to the MDC100, this signal forces the D input of a D flop to a logic "0" and prevents it from firing, thereby preventing an output pulse to occur with the 3412 set to NON Burst Guard mode. In Burst Guard mode the veto must completely overlap the input pulse in order to be effective.

2. **Rear Panel Mask (Individual Channels)**
   The Rear Panel Mask provides a method to mask any of the 16 channels by applying an ECL logic "1" level to the True input and an ECL "0" level to its Complementary input of the 16 pairs. Each of the 100 ohm pairs are terminated with two 56 ohm resistors in series between each pair, and their midpoints tied to ground through a 0.01ufd capacitor. Each pair is applied to the inputs of a ECL line receiver (10114). The true output of each line receiver is emitter OR'ed with the CAMAC Mask and applied to the Mask input of its respective MDC100. Internal to the MDC100 this mask forces the D input of the D flop to a logic "0" (as with the fast veto above). A logic gate in the MDC100 prevents the Test input from generating an output when the mask input is true.

3. CAMAC Mask (Individual Channels)
Each channel can also be masked by a supplying a CAMAC F(16) A(0) command along with a 16 bit data word (W1-W16). The data word will be latched into a 16-bit register (2-8 bit HCT273s) during S1 time. The contents of this register will be retained until the next CAMAC F(16) A(0) command is issued or the unit is cleared with a CAMAC C or Z command. The Q output of each register is converted from TTL logic levels to ECL levels (required by the MDC100s) by a resistive attenuator and a level shifting stage. The output of this stage is emitter OR'ed with the Rear Panel Mask and applied to the Mask input of its respective MDC (see Rear Panel Mask).

4. CAMAC Inhibit (Common to all 16 Channels)
The CAMAC Inhibit command I provides a mask to all 16 channels. This command is only active in Remote mode. One section of a quad, two input TTL OR gate (HCT132) provides this logic function. With the CAMAC I command in its true state (active low) the output of the OR gate will also be low provided that the 3412 is in the Remote mode. This TTL level is attenuator and level shifted by a resistive voltage divider and an emitter follower (p/o U24 ca3127), to provide the required ECL logic levels for the MDC100s. The output of this circuit drives one of the two Front End Enables on each of the 16 MDC100s. An ECL logic "0" level at this input forces the D input of the internal flop also to a "0" logic level preventing the flop from being triggered, thereby masking the input.

TEST CIRCUIT

The 3412 provides two means to apply a test pulse to the 16 MDC100s, either by a front panel lemo (NIM) or under CAMAC control. The NIM signal applied to the lemo is level shifted by an emitter follower (Q41) to provide a ECL logic "0" level to one input of a hex inverter (10H189). The output of this inverter is AC coupled to the input of another inverter, with about a 50 nsec time constant. The CAMAC controlled test circuit's output is also connected to this input. Both signals form an OR function to provide an ECL logic "0" level pulse to the Test* inputs of all 16 MDC100s. The CAMAC controlled Test signal must be translated from TTL logic levels to ECL levels before it can drive the input of the inverter. This function is provided by a resistive attenuator and an emitter follower (Q2).

Analog Sum Circuit

The output and its complement of each MDC100 drives a discrete differential stage with a standing current of 1 mA. One collector of the differential pair (2 BFR92As) is returned to ground, the other is connected to the Sum Out lemo on the rear panel of the 3412. The output current is diverted to ground for a channel that is not triggered. The output current for a channel that is triggered flows through the collector that is connected to the lemo. This provides 1 mA to the external 50 summing resistor, except for when a channel fires this 1 mA of current flows though the common summing resistor (external to the 3412 and usually 50 ohms), thereby producing a -50 mV level for each channel that is fired.

CAMAC Decoder

The majority of the CAMAC decoding is handled by a 22V10B TTL/CMOS PAL device and a HCT138 3 Line to 8 Decoder. All the A lines are decoded in the HCT138 the N line is used as an enable. The PAL generates a TTL logic "0" pulse during S2 time when F16 is true (and a valid A is also true) this pulse drives one input of four dual input OR

gates, the other inputs are driven by the decoded A commands. This allows the 16 bit data word (W1-W16) to be latched into its respective register during A(0). Likewise A(1) and A(2) latches the 12 bit data word for the threshold and width DACs respectively. A(3) latches the 2 bit data word for Update (W1) and Burst Guard (W2) modes. The state of these registers are read back at F(0) and their respective A commands.