Model 3232
Simultaneously Sampling
Transient Recorder

INSTRUCTION MANUAL

Aeon Systems Inc.
1704 Moon NE
Albuquerque, NM 87112

CHANGE RECORD

Rev.	Date	Description
A	9/85	Initial Release
B	6/86	Corrected Data in binary tables. Each bit has a value of 1.25 mv. Also the Module Gain status returned in the Status register (R11 and R12) has been corrected.
C	9/86	Correction of Fig. 2-1. Switch, Jumper and Controls to reflect Rev.4.0 control boards.

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1. INTRODUCTION

1.1 Modes of Operation

The Model 3232 Transient Recorder is a multichannel analog-to-digital converter with the following special features:

a. Simultaneous sampling. Each channel includes a track and hold amplifier so that all inputs can be sampled simultaneously on command.

b. Memory management. The 3232 incorporates control circuitry necessary to load digitized measurements into external memory modules and to unload the data onto the CAMAC dataway. Memory management provides for maximum utilization of memory no matter how many channels are in use.

c. Pre-trigger or post-trigger operation. In pre-trigger mode, the 3232 scans its inputs, digitizes and stores measurements in memory continuously until it receives a trigger signal. After the trigger, it digitizes and stores a specified number of additional measurements and stops. Since the 3232 writes and rewrites memory locations in a round robin fashion, the typical result of a pre-trigger operation is to have all of memory filled with new measurements, part of which were taken before the trigger signal was received. The number of measurements after the trigger is specified by a CAMAC command. In post-trigger mode, the 3232 begins scanning its inputs, digitizing and storing measurements when it receives a trigger signal. It continues scanning until the available memory is filled or until stopped by a CAMAC command.

d. Internal clock. Module timing and synchronization are accomplished by means of an internal clock. Several different clock rates are software selectable. An input is provided for an external clock signal. Triggering can be accomplished by an external signal or by CAMAC command.

e. Self test. A CAMAC command causes all the inputs to be connected to an internal reference waveform for the purpose of self testing.

1.2 Versions

The 3232 can accomodate up to 32 analog inputs. Model 3232 versions are as follows:

Model	Inputs	Packaging
3232-4	4	Single-wide module
3232-8	8	Double-wide module
3232-16	16	Double-wide module
3232-32	32	Triple-wide module

For each version, the number of active inputs up to the version maximum is set by a CAMAC command.

2. INSTALLATION

2.1 Unpacking and Inspection

The packing material in which the 3232 is shipped is specially designed to protect the module from physical damage and from damage due to electrostatic discharge. Aeon Systems recommends that you save this material in case it becomes necessary to ship the module back for repair.

Upon unpacking, inspect the module closely for shipping damage. This could include broken or missing components, loose screws, etc. If you find such damage, notify the carrier immediately.

2.2 Configuration

Before installing the 3232 in the crate, set the module's configuration by means of the switches and jumpers described in this section. These switches and jumpers are on the control board, which is the leftmost board in the module as viewed from the front. The positions of the switches and jumpers on this board are shown in Figure 2-1. Access to the switches is through openings on the module cover. Access to the jumpers is described in the appropriate sections below.

A. Input Amplifier

The polarity and gain of the analog to digital converter's input amplifier are set by the two dip switches located on the side of the module. The amplifiers can be set for either unipolar or bipolar inputs. The switch settings are as follows:

	SWITCH 2 (SW2)	
Input range	Section 1	Section 2
0 to +10.24 Volts	OFF	OFF
-10.24 to +10.24 Volts	ON	OFF
0 to +5.12 Volts	OFF	ON
-5.12 to +5.12 Volts	ON	ON

NOTE: "ON" position is toward front panel of unit

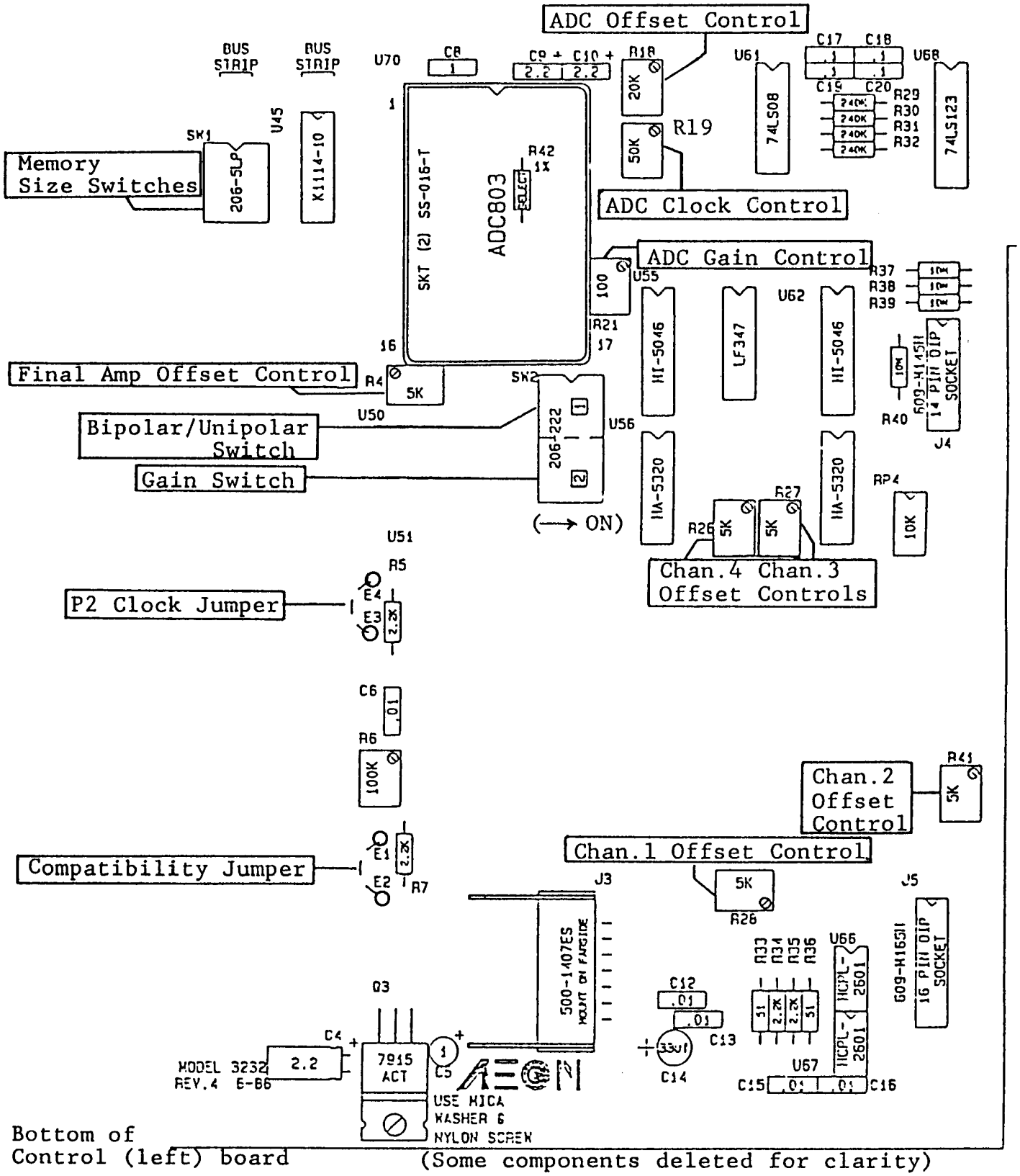


Figure 2-1. Switch, Jumper and Controls Positions

B. Memory Size

The size of available memory is set by the five dip switches located on the side of the module. The switches are set as follows:

Switch 1	Switch 2	Switch 3	Switch 4	Switch 5	Memory Size
ON	ON	ON	ON	ON	32K
ON	ON	ON	ON	OFF	64K
ON	ON	ON	OFF	ON	96K
ON	ON	ON	OFF	OFF	128K
ON	ON	OFF	ON	ON	160K
ON	ON	OFF	ON	OFF	192K
ON	ON	OFF	OFF	ON	224K
ON	ON	OFF	OFF	OFF	256K
ON	OFF	ON	ON	ON	288K
ON	OFF	ON	ON	OFF	320K
ON	OFF	ON	OFF	ON	352K
ON	OFF	ON	OFF	OFF	384K
ON	OFF	OFF	ON	ON	416K
ON	OFF	OFF	ON	OFF	448K
ON	OFF	OFF	OFF	ON	480K
ON	OFF	OFF	OFF	OFF	512K
OFF	ON	ON	ON	ON	544K
OFF	ON	ON	ON	OFF	576K
OFF	ON	ON	OFF	ON	608K
OFF	ON	ON	OFF	OFF	640K
OFF	ON	OFF	ON	ON	672K
OFF	ON	OFF	ON	OFF	704K
OFF	ON	OFF	OFF	ON	736K
OFF	ON	OFF	OFF	OFF	768K
OFF	OFF	ON	ON	ON	800K
OFF	OFF	ON	ON	OFF	832K
OFF	OFF	ON	OFF	ON	864K
OFF	OFF	ON	OFF	OFF	896K
OFF	OFF	OFF	ON	ON	928K
OFF	OFF	OFF	ON	OFF	960K
OFF	OFF	OFF	OFF	ON	992K
OFF	OFF	OFF	OFF	OFF	1024K

C. Compatibility Jumper

If the 3232 is to be operated in Princeton 908 compatibility mode (refer to Appendix A for more information on this mode), install a jumper between the jumper pads marked E1 and E2.

D. P2 Clock Jumper

In applications requiring synchronized operation of 3232 modules with other modules, the 3232 module can be configured to take its master clock from the P2 pin on the dataway instead of the internal 1MHz oscillator. To operate in this manner, install a jumper between the pads marked E3 and E4.

2.3 Insertion in the Crate

Inserting the 3232 module into a CAMAC crate is not difficult, but should be done with care to avoid damage to the module. Use the following procedure:

Step	Procedure
1	The 3232 may be inserted in any slot. It should, however, be installed next to its associated memory modules in order to minimize cable length.
2	Insert the card edges into the slots and slide the module back until it stops against the connectors at the back of the slots.
3	Press firmly against the front panel of the module to seat the connectors. Press only until the mounting screw on the front panel can be threaded into the hole on the front of the crate.
4	Finish seating the module into its connectors by tightening the mounting screw.

2.4 Input Wiring

Analog, trigger and external clock input connectors

The 3232 may be ordered with either 2 or 3 pin connectors for the inputs. The Part Numbers and connections for each are shown below.

2 Pin LEMO Connector

Panel Connector	Mating Plug	Connections	
RA0.302NYL	F0.302NYL/3.7	Pin	Description
		1	Input (+)
		2	Input (-)

3 Pin LEMO Connector

Panel Connector	Mating Plug	Connections	
RG0B.303CA322	FG0B.303C0045	Pin	Description
		1	Ground
		2	Input (+)
		3	Input (-)

DAC CON connector - refer to Section 8.

The 3232 may be ordered with or without the DAC CON output. The Part Numbers for the DAC CON connector are:

4 Pin LEMO Connector

Panel Connector	Mating Plug
RG0B.304C322	FG0B.304C004

3. OPERATION

3.1 Introduction

All functions of the 3232 are controlled by CAMAC commands that are summarized in Table 3-1. In the descriptions that follow, commands are gathered into three groups:

1. Data acquisition (load memory). These commands control data input, conversion and memory management. The self-test command is in this group.

2. Unload memory. These commands control the output of data from the transient recorder memory modules.

3. Operating Status. These commands read the contents of the 3232's status registers.

The forms of the commands are presented in a shorthand form. For example

F( ) A( ) D(R or W)

F is the function code of the command and A is the subaddress. The data field, D, may be from 1 to 3 bytes, depending on the instruction. The R or W in the data field indicates whether the information is read (R) from the 3232 or written (W) to the 3232. Some commands have no required data field. The other essential part of the command, the slot number (N), is the slot in the CAMAC crate which the 3232 occupies. When using a double or triple wide module, the leftmost slot which the 3232 occupies is the slot number.

TABLE 3-1
3232 CAMAC Commands

Command Form	Name	Page
Data Acquisition Commands		
F(16) A(0) D(W)	Arm Module	11
F(25) A(0)	Set End of Record Flag	15
F(25) A(1)	Start Self Test	16
F(25) A(2)	Trigger Module	16
F(26) A(0)	Rearm Module	15
Unload Memory Commands		
F(2) A(Y) D(R)	Read Memory Buffer	20
F(16) A(1) D(W)	Enable Unload	17
Operating Status Read Commands		
F(0) A(0) D(R)	Status Register	22
F(0) A(1) D(R)	Post-Trigger Sample Count	24
F(0) A(2) D(R)	Valid Sample Register	24
F(6) A(0) D(R)	Module ID Number	24

3.2 Data Acquisition

A. Arm Module Command

Form:

F(16) A(0) D(W)

where W is a 24 bit number written to the 3232 to set the operating mode.

Description:

Sets the digitizing mode of the 3232, clears the EOR flag if set and sets the memory address pointer to location zero. This command is required before any digitizing sequence can be executed. The data on the dataway write lines set the operating mode as follows:

Bit	Function
W1	Set operating mode 0 = Post-trigger mode 1 = Pre-trigger mode
W2-W5	Set digitizing clock

	Without Compatibility Jumper	Number of Channels For Which This Speed Is Valid
0	External Clock	
1	250 KHz	1
2	167 KHz	1,2
3	100 KHz	1,2,4
4	50 KHz	1,2,4,8
5	20 KHz	1,2,4,8,16
6	10 KHz	1,2,4,8,16,32
7	5 KHz	1,2,4,8,16,32
8	2 KHz	1,2,4,8,16,32
9	1 KHz	1,2,4,8,16,32
A	500 Hz	1,2,4,8,16,32
B	200 Hz	1,2,4,8,16,32
C	100 Hz	1,2,4,8,16,32
D	50 Hz	1,2,4,8,16,32
E	20 Hz	1,2,4,8,16,32
F	10 Hz	1,2,4,8,16,32

W2-W5 Set digitizing clock

	With Compatibility Jumper	Number of Channels For Which This Speed Is Valid
0	External Clock	
1	40 KHz	4,8
2	20 KHz	4,8,16
3	10 KHz	4,8,16,32
4	5 KHz	4,8,16,32
5	2 KHz	4,8,16,32
6	1 KHz	4,8,16,32
7	500 Hz	4,8,16,32
8	200 Hz	4,8,16,32
9	100 Hz	4,8,16,32
A-F	Unused	

W6-W8 Set number of active channels

	With Compatibility Jumper	Without Compatibility Jumper
0	32 channels	32 channels
1	16 channels	16 channels
2	8 channels	8 channels
3	4 channels	4 channels
4	unused	2 channels
5	unused	1 channel

W9-W24 Set post-trigger sample count. This 16-bit field contains the number of sample blocks (16 samples per active channel) to be digitized after receipt of the event trigger in pre-trigger mode. The number of words loaded after the trigger is calculated as follows:

(number of words) = (post-trigger sample count)
X (number of active channels)
X 16 (samples per block)

This field has no effect when operating in the post-trigger mode.

Discussion:

The 3232 includes circuitry necessary to write digitized measurements into up to 1 megaword (12-bits per word) of memory. The amount of memory used is dependent on the settings of the Memory Size switches. (Refer to section 2.2B). Loading proceeds in sequence beginning with channel 0 in the first word.

a. Pre-Trigger Mode. When armed in pre-trigger mode by the Arm Module command, the 3232 immediately begins scanning its inputs, digitizing the input signals and loading the measurements in memory. After all available memory has been filled, the next measurement is loaded in the first memory word and memory is overwritten in sequence. In this way, the latest measurements are always stored in memory.

Upon receipt of the trigger signal, the 3232 continues to digitize in sequence until the number of post-trigger sample blocks specified by the arming CAMAC command have been digitized. When the specified samples have been digitized, the 3232 stops scanning, sets the End of Record (EOR) flag, and saves the address of the oldest sample for channel 0. It also saves the number of valid data samples loaded into memory.

Since the event trigger is asynchronous with the clock, there is a maximum time uncertainty of one clock cycle between the trigger and the first post-trigger sample. Clock jitter is less than 1 microsecond.

b. Post-trigger Mode. Upon receiving the Arm Module command in post-trigger mode, the 3232 sets the memory loading address pointer to zero and waits for the trigger signal. Upon receiving the trigger, the 3232 begins sampling its inputs, digitizing the input signals and loading the measurements in memory. It proceeds in this manner until all available memory has been filled or until a Set End of Record command is sent. The time between the event trigger and the first sample is one sampling clock cycle and has a maximum jitter of less than one microsecond.

When all available memory is filled, the 3232 sets the EOR flag, and ignores all further clocks and triggers until armed by the Arm Module or Rearm Module command.

Because of the time required to digitize samples and load them into memory, all 32 channels cannot be digitized at the highest speeds. At 250 KHz, for example, only 1 channel can be digitized. At speeds of 10 KHz or less, all 32 channels can be handled.

Example:

Assume a 3232 module with the compatibility jumper installed is to be set to operate in pre-trigger mode at 500 samples per second with 32 active channels and 100 post-trigger sample blocks for each channel. Referring to the function table, the write line bits can be defined as follows:

Bit	Value	
W24	0	
W23	0	
W22	0	
W21	0	
W20	0	
W19	0	
W18	0	100 post-trigger sample blocks =
W17	0	0064 hexadecimal =
W16	0	0000 0000 0110 0100 binary
W15	1	
W14	1	For the Post-Trigger sample register:
W13	0	W24 is the most significant bit
W12	0	W9 is the least significant bit
W11	1	
W10	0	
W9	0	
W8	0	
W7	0	0 = 32 channels
W6	0	
W5	0	
W4	1	
W3	1	7 = 500 Hz
W2	1	
W1	1	Pre-trigger mode

To form the Arm Module command data, determine the required dataway write line bits by referring to the function table above. Taking W24 as the most significant bit and W1 as the least significant bit, form a binary number representing the write line bits. Then translate this binary number to decimal, hexadecimal or the required base of the application software in use. The example shown below divides the write lines into 3 bytes of data and gives the binary, hexadecimal and decimal values for this Arm command.

Write Lines	W24		W1
Data in:			
Binary	0000 0000	0110 0100	0000 1111
Hexadecimal	00	64	0F
Decimal	0	100	15

B. Rearm Module

Form:

F(26) A(0)

Description:

Arms the module using the data transmitted with the last Arm Module (F(16) A(0) D(W)) command.

C. Set End of Record (EOR) Flag

Form:

F(25) A(0)

Description:

Sets the EOR flag. Has the effect of stopping digitizing immediately.

D. Trigger Module

Form:

F(25) A(2)

Description:

This command has the same effect as the event trigger input on the front panel. That is, it starts digitizing in post-trigger mode or starts the sample count in pre-trigger mode.

E. Start Self Test

Form:

F(25) A(1)

Description:

Starts self-test sequence. The Arm Module command must be received before the 3232 can execute this command. Returns with Q=0 if the module is not armed.

Discussion:

The self-test command connects a reference triangle wave signal to the analog to digital converter and triggers the module to start digitizing. Unloading memory subsequently allows the digitized data to be compared with the reference waveform.

In post-trigger mode, the self-test command runs until all available memory has been filled. In pre-trigger mode, the self-test command fills available memory and then takes the number of post-trigger samples specified in the Arm Module command.

The self test signal is a 200 Hz triangle wave with an approximate amplitude of $\pm$10.24V or $\pm$5.12V, depending on the gain setting. Refer to Section 2.2A for information on the gain setting switches.

3.3 Unload Memory

A. Enable Unload

Form:

F(16) A(1) D(W)

where W is a 23 bit number written to the 3232 to set the Sample number and the channel number of the next Read Memory Buffer command.

Description:

Sets up the memory unloading sequence. This command is required before the Read Memory Buffer command can actually read memory data. If the compatibility jumper is installed, or if the jumper is not installed, but 4 or more active channels are selected, the data on the write lines is interpreted as follows:

Bit	Function
W1-W18	Sample number of data to be placed in the memory buffer. The first sample (which is the oldest data) is addressed by setting the Sample number to 0.
W19-W23	Channel number of data word to be placed in memory buffer (0-31). Command returns with Q=0 if this channel has not been digitized since the last arm command.

For 2 active channels (without compatibility jumper), the bits are allocated as follows:

W1-W19	Sample Number of requested channel data.
W20	Channel number
W21-W23	Set to 0.

For 1 active channel (without compatibility jumper), the bits are allocated as follows:

W1-W20	Sample Number of requested channel data.
W21-W23	Set to 0.

Discussion:

To read data from memory, the 3232 first must be enabled by the Enable Unload command that specifies the channel number to be read and the Sample Number. The 3232 calculates the address of the first word to be read as follows:

ADDRESS=(address of oldest data in memory)
+(number of active channels) X (Sample Number)
+(requested channel number)

The first word to be unloaded is placed in the memory read buffer. A subsequent Read Memory Buffer (see Section 3.3B, below) command causes the 3232 to place the contents of the buffer on the read lines of the dataway and to increment the memory address by the amount in the command. In this way, a series of Read Memory Buffer commands can read the memory data in any sequence required.

Example:

Assume that the 3232 has been configured as shown in the example in Section 3.2A, above, namely, with 32 active channels and 100 post-trigger samples per channel. To begin reading at the 30th sample after the trigger, first determine the total number of valid samples taken for channel 0 by means of the Read Valid Samples command (refer to Section 3.4C). There are two cases, as follows:

1. If bit 20 (bit 21 if compatibility jumper not installed) of the Valid Sample Register is 0, then memory has not been filled since the module was armed and the address of the oldest data sample is 0. The sample number of the first sample after the trigger is:

   (valid sample count) - (post-trigger sample count * 16)

   If the contents of the Valid Sample Register are 10,000 decimal, then the sample number of the first sample after the trigger in the example is 10000 - (100 X 16) = 8400 decimal. The sample number where unloading starts is 8430.

2. If bit 20 of the Valid Sample Register is set, then memory has been filled at least once. The sample number of the first sample after the trigger is:

   (memory / channels) - (count * 16)

   where:
   memory = total size of memory being used
   channels = number of active channels
   count = post-trigger sample count

   If the size of memory is 65536, then the sample number of the first sample after the trigger is:

   (65536 / 32) - (100 * 16) = 2048 - 1600
   = 448 decimal

   The sample number where unloading starts is 478.

To form the data for the Enable Unload command, express the sample number where unloading is to start as an 18-bit binary number (unless only 1 or 2 channels are active) and the channel number where unloading is to start as a 5-bit binary number. Concatenate the two numbers with the channel number as the high-order bits.

If only 2 channels are active, 19 bits are required to express the sample number in the maximum memory size. Thus the sample number where unloading is to start must be expressed as a 19-bit binary number. A single bit, bit 20 is sufficient for the channel number. Bits 21 to 23 should be set to 0. For one channel, 20 bits are required for the sample number, but no channel number bit is required. Again, set bits 21 to 23 to 0.

R. Read Memory Buffer

Form:

F(2) A(Y) D(R)

where Y is the next sample of the designated channel to read and R is 16 bits of digitized data.

Description:

Read the data from the 3232 for the channel designated by the most recent Enable Unload command. (Refer to section 3.3A.) The value of Y determines which sample will be returned by the next Read Memory Buffer command. The 3232 increments its memory address by (Y+1) * (number of active channels). If this command is received before the Enable Unload command has been executed, the 3232 returns Q=0 and puts zeros on the dataway read lines.

Discussion:

The Enable Unload command determines which channel will be read and with which sample number to start. No data is returned by the Enable Unload command. The Read Memory Buffer command reads the data and determines which sample will be returned by the next Read Memory Buffer command. This method of reading the data and, in the same command, determining what sample will be read next, permits a faster rate of data transfer.

If the address generated by the Read Memory Buffer command is greater than the memory size, then the address wraps around. That is, if the current memory address is the last address in memory, incrementing it by one makes the new memory address 0. Note that it is the programmer's responsibility to make sure the data at any address is valid or acceptable.

Examples:

To read each successive sample for a particular channel, set the value of Y to 0. To read every 4 samples of a channel, set Y to 3.

The data (R) returned is a 2's complement number, sign extended to 16 bits. The table below shows the values returned for 0V, for the minimum absolute voltage and the maximum absolute voltage that each range is able to measure. When using the 0 to 10.24 volt range and the -10.24 to +10.24 volt range, the low order bit is always 0.

RANGE
0 TO +5.12 VOLTS

Input Voltage	Data in Binary	Data in Decimal
0V	0000 0000 0000 0000	0
1.25mV	0000 0000 0000 0001	1
+5.12V	0000 1111 1111 1111	4095

RANGE
0 TO +10.24 VOLTS

Input Voltage	Data in Binary	Data in Decimal
0V	0000 0000 0000 0000	0
2.5mV	0000 0000 0000 0010	2
+10.24V	0001 1111 1111 1110	8190

RANGE
-5.12 TO +5.12 VOLTS

Input Voltage	Data in Binary	Data in Decimal
-5.12V	1111 0000 0000 0000	-4096
-2.5mV	1111 1111 1111 1110	-2
0V	0000 0000 0000 0000	0
+2.5mV	0000 0000 0000 0010	+2
+5.12V	0000 1111 1111 1110	+4094

RANGE
-10.24 TO +10.24 VOLTS

Input Voltage	Data in Binary	Data in Decimal
-10.24V	1110 0000 0000 0000	-8192
-5mV	1111 1111 1111 1100	-4
0V	0000 0000 0000 0000	0
+5mV	0000 0000 0000 0100	+4
+10.24V	0001 1111 1111 1100	+8188

3.4 Operating Status Read Commands

A. Status Register

Form:

F(0) A(0) D(R)

where R is 19 bits of status, indicating the operating mode, the operating state, the memory size, the gain setting, the number of active channels and the clock setting. R is 18 bits when operating with the compatibility jumper installed.

Description:

Places the contents of the 3232 status register on the dataway read lines. The status register bits are as follows:

R1-R3 Operating mode

0 = Clear
1 = Post-trigger Mode
2 = Pre-trigger Mode
3 = Unload Mode

R4-R5 Operating State

0 = Clear
1 = Armed
2 = Armed and Digitizing
3 = Digitizing Sequence Complete

R6-R10 Available Memory

0 = 32K (K = 1024 words)
1 = 64K
2 = 96K
.
.
.
30 = 992K
31 = 1024K

R11-R12 Module Gain (Scale) Setting

0 = 0 - +10 volts
1 = 0 - +5 volts
2 = $\pm$ 5 volts
3 = $\pm$ 10 volts

R13-R14 Number of Active Channels (with compatibility jumper installed)

0 = 32 channels
1 = 16 channels
2 = 8 channels
3 = 4 channels

R13-R15 Number of Active Channels (without compatibility jumper)

0 = 32 channels
1 = 16 channels
2 = 8 channels
3 = 4 channels
4 = 2 channels
5 = 1 channels

R15-R18 Clock Selection (with compatibility jumper)

0 = External Clock
1 = 40 KHz
2 = 20 KHz
3 = 10 KHz
4 = 5 KHz
5 = 2 KHz
6 = 1 KHz
7 = 500 Hz
8 = 200 Hz
9 = 100 Hz

R16-R19 Clock Selection (without compatibility jumper)

0 = External Clock
1 = 250 KHz
2 = 167 KHz
3 = 100 KHz
4 = 50 KHz
5 = 20 KHz
6 = 10 KHz
7 = 5 KHz
8 = 2 KHz
9 = 1 KHz
A = 500 Hz
B = 200 Hz
C = 100 Hz
D = 50 Hz
E = 20 Hz
F = 10 Hz

B. Post-Trigger Sample Count

Form:

F(0) A(1) D(R)

where R is a 16 bit number to be read from the 3232.

Description:

Reads the number of sample blocks specified by the last Arm module command.

C. Valid Sample Register

Form:

F(0) A(2) D(R)

where R is a 21 bit number read from the 3232.

Description:

If the compatibility jumper is not installed, the number of valid samples taken for channel 0 is returned on bits R20-R1. If all available memory has been filled at least once, bit R21 is set. With the compatibility jumper installed, operation is similar except that the number of samples is on R1-R19 and the memory full flag is bit R20. Bit R21 is unused.

D. Module ID Number

Form:

F(6) A(0) D(R)

where R is a 16 bit number read from the 3232.

Description:

Reads the 3232 module identification number. The module identification depends on whether the compatibility jumper is installed, as follows:

	Without Compatibility Jumper	With Jumper
Module ID	940 (decimal)	909 (decimal)

4. MECHANICAL DESIGN

Front panel LED indicators and LEMO connectors for analog, external clock and trigger inputs are shown in figure 4-1. All switches are accessible without disassembling the module. Boards in the module are connected through flat cables and may be disassembled without unsoldering connections.

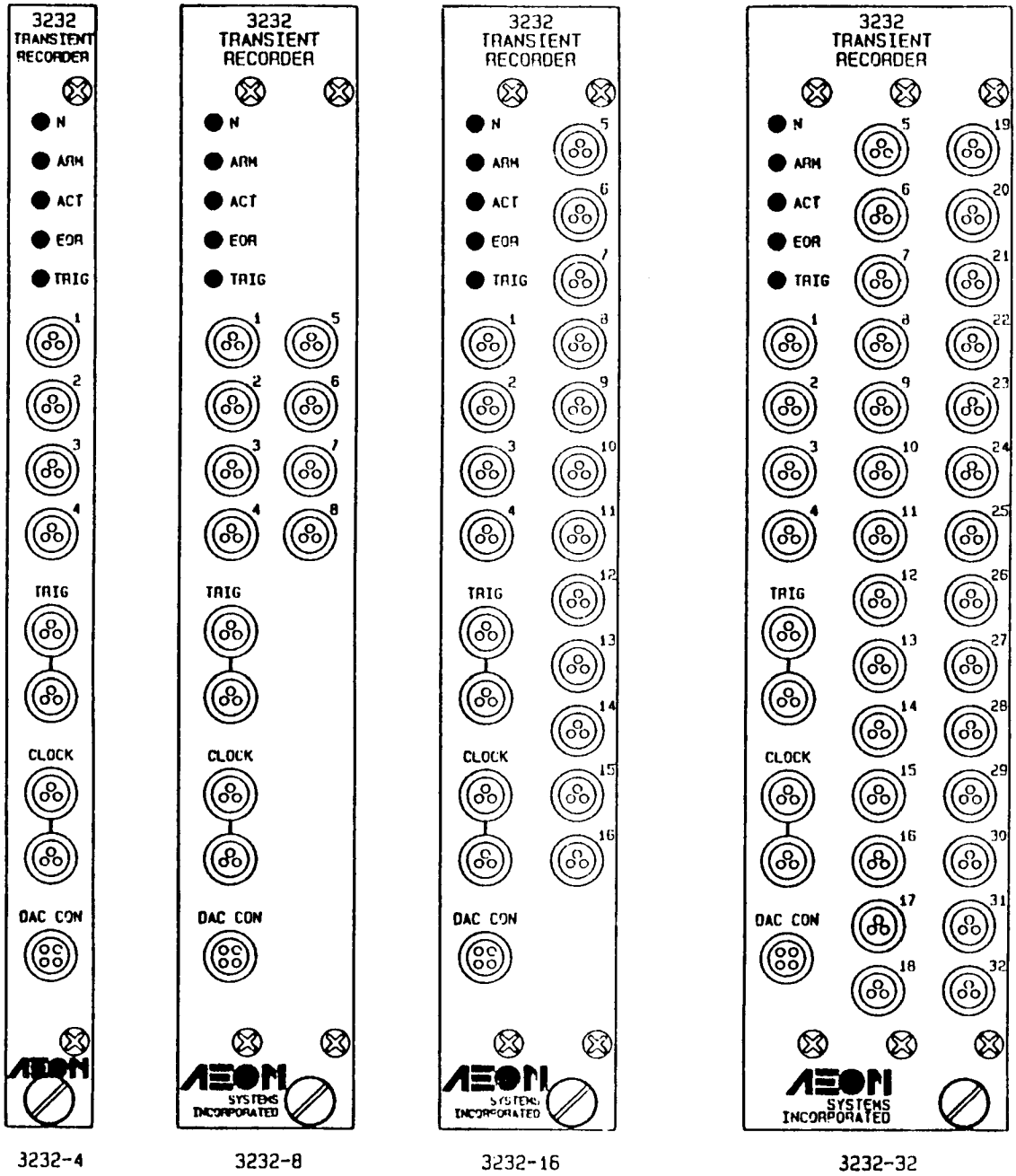


Figure 4-1. Model 3232 Front Panel

5. ELECTRICAL CHARACTERISTICS

a. CAMAC connections. All dataway and power connections conform to IEEE standard 583-1975.

b. Analog input characteristics. Full-scale input ranges can be selected by means of switches on the module. Available ranges are as follows:

0 to 10.24 volts
0 to 5.12 volts
-5.12 to +5.12 volts
-10.24 to +10.24 volts

All inputs are differential and are protected from overvoltages of up to 200 volts.

6. CONVERSION CHARACTERISTICS

a. Resolution. 12 bits
b. Accuracy. $\pm$.03% of full scale $\pm$ 1/2 LSB
c. Missing codes. None
d. Nonlinearity. $\pm$ 1/2 LSB
e. Maximum conversion time. 2 microseconds per channel + 1.7 microseconds overhead.
f. Throughput.
Digitizing - 400×10^3 per second (4 channels)
320×10^3 per second (32 channels)
Memory Unloading - 1×10^6 words per second
g. Output coding. 2's complement with sign extended to 16 bits. Refer to section 3.3B.

7. SELF-TEST

The self-test command connects a reference signal to all inputs and triggers the 3232 to digitize the signal. The test signal has the following characteristics:

Waveform - Triangular
Amplitude - $\pm$5.12 volts at gain = 2
$\pm$10.24 volts at gain = 1
Frequency - 200 Hz

In post-trigger mode, the test signal remains connected until all memory has been filled with samples. In pre-trigger mode, the 3232 fills memory with test samples and then digitizes the number of post-trigger samples set in the last Arm Module command. The 3232 must have received a pre-trigger or post-trigger Arm Module command before the self-test can be executed.

8. DAC CON CONNECTOR

The DAC CON Connector on the front panel allows other devices to monitor the 3232's activity on the memory bus and dataway. This allows a digital to analog converter, for example, to access the sample memory without involving the CAMAC controller. The four-pin LEMO connector has the following pin-out:

Pin 1	ARM. Indicates that the 3232 is armed. Active HIGH.
Pin 2	UNLOAD. Indicates that the 3232 has received an Enable Unload command. Active HIGH.
Pin 3	ENADD (Address Enable). In conjuction with ARM or UNLOAD, indicates that the indicated bus activity is in progress. Active HIGH.
Pin 4	N. Indicates that a CAMAC command has addressed the 3232. Active LOW.

The 3232 may be ordered with or without the DAC CON connection.

APPENDIX A
908 Compatibility Mode

The 3232 can be operated either in a "native" mode or in a mode in which its operation is compatible with the Princeton model 908 transient digitizer. The major difference between these modes is in the available sampling rates.

Sampling rate is determined by dividing down either an internal clock or an external clock signal. If the 908 compatibility jumper is installed, the maximum internal clock rate is 40 KHz. Clock rates are selected by the Arm Module command as described in Section 3.2A. The following sampling rates are available.

With Compatibility Jumper

Rate	Number of inputs for which this rate may be used
40 KHz	4,8
20 KHz	4,8,16
10 KHz	4,8,16,32
5 KHz	4,8,16,32
2 KHz	4,8,16,32
1 KHz	4,8,16,32
500 Hz	4,8,16,32
200 Hz	4,8,16,32
100 Hz	4,8,16,32

Princeton University: PPPL Computer Division

To: Distribution Date: July 16, 1987

From: W. Rauch Subject: Overdriven H911 Scaler and H908/3232 Digitizer CAMAC Module Input Optical Device

W Rauch

==========

H911 PROBLEM

The H911 Scaler receives and counts pulses on 32 optical isolated inputs. The receiver chips are Hewlett Packard 2601's. Each contains a light emitting diode, thereby providing optical isolation. The anomaly identified is a tendency for some of these chips to turn back on during turn-off. This turn-on, turn-off, turn-on, turn-off transition exceeds the logic thresholds of the succeeding logic buffer (TTL chip) and results in two pulses when actually only one was received at the input. This is shown in Fig. 1.

H911 RESOLUTION

Further examination (see attachment A) shows that the existing H911 2601 forward light emitting diode current (I_F) could be as great as 35 ma. However, its absolute maximum specified rating is only 20 ma. For the H911 it was shown that the series terminating resistor should be approximately 390 Ω instead of 100 Ω to provide the recommended I_F of 6.3 ma (see attachment B). Figure 2 substantiates the effect of changing this resistor to the appropriate value.

H911 IMPACT

Eighteen scalers are presently in service. Diagnosticians recognized this anomaly as a system problem quite some time ago, and have the

ability through a software switch to compensate for double pulses. Changing the resistor value would be transparent to the system where they are presently used.

H908 AND H3232 DIGITIZER

The External Clock and trigger inputs of the H908 and H3232 digitizer use the same optical isolated input device. The trigger input has been determined to not be of concern, because of the nature of the internal logic of the digitizer. However, the External Clock input was shown that if driven by the 904 and 412 timing and sequencing modules, that the same double pulsing occurs. The present circuit could be driven by as much as 68 ma I_F, which exceeds the 20 ma absolute maximum rating (see Attachment A). Replacing the 51 Ω terminating resistor with a nominal value of 390 Ω was verified to correct the problem (see Attachment C) at a nominal I_F of 10 ma.

Because only a few applications use the configuration that requires the External Clock input, I would suggest that a series external terminating resistor be inserted at the digitizer end of the External Clock signal cable (possible in a Pamona box).

WR:vz
Attachments
Distribution
N. Arnold
W. Bergin
H. Feng
S. Hosein
G. Kolinchak
J. Montague
P. Sichta
J. Wertenbaker

cc: G. Oliaro
N. Sauthoff
K. Young

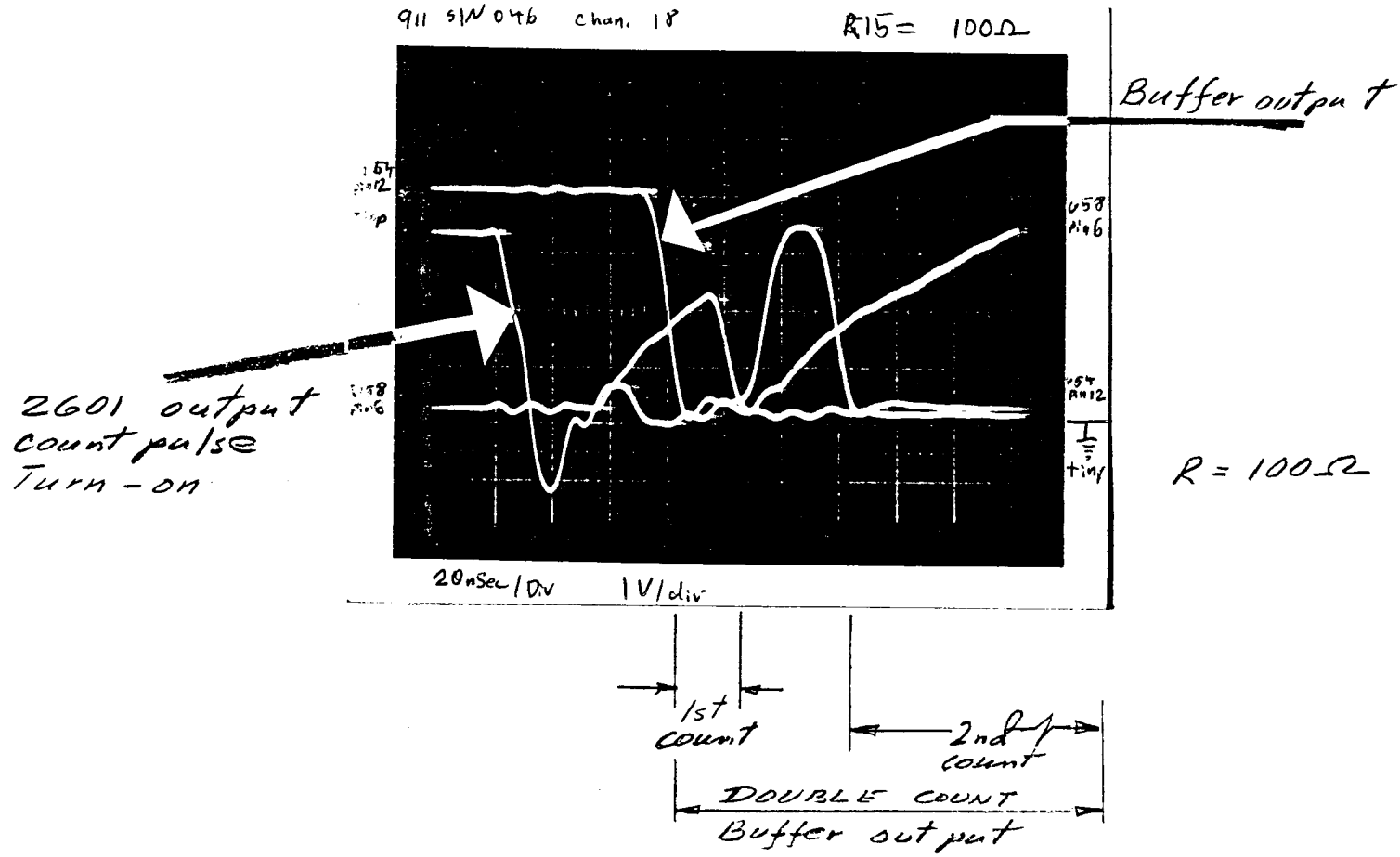


Figure 1

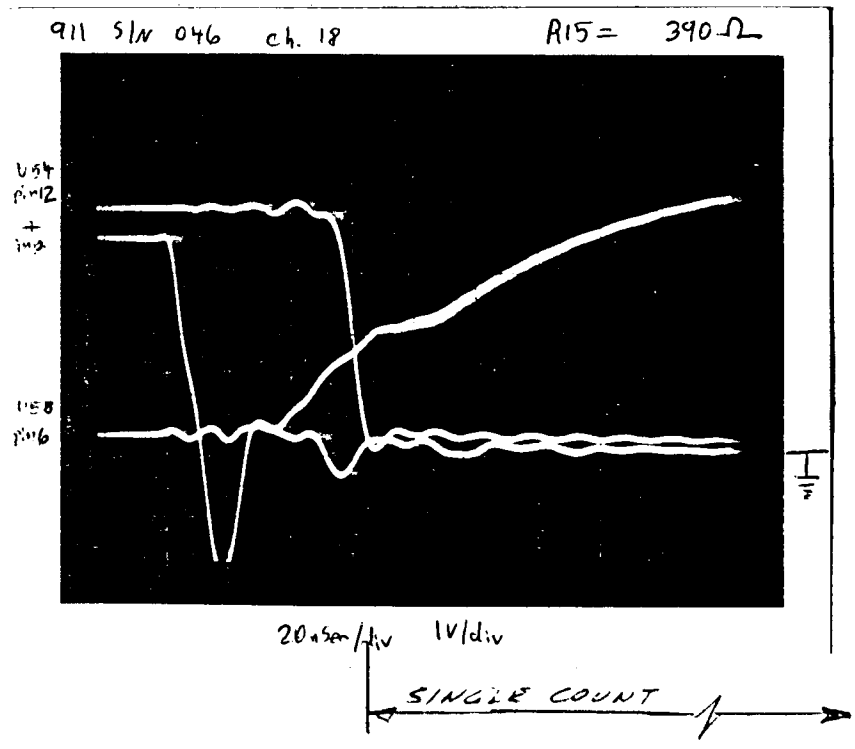


Figure 2

2601 opto Isolator Specs

Input Forward Voltage $V_{F_{TYP}} = 1.5V$, $V_{max} = 1.75V$ } $I_F = 10ma$

Recommended $I_F = 6.3ma$ at $V_{cc} = 5 \pm .5V$

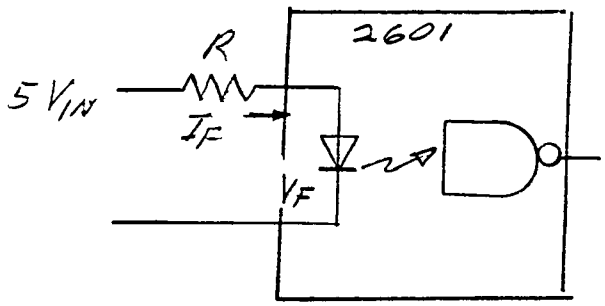
Absolute Max $I_F = 20ma$

Input diode Temperature coefficient

$$\frac{\Delta V_F}{\Delta T_A} = -1.6 \text{ mV}/^{\circ}C \text{ at } I_F = 10_{ma}$$

H911, $R = 100\Omega$

$$I_F = \frac{V_{IN} - V_F}{100} = \frac{5-1.5}{100} = 35ma$$



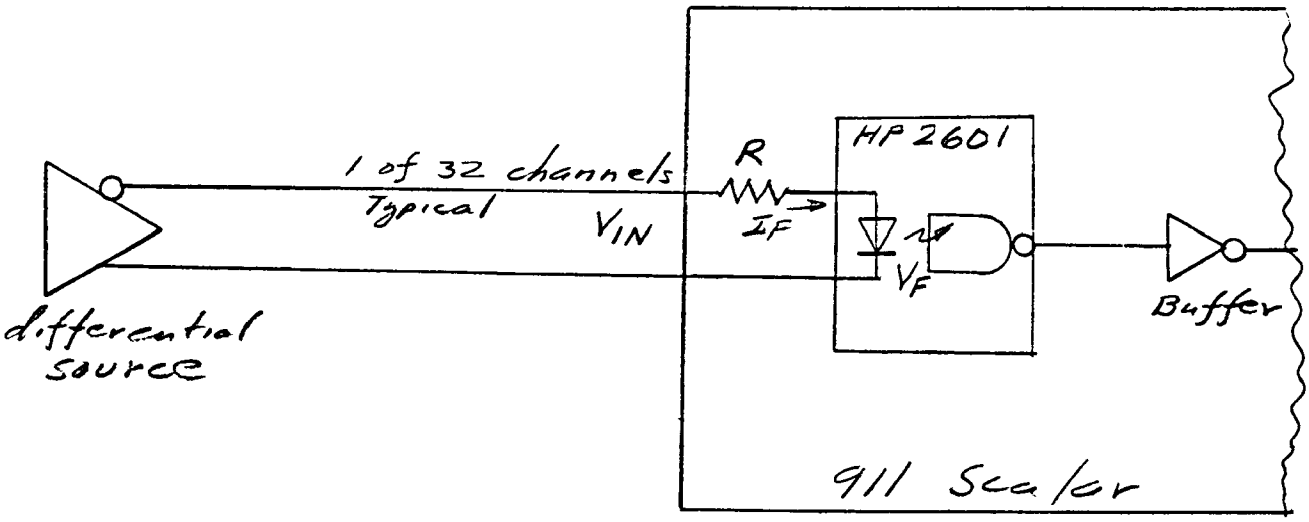
H908 and 3232 EXT CLK, $R = 51\Omega$

$$I_F = \frac{V_{IN} - V_F}{51} = \frac{5-1.5}{51} = 68ma$$

ATTACHMENT A

H911 Multi-channel latching scalar

$V_{IN_{MIN}} = 3V$
$V_{IN_{MAX}} = 5V$ differential (per 911 spec)



$I_F = 6.3ma$ recommended by mfg.

$$R_{MIN} = \frac{V_{IN_{MIN}} - V_{F_{MAX}}}{I_F} = \frac{3 - 1.75}{6.3\,ma} = \frac{1.25}{6.3ma} = 198\,\Omega$$

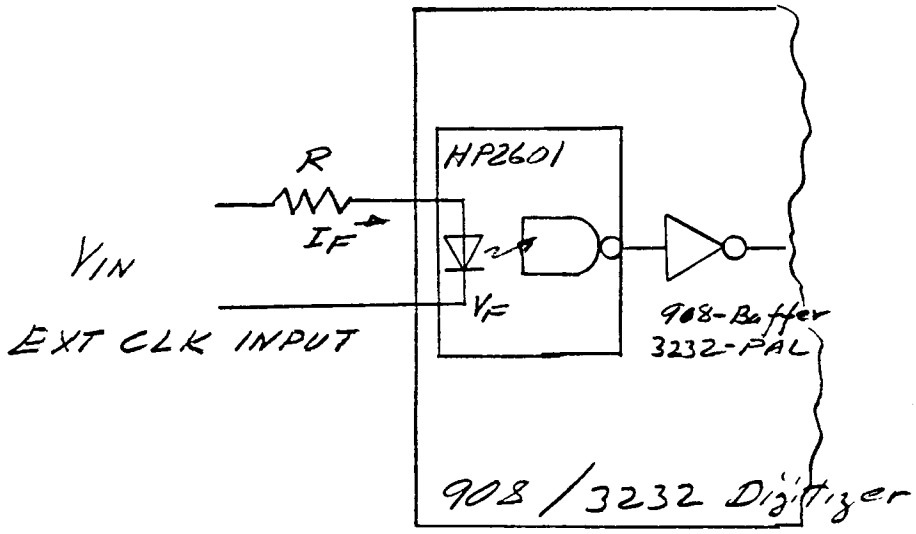
$$R_{max} = \frac{V_{IN_{MAX}} - V_{TYP}}{I_F} = \frac{5 - 1.5}{6.3ma} = \frac{3.5}{6.3ma} = 555\,\Omega$$

$$R_{NOM} = \frac{V_{NOM} - V_{TYP}}{I_{F_{NOM}}} = \frac{4 - 1.5}{6.3\,ma} = 396\,\Omega$$

ATTACHMENT B

H908 & 3232 Transient Digitizer

EXT CLK $V_{IN} = 5V \pm 20\%$ (per TFTR-10A2-H57)
$= 5V \pm 1V$



use $I_F = 10$ ma

$$R_{MIN} = \frac{V_{IN_{MIN}} - V_{F_{MAX}}}{I_F} = \frac{4 - 1.75}{10\text{ ma}} = 225\ \Omega$$

$$R_{MAX} = \frac{V_{IN_{MAX}} - V_{TYP}}{I_F} = \frac{6 - 1.5}{10\text{ ma}} = 450\ \Omega$$

$$R_{NOM} = \frac{V_{IN_{NOM}} - V_{TYP}}{I_{F_{NOM}}} = \frac{5 - 1.5}{10\text{ ma}} = 350\Omega \quad \text{use } 390\Omega$$

ATTACHMENT C

ADC CLOCK TIMING ADJUSTMENT

To perform tests that rely on EOC (end of convert from ADC), it will be necessary to perform timing adjustments to the ADC clock.

2.05 Set memory size switches to 64K

Select test 12...

Set clock = 10 KHz

Set mode = post-trigger

Set number of active channels = 4

Loop on one channel (any channel)

Attach chan 1 scope probe to U 41 pin 13 (CLKCH) and trigger on this.
Attach chan 2 scope probe to ADC pin 17 (on back of control board). This signal is ADC clock out.
Confirm that chan. 1 shows 4 positive going pulses, 100 nS in width. These pulses should be in a group that occurs every 100 uS.
Expand scope time base to show four positive pulses of scope chan. 1.
Adjust R 19 so that rep. rate of CLKCH = 2.2 uS. (Pos. portion of CLKCH will remain at approx. 100 uS.).
Observe scope chan. 2, carefully adjust R 19 so that 13 positive going pulses occur, the last one being before the rising edge of CLKCH.
NOTE: CLKCH will jump in 100 nS increments. Be careful that CLKCH remains at 2.2 uS and ADC clock out shows 13 positive pulses.

3232 INPUT PROTECTION MODIFICATION

John Wertenbaker
6/9/06

PURPOSE: The 3232 Transient Digitizer inputs are protected for 200V, according to the manual. Last year, 4 digitizers were destroyed by bad hi-pots and a plasma disruption. 3 of those digitizers were in the same rack. When the inputs blow, the clamping diodes, which are across the power supply, short out the power supply and overheat. If the overheating components are left to simmer for a long time, they will eventually burn holes in the printed circuit board. Many digitizers have been damaged beyond repair this way.

DESCRIPTION: The existing input protection consists of series constant-current diodes and parallel input clamping diodes. See the top figure. These constant current diodes are rated at 240 volts, and they short when this voltage is exceeded. The modification replaces these series diodes with a 1 Megohm resistor paralleled by a .01uf 1,000 volt capacitor, on each leg of the input. The resistors limit the current to the input protection diodes. The capacitors compensate for higher frequency attenuation. This raises the input protection to 500V.